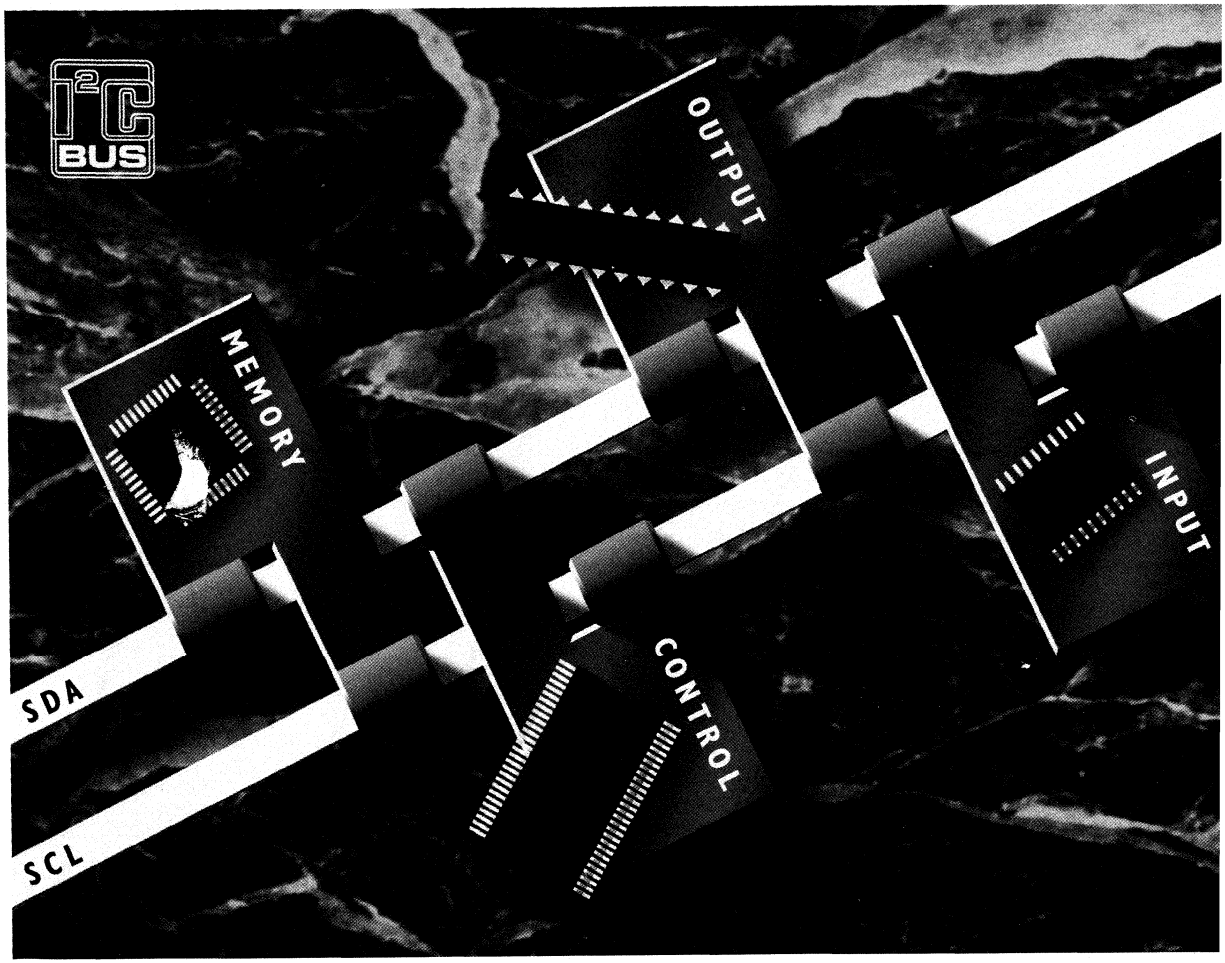
TEGRATED CIRCUITS

I^2C Peripherals



1996

DATA HANDBOOK IC12

Philips Semiconductors

PHILIPS

QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

I²C Peripherals

CONTENTS

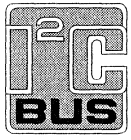
DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

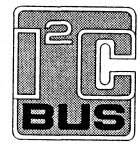
PURCHASE OF PHILIPS I²C COMPONENTS



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

PREFACE

When Philips first introduced the 2-wire I²C-bus, or 'Inter-Integrated Circuit' bus, in the early 1980s it was never anticipated that 15 years later the I²C-bus would be a worldwide industry standard.



The I²C-bus was originally developed as a control bus for linking microcontroller and peripheral ICs for Philips consumer products. The elegant simplicity of a 2-wire bus that combined both address and data bus functions was quickly adopted in such diverse applications as:

- Telecommunications (wirebound and wireless handsets in particular)
- Automotive dashboards
- EDP (as a diagnostics bus)
- Energy management systems
- Test and measurement products
- Medical equipment
- Point of sales terminals
- Security systems
- Toys, even!

Spreading first throughout Europe, and then Asia, I²C-bus has made major inroads in North America in the '90s where interest in I²C-bus has risen dramatically. As soon as embedded systems designers realize the cost, space, and flexibility of this robust serial protocol, they are hooked on I²C.

No longer a Philips-only concept, I²C has been licensed to over a dozen manufacturers who now produce over 500 I²C-bus compatible devices. I²C-bus based system designs require no special licence, and the I²C-bus protocol is easily implemented by virtually any microcontroller on the market.

This I²C-bus peripherals data handbook contains a collection of data sheets and related information about Philips general purpose I²C-bus compatible ICs.

Application-specific devices with I²C-bus are listed but are not included (i.e. tuner ICs, synthesizers, etc.). They can be found in Philips application-specific data handbooks.

With this latest edition of the I²C-bus peripherals data handbook, we hope to provide you with a useful guide to the diverse range of I²C-bus peripheral products from Philips Semiconductors. Philips also provides a wide range of microcontroller products with dedicated I²C-bus interface in 8048, 8051, and 68000 flavours. Ask your local Philips Semiconductors representative for further information about I²C-bus microcontrollers, demo boards, emulators, evaluation tools and application notes. They will be happy to help you with your I²C-bus based designs.

SELECTION GUIDE

Selection guide — Functional index

GENERAL

PHILIPS SEMICONDUCTORS ASSIGNED I²C-BUS ADDRESSES

Type number	Description	I²C slave address						
		A6	A5	A4	A3	A2	A1	A0
–	General call address	0	0	0	0	0	0	0
–	Reserved addresses	0	0	0	0	X	X	X
NE5751	Audio processor for RF communication	1	0	0	0	0	0	A
PCA1070	Programmable speech transmission IC	0	1	0	0	0	1	A
PCA8510	Stand-alone OSD circuit	1	0	1	1	1	0	1
PCA8516	Stand-alone OSD IC	1	0	1	1	1	0	1
PCA8581/C	128 × 8-bit EEPROM	1	0	1	0	A	A	A
PCB5020	Digital audio signal processor for car radio including ROM	0	0	1	1	0	A	A
PCB5021	Digital audio signal processor for car radio excluding ROM	0	0	1	1	0	A	A
PCD3311C	DTMF/modem/musical tone generator	0	1	0	0	1	0	A
PCD3312C	DTMF/modem/musical-tone generator	0	1	0	0	1	0	A
PCD4430	Programmable tone detector and DTMF generator	0	1	0	0	0	0	A
PCD4440	Analog voice scrambler/descrambler for mobile telephones	1	1	0	1	1	1	A
PCD5002	Pager decoder	0	1	0	0	1	1	1
PCF1810	8 × 8 cross-point matrix analog switch	0	0	1	1	1	A	A
PCF2116	LCD controller/driver	0	1	1	1	0	1	A
PCF8566	96-segment LCD driver 1:1 - 1:4 Mux rates	0	1	1	1	1	1	A
PCF8568	LCD row driver for dot matrix displays	0	1	1	1	1	0	A
PCF8569	LCD column driver for dot matrix displays	0	1	1	1	1	0	A
PCF8570/C	256 × 8-bit static RAM	1	0	1	0	A	A	A
PCF8573	Clock/calendar	1	1	0	1	0	A	A
PCF8574	8-bit remote I/O port (I²C-bus to parallel converter)	0	1	0	0	A	A	A
PCF8574A	8-bit remote I/O port (I²C-bus to parallel converter)	0	1	1	1	A	A	A
PCF8576	16-segment LCD driver 1:1 - 1:4 Mux rates	0	1	1	1	0	0	A
PCF8577A	32/64-segment LCD display driver	0	1	1	1	0	1	1
PCF8577C	32/64-segment LCD display driver	0	1	1	1	0	1	0
PCF8578	Row/column LCD dot matrix driver/display	0	1	1	1	1	0	A
PCF8579	Row/column LCD dot matrix driver/display	0	1	1	1	1	0	A
PCF8582/A	256 × 8-bit CMOS EEPROM	1	0	1	0	A	A	A
PCF8583	256 × 8-bit RAM/clock/calendar	1	0	1	0	0	0	A
PCF8591	4-channel, 8-bit Mux ADC and one DAC	1	0	0	1	A	A	A
PCF8593	Low-power clock calender	1	0	1	0	0	0	1

Type number	Description	I²C slave address						
		A6	A5	A4	A3	A2	A1	A0
PCX8594X-2	512 × 8-bit CMOS EEPROM	1	0	1	0	A	A	P
PCX8598X-2	1024 × 8-bit CMOS EEPROM	1	0	1	0	A	P	P
SAA1064	4-digit LED driver	0	1	1	1	0	A	A
SAA1136	PCM audio interface	0	0	1	1	1	0	0
SAA1137	PCM audio processor	0	1	0	0	0	0	A
SAA1300	Tuner switch circuit	0	1	0	0	0	A	A
SAA1770	D2MAC decoder for satellite and cable TV	0	0	1	1	1	1	A
SAA2502	MPEG audio source decoder	0	0	1	1	1	0	1
SAA2510	Video-CD MPEG-audio/video decoder	0	0	1	1	0	1	A
SAA4700	VPS dataline processor	0	0	1	0	0	0	A
SAA5240A	625-line teletext decoder; english/german/swedish	0	0	1	0	0	0	1
SAA5240B	625-line teletext decoder; french/italian/german	0	0	1	0	0	0	1
SAA5240P/D	625-line teletext decoder; spanish	0	0	1	0	0	0	1
SAA5240P/C	625-line teletext decoder; arabic	0	0	1	0	0	1	0
SAA5240P/F	625-line teletext decoder; hebrew	0	0	1	0	0	0	1
SAA5241A	625-line teletext decoder; english/german/swedish	0	0	1	0	0	0	1
SAA5241B	625-line teletext decoder; french/italian/german	0	0	1	0	0	0	1
SAA5243P/K	Computer controlled teletext circuit	0	0	1	0	0	0	1
SAA5243P/L	Computer controlled teletext circuit	0	0	1	0	0	0	1
SAA5243P/H	Computer controlled teletext circuit	0	0	1	0	0	0	1
SAA5243P/E	Computer controlled teletext circuit	0	0	1	0	0	0	1
SAA5244	Integrated VIP and teletext	0	0	1	0	0	0	1
SAA5245	525-line teletext decoder/controller	0	0	1	0	0	0	1
SAA5246	Integrated VIP and teletext	0	0	1	0	0	0	1
SAA5252	Line 21 decoder	0	0	1	0	1	0	0
SAA7110	Digital multistandard decoder	1	0	0	1	1	1	A
SAA7140	High performance video scaler	0	1	1	1	0	0	A
SAA7151B	8-bit digital multistandard TV decoder	1	0	0	0	1	A	1
SAA7152	Digital comb filter	1	0	1	1	0	0	1
SAA7165	Video enhancement D/A processor	1	0	1	1	1	1	1
SAA7186	Digital video scaler	1	0	1	1	1	A	0
SAA7191	Digital multistandard TV decoder	1	0	0	0	1	A	1
SAA7192A	Digital colour space-converter	1	1	1	0	0	0	A

Type number	Description	I²C slave address						
		A6	A5	A4	A3	A2	A1	A0
SAA7194	Digital video decoder/scaler	0	1	0	0	0	0	A
SAA7199B	Digital multistandard encoder	1	0	1	1	0	0	A
SAA7250	General purpose digital audio signal processor	0	0	1	1	0	0	A
SAA7370	CD-decoder plus digital servo processor	0	0	1	1	0	0	A
SAA9020	Field memory controller	0	0	1	0	1	A	A
SAA9041	Digital video text - backend	0	0	1	0	0	0	1
SAA9051	Digital multistandard colour TV decoder	1	0	0	0	1	A	1
SAA9053	Digital NTSC TV decoder	1	0	0	0	1	A	1
SAA9056	Digital SECAM colour decoder	1	0	0	0	1	A	1
SAA9060	Black and white PIP	1	0	0	0	1	1	0
SAA9065	Video enhancement and D/A processor	1	0	1	1	1	1	1
SAB3028	Remote control RC-5 transcoder	0	1	0	0	1	1	0
SAB3035	Digital tuning circuit for computer-controlled TV	1	1	0	0	0	A	A
SAB3036	Digital tuning circuit for computer-controlled TV	1	1	0	0	0	A	A
SAB3037	Digital tuning circuit for computer-controlled TV	1	1	0	0	0	A	A
SAB9070	PIP8 controller	0	0	1	0	0	1	0
SAF1134P	Dataline 16 decoder for VPS (gate array)	0	0	1	0	0	A	A
SAF1135P	Dataline 16 decoder for VPS (cell array)	0	0	1	0	0	A	A
TDA1551B	2 × 22 W BTL audio power amplifier	1	1	0	1	1	0	1
TDA1551Q	2 × 22 W BTL audio power amplifier	1	1	0	1	1	0	0
TDA4670	Picture signal improvement (PSI) circuit	1	0	0	0	1	0	0
TDA4670	Picture signal improvement (PSI) circuit	1	0	0	0	1	0	0
TDA4671	Picture signal improvement (PSI) circuit	1	0	0	0	1	0	0
TDA4672	Picture signal improvement (PSI) circuit	1	0	0	0	1	0	0
TDA4680	Video processor	1	0	0	0	1	0	0
TDA4685	Video processor	1	0	0	0	1	0	0
TDA4687	Video processor	1	0	0	0	1	0	0
TDA4688	Video processor	1	0	0	0	1	0	0
TDA4780	Video control with gamma control	1	0	0	0	1	0	0
TDA6360	Five-band equalizer for car radio	1	0	0	0	0	1	A
TDA8045	QAM-64 demodulator	0	0	0	1	1	A	A
TDA8363	Single chip NTSC decoder	1	0	0	0	1	0	0
TDA8366	One-chip multistandard video	1	0	0	0	1	0	1

Type number	Description	I²C slave address						
		A6	A5	A4	A3	A2	A1	A0
TDA8370	High/medium perf. sync. processor	1	0	0	0	1	1	0
TDA8376	One-chip multistandard video	1	0	0	0	1	0	1
TDA8405	Stereo/dual language decoder	1	0	0	0	0	1	0
TDA8415	TV/VCR stereo/dual sound processor	1	0	0	0	0	1	0
TDA8416	TV/VCR stereo/dual sound processor	1	0	1	1	0	1	0
TDA8417	TV/VCR stereo/dual sound processor	1	0	0	0	0	1	0
TDA8420	Audio processor with loudspeaker and headphone channel	1	0	0	0	0	0	A
TDA8421	Audio processor with loudspeaker and headphone channel	1	0	0	0	0	0	A
TDA8424	Audio processor with loudspeaker channel	1	0	0	0	0	0	1
TDA8425	Audio processor with loudspeaker channel	1	0	0	0	0	0	1
TDA8426	Hi-fi stereo audio processor	1	0	0	0	0	0	1
TDA8432	Sync. controller and deflection processor	1	0	0	0	1	1	A
TDA8433	TV deflection processor	1	0	0	0	1	1	A
TDA8440	Video/audio switch	1	0	0	1	A	A	A
TDA8442	Interface for colour decoder	1	0	0	0	1	0	0
TDA8443/A	YUV/RGB matrix switch	1	1	0	1	A	A	A
TDA8444	Octal 6-bit DAC	0	1	0	0	A	A	A
TDA8461	PAL/NTSC colour decoder with RGB processor	1	0	0	0	1	0	A
TDA8466	PAL/NTSC colour decoder with RGB processor	1	0	0	0	1	0	A
TDA8480	RGB gamma-correction processor	1	0	0	0	0	1	A
TDA8540	4 × 4 video switch matrix	1	0	0	1	A	A	A
TDA9140	Alignment-free multistandard decoder	1	0	0	0	1	A	1
TDA9141	Alignment-free multistandard decoder	1	0	0	0	1	A	1
TDA9145	Multistandard decoder	1	0	0	0	1	0	1
TDA9150	Deflection processor	1	0	0	0	1	1	0
TDA9160	Multistandard decoder/sync. processor	1	0	0	0	1	A	1
TDA9161	Bus-controlled decoder/sync. processor	1	0	0	0	1	0	1
TDA9162	Multistandard decoder/sync. processor	1	0	0	0	1	A	1
TDA9840/T	TV stereo/dual sound processor	1	0	0	0	0	1	0
TDA9860	Hi-fi audio processor	1	0	0	0	0	0	A
TEA6000	FM/IF and search tuning interface	1	1	0	0	0	0	1
TEA6100	FM/IF for computer-controlled radio	1	1	0	0	0	0	1
TEA6300	Sound fader control and preamplifier/source selector	1	0	0	0	0	0	0

Type number	Description	I²C slave address						
		A6	A5	A4	A3	A2	A1	A0
TEA6320	4-input tone/volume controller with fader control	1	0	0	0	0	0	0
TEA6330	Tone/volume controller	1	0	0	0	0	0	0
TEA6360	5-band equalizer	1	0	0	0	1	1	A
TSA5510	1.2 GHz PLL frequency synthesizer without AFC ADC	1	1	0	0	0	A	A
TSA5511	1.3 GHz PLL frequency synthesizer for TV	1	1	0	0	0	A	A
TSA5512	1.3 GHz PLL frequency synthesizer for TV	1	1	0	0	0	A	A
TSA5514	1.3 GHz PLL frequency synthesizer for TV	1	1	0	0	0	A	A
TSA5519	1.3 GHz PLL frequency synthesizer ADC	1	1	0	0	0	A	A
TSA6057	Radio tuning PLL frequency synthesizer	1	1	0	0	0	1	A
TSA6060	Radio tuning PLL frequency synthesizer	1	1	0	0	0	1	A
TSA6061	150 MHz PLL and IF-counter	1	1	0	0	0	1	A
UMA1000T	Data processor for mobile telephones	1	1	0	1	1	A	A
UMA1009	Frequency synthesizer for mobile telephones	1	1	0	0	0	A	A
UMA1010	Frequency synthesizer for mobile telephones	1	1	0	0	0	A	A
UMA1014T	Frequency synthesizer for mobile telephones	1	1	0	0	0	1	A
–	Reserved addresses	1	1	1	1	X	X	X

X = Don't care
A = Programmable address bit
P = Page selection bit

PHILIPS SEMICONDUCTORS I²C-BUS ADDRESS ALLOCATION TABLE

GROUP 0 (000)				
0	0	0	–	General call address
X	X	X	–	Reserved addresses
GROUP 1 (0001)				
1	A1	A0	TDA8045	QAM-64 demodulator
GROUP 2 (0010)				
0	0	A0	SAA4700	VPS dataline processor
0	0	1	SAA5240A	625-line teletext decoder; english/german/swedish
0	0	1	SAA5240B	625-line teletext decoder; french/italian/german
0	0	1	SAA5240P/F	625-line teletext decoder; hebrew
0	0	1	SAA5240P/D	625-line teletext decoder; spanish
0	0	1	SAA5241A	625-line teletext decoder; english/german/swedish
0	0	1	SAA5241B	625-line teletext decoder; french/italian/german
0	0	1	SAA5243P/H	Computer controlled teletext circuit
0	0	1	SAA5243P/K	Computer controlled teletext circuit
0	0	1	SAA5243P/L	Computer controlled teletext circuit
0	0	1	SAA5243P/E	Computer controlled teletext circuit
0	0	1	SAA5244	Integrated VIP and teletext
0	0	1	SAA5245	525-line teletext decoder/controller
0	0	1	SAA5246	Integrated VIP and teletext
0	0	1	SAA9041	Digital video text - backend
0	1	0	SAA5240P/C	625-line teletext decoder; arabic
0	1	0	SAB9070	PIP8 controller
0	A1	A0	SAF1134P	Dataline 16 decoder for VPS (gate array)
0	A1	A0	SAF1135P	Dataline 16 decoder for VPS (cell array)
1	0	0	SAA5252	Line 21 decoder
1	A1	A0	SAA9020	Field memory controller
GROUP 3 (0011)				
0	0	A0	SAA7250	General purpose digital audio signal processor
0	0	A0	SAA7370	CD-decoder plus digital servo processor
0	A1	A0	PCB5020	Digital audio signal processor for car radio incl. ROM
0	A1	A0	PCB5021	Digital audio signal processor for car radio excl. ROM
0	1	A0	SAA2510	Video-CD MPEG-audio/video decoder
1	0	0	SAA1136	PCM audio interface

GROUP 3 (0011)				
1	0	1	SAA2502	MPEG audio source decoder
1	A1	A0	PCF1810	8 × 8 cross-point matrix analog switch
1	1	A0	SAA1770	D2MAC decoder for satellite and cable TV
GROUP 4 (0100)				
0	0	A0	PCD4430	Programmable tone detector and DTMF generator
0	0	A0	SAA1137	PCM audio processor
0	0	A0	SAA7194	Digital video decoder/scaler
0	1	A0	PCA1070	Programmable speech transmission IC
0	A1	A0	SAA1300	Tuner switch circuit
1	0	A0	PCD3311C	DTMF/modem/musical tone generator
1	0	A0	PCD3312C	DTMF/modem/musical-tone generator
1	1	0	SAB3028	Remote control RC-5 transcoder
1	1	1	PCD5002	Pager decoder
A2	A1	A0	PCF8574	8-bit remote I/O port (I²C-bus to parallel converter)
A2	A1	A0	TDA8444	Octal 6-bit DAC
GROUP 7 (0111)				
0	0	A0	PCF8576	16-segment LCD driver 1:1 - 1:4 Mux rates
0	0	A0	SAA7140	High performance video scaler
0	1	A0	PCF2116	LCD controller/driver
0	1	0	PCF8577C	32/64-segment LCD display driver
0	A1	A0	SAA1064	4-digit LED driver
0	1	1	PCF8577A	32/64-segment LCD display driver
1	0	A0	PCF8568	LCD row driver for dot matrix displays
1	0	A0	PCF8569	LCD column driver for dot matrix displays
1	0	A0	PCF8578	Row/column LCD dot matrix driver/display
1	0	A0	PCF8579	Row/column LCD dot matrix driver/display
1	1	A0	PCF8566	96-segment LCD driver 1:1 - 1:4 Mux rates
A2	A1	A0	PCF8574A	8-bit remote I/O port (I²C-bus to parallel converter)
GROUP 8 (1000)				
0	0	A0	NE5751	Audio processor for RF communication
0	0	A0	TDA8420	Audio processor with loudspeaker and headphone channel
0	0	A0	TDA8421	Audio processor with loudspeaker and headphone channel
0	0	A0	TDA9860	Hi-fi audio processor
0	0	0	TEA6300	Sound fader control and preamplifier/source selector

GROUP 8 (1000)				
0	0	0	TEA6320	4-input tone/volume controller with fader control
0	0	0	TEA6330	Tone/volume controller
0	0	1	TDA8424	Audio processor with loudspeaker channel
0	0	1	TDA8425	Audio processor with loudspeaker channel
0	0	1	TDA8426	Hi-fi stereo audio processor
0	1	A0	TDA6360	Five-band equalizer for car radio
0	1	0	TDA8405	Stereo/dual language decoder
0	1	0	TDA8415	TV/VCR stereo/dual sound processor
0	1	0	TDA8417	TV/VCR stereo/dual sound processor
0	1	A0	TDA8480	RGB gamma-correction processor
0	1	0	TDA9840/T	TV stereo/dual sound processor
1	0	0	TDA4670	Picture signal improvement (PSI) circuit
1	0	0	TDA4670	Picture signal improvement circuit
1	0	0	TDA4671	Picture signal improvement circuit
1	0	0	TDA4672	Picture signal improvement (PSI) circuit
1	0	0	TDA4680	Video processor
1	0	0	TDA4685	Video processor
1	0	0	TDA4687	Video processor
1	0	0	TDA4688	Video processor
1	0	0	TDA4780	Video control with gamma control
1	0	0	TDA8363	Single chip NTSC decoder
1	0	0	TDA8442	Interface for colour decoder
1	0	A0	TDA8461	PAL/NTSC colour decoder with RGB processor
1	0	A0	TDA8466	PAL/NTSC colour decoder with RGB processor
1	0	1	TDA8366	One-chip multistandard video
1	0	1	TDA8376	One-chip multistandard video
1	0	1	TDA9145	Multistandard decoder
1	0	1	TDA9161	Bus-controlled decoder/sync. processor
1	1	0	SAA9060	Black and white PIP
1	1	0	TDA8370	High/medium perf. sync. processor
1	1	A0	TDA8432	Sync. controller and deflection processor
1	1	A0	TDA8433	TV deflection processor
1	1	0	TDA9150	Deflection processor
1	1	A0	TEA6360	5-band equalizer

GROUP 8 (1000)				
1	A1	1	SAA7151B	8-bit digital multistandard TV decoder
1	A1	1	SAA7191	Digital multistandard TV decoder
1	A1	1	SAA9051	Digital multistandard colour TV decoder
1	A1	1	SAA9053	Digital NTSC TV decoder
1	A1	1	SAA9056	Digital SECAM colour decoder
1	A1	1	TDA9140	Alignment-free multistandard decoder
1	A1	1	TDA9141	Alignment-free multistandard decoder
1	A1	1	TDA9160	Multistandard decoder/sync. processor
1	A1	1	TDA9162	Multistandard decoder/sync. processor
GROUP 9 (1001)				
1	1	A0	SAA7110	Digital multistandard decoder
A2	A1	A0	PCF8591	4-channel, 8-bit Mux ADC and one DAC
A2	A1	A0	TDA8440	Video/audio switch
A2	A1	A0	TDA8540	4 × 4 video switch matrix
GROUP A (1010)				
0	0	A0	PCF8583	256 × 8-bit RAM/clock/calendar
0	0	1	PCF8593	Low power clock calender
A2	P	P	PCX8598X-2	1024 × 8-bit CMOS EEPROM
A2	A1	A0	PCF8570/C	256 × 8-bit static RAM
A2	A1	A0	PCA8581/C	128 × 8-bit EEPROM
A2	A1	A0	PCF8582/A	256 × 8-bit CMOS EEPROM
A2	A1	P	PCX8594X-2	512 × 8-bit CMOS EEPROM
GROUP B (1011)				
0	0	A0	SAA7199B	Digital multistandard encoder
0	0	1	SAA7152	Digital comb filter
0	1	0	TDA8416	TV/VCR stereo/dual sound processor
1	0	1	PCA8510	Stand-alone OSD circuit
1	0	1	PCA8516	Stand-alone OSD IC
1	A1	0	SAA7186	Digital video scaler
1	1	1	SAA7165	Video enhancement D/A processor
1	1	1	SAA9065	Video enhancement and D/A processor

GROUP C (1100)				
0	0	1	TEA6000	FM/IF and search tuning interface
0	0	1	TEA6100	FM/IF for computer-controlled radio
0	A1	A0	SAB3035	Digital tuning circuit for computer-controlled TV
0	A1	A0	SAB3036	Digital tuning circuit for computer-controlled TV
0	A1	A0	SAB3037	Digital tuning circuit for computer-controlled TV
0	A1	A0	TSA5510	1.2 GHz PLL frequency synthesizer without AFC ADC
0	A1	A0	TSA5511	1.3 GHz PLL frequency synthesizer for TV
0	A1	A0	TSA5512	1.3 GHz PLL frequency synthesizer for TV
0	A1	A0	TSA5514	1.3 GHz PLL frequency synthesizer for TV
0	A1	A0	TSA5519	1.3 GHz PLL frequency synthesizer ADC
0	1	A0	TSA6057	Radio tuning PLL frequency synthesizer
0	1	A0	TSA6060	Radio tuning PLL frequency synthesizer
0	1	A0	TSA6061	150 MHz PLL and IF-counter
0	A1	A0	UMA1009	Frequency synthesizer for mobile telephones
0	A1	A0	UMA1010	Frequency synthesizer for mobile telephones
0	1	A0	UMA1014T	Frequency synthesizer for mobile telephones
GROUP D (1101)				
0	A1	A0	PCF8573	Clock/calendar
1	0	0	TDA1551Q	2 × 22 W BTL audio power amplifier
1	0	1	TDA1551B	2 × 22 W BTL audio power amplifier
1	1	A0	PCD4440	Analog voice scrambler/descrambler for mobile telephones
1	A1	A0	UMA1000T	Data processor for mobile telephones
A2	A1	A0	TDA8443/A	YUV/RGB matrix switch
GROUP E (1110)				
0	0	A0	SAA7192A	Digital colour space-converter
GROUP F (1111)				
X	X	X	–	Reserved addresses

The Group number represents the hexadecimal equivalent of the four most significant bits (A6-A3) of the salve address.

X = Don't care
A = Programmable address bit
P = Page selection bit

Microcontroller bulletin boards

To better serve our customers, Philips maintains two microcontroller bulletin boards. These computer bulletin board systems feature microcontroller newsletters, application and demonstration programs for download, and the ability to send messages to microcontroller application engineers.

The telephone numbers are:

North American Bulletin Board
300/1200/2400 baud 8-N-1
(800) 451-6644 (in the U.S.)
or
(408) 991-2406

European Bulletin Board
MAX 14.400 baud
Standards V32/V42/V42.bis/HST
+31 40 721102

European Application Help Desk
+31 40 722749
9a.m. – 16p.m. CET (Central European Time)

Sunnyvale ROMcode Bulletin Board

We also have a ROM code bulletin board through which you can submit ROM codes. This is a closed bulletin board for security reasons. To get an ID, contact your local sales office. The system can be accessed with a 2400, 1200, or 300 baud modem, and is available 24 hours a day.

The telephone number is:

(408) 991-3459

The following application note files are available on the Philips BBS:

App Note	BBS file name	App Note	BBS file name
AN417	PRN256K.ZIP	AN434	I2CPCKB.ZIP
AN420	INTRUPTS.ASM	AN435	IIC_OS.ZIP
AN422	I2CAPP.ZIP	AN438	I2C528.EXE
AN423	RS751.ASM	AN439	BATTCHRG.C
AN424	WARMBOOT.ZIP	AN440	BOOTSTRP.ZIP
AN425	I2C8584.ZIP	AN443	MAZEMOUS.ZIP
AN427	TIMER1.ZIP	AN445	ABMOUSE.ZIP
AN428	DEMO752.ASM	AN446	DUPUART.ZIP
AN429	AN429.ZIP	AN447	AUTOBAUD.ZIP
AN430	MM751.ZIP	EIE/AN91007	MM751B.ZIP
AN433	SLV751.ZIP	EIE/AN91009	EEPRM851.ZIP

Articles:

Add text overlay to any video display
CCI6.ZIP, MTV.ZIP

80C51 microcontroller family features guide

Part Number (ROMless)		Memory			Counter Timers	I/O Port	Serial Interfaces	External Interrupt	Comments/ Special Features
		ROM	EPRM	RAM					
P	83C750	1K		64	1 (16-bit)	2-3/8	-	2	40 MHz, Lowest cost, SSOP
P	87C750		1K	64	1 (16-bit)	2-3/8	-	2	40 MHz, Lowest cost, SSOP
P	83C748	2K		64	1 (16-bit)	2-3/8	-	2	8XC751 w/o I²C, SSOP
P	87C748		2K	64	1 (16-bit)	2-3/8	-	2	8XC751 w/o I²C, SSOP
S	83C751	2K		64	1 (16-bit)	2-3/8	I²C (bit)	2	24-pin Skinny DIP, SSOP
S	87C751		2K	64	1 (16-bit)	2-3/8	I²C (bit)	2	24-pin Skinny DIP, SSOP
P	83C749	2K		64	1 (16-bit)	2-5/8	-	2	8XC752 w/o I²C, SSOP
P	87C749		2K	64	1 (16-bit)	2-5/8	-	2	8XC752 w/o I²C, SSOP
S	83C752	2K		64	1 (16-bit)	2-5/8	I²C (bit)	2	5 Channel 8-bit A/D, PWM Output, SSOP
S	87C752		2K	64	1 (16-bit)	2-5/8	I²C (bit)	2	5 Channel 8-bit A/D, PWM Output, SSOP
MAx	8051AH (8031AH)	4K		128	2	4	UART	2	NMOS
SC	80C51 (80C31)	4K		128	2	4	UART	2	CMOS (Sunnyvale)
PCx	80C51 (80C31)	4K		128	2	4	UART	2	CMOS (Hamburg)
SC	87C51		4K	128	2	4	UART	2	CMOS
P	80CL51 (80CL31)	4K		128	2	4	UART	10	Low Voltage (1.8V to 6V), Low Power
P	83CL410 (80CL410)	4K		128	2	4	I²C	10	Low Voltage (1.8V to 6V), Low Power
SC	83C451 (80C451)	4K		128	2	7	UART	2	Extended I/O, Processor Bus Interface
SC	87C451		4K	128	2	7	UART	2	Extended I/O, Processor Bus Interface
P	83C550 (80C550)	4K		128	2 + Watchdog	4	UART	2	8 Channel 8-bit A/D
P	87C550		4K	128	2 + Watchdog	4	UART	2	8 Channel 8-bit A/D
P	83C851 (80C851)	4K		128	2	4	UART	2	256B EEPROM, 80C51 Pin compatible
P	83C542	4K		256	2	1	I²C	2	ACCESS.bus, replaces 8042 KB controller
P	87C542		4K	256	2	1	I²C	2	See Above
P	83C852	6K		256	2 (16-bit)	2/8	-	1	Smartcard Controller with 2K EEPROM (Data, Code) Cryptographic Calc Unit
P	83CL580 (80CL580)	6K		256	3 + Watchdog	5	UART, I²C	9	4 Channel 8-bit A/D, PWM Output, Low Voltage (2.5V to 6V), Low Power
MAx	8052AH (8032AH)	8K		256	3	4	UART	2	NMOS
P	80C52 (80C32)	8K		256	3	4	UART	2	80C51 Pin Compatible
P	87C52		8K	256	3	4	UART	2	(see above)
P	83C652 (80C652)	8K		256	2	4	UART, I²C	2	80C51 Pin Compatible
S	87C652		8K	256	2	4	UART, I²C	2	(see above)
P	83C453 (80C453)	8K		256	2	7	UART	2	Extended I/O, Processor Bus Interface
P	87C453		8K	256	2	7	UART	2	Extended I/O, Processor Bus Interface
S	83C51FA (80C51FA)	8K		256	3 + PCA	4	UART	2	Enhanced UART, 3 timers + PCA
S	87C51FA		8K	256	3 + PCA	4	UART	2	Enhanced UART, 3 timers + PCA
S	83L51FA	8K		256	3 + PCA	4	UART	2	Low Voltage 83C51FA (3V @ 20MHz)
S	87L51FA		8K	256	3 + PCA	4	UART	2	Low Voltage OTP 87C51FA (3V @ 20MHz)
P	83C575 (80C575)	8K		256	3 + PCA+ Watchdog	4	UART	2	High Reliability, with Low Voltage Detect, OSC Fail Detect, Analog Comparators, PCA
P	87C575		8K	256	(see above)	4	UART	2	(see above)
P	83C576 (80C576)	8K		256	3 + PCA+ Watchdog	4	UART	2	Same as 8XC575 plus UPI and 10-bit A/D
P	87C576		8K	256	(see above)	4	UART	2	(see above)
PC	83C562 (80C562)	8K		256	3 + Watchdog	6	UART	2	8 Channel 8-bit A/D, 2 PWM Outputs, Capture/Compare Timer
PCx	83C552 (80C552)	8K		256	3 + Watchdog	6	UART, I²C	2	8 Channel 10-bit A/D, 2 PWM Outputs, Capture/Compare Timer
S	87C552		8K	256	3 + Watchdog	6	UART, I²C	2	(see above)

Notes: Part number prefixes are noted in the first column.
All combinations of part type, speed, temperature and package may not be available.

80C51 microcontroller family features guide

Part Number (ROMless)		Program Security?	Clock Freq (MHz)	Temperature Ranges (°C)			Package				
				0 to 70	–40 to +85	–55 to +125	PDIP	CDIP	PLCC	CLCC	PQFP/SSOP
83C750	S	N	3.5 to 40	X	X		N24	F24	A28		DB24 (0–70F)
87C750	S	Y	3.5 to 40	X	X		N24	F24	A28		DB24 (0–70F)
83C748	S	N	3.5 to16	X	X		N24		A28		DB24 (0–70F)
87C748	S	Y	3.5 to16	X	X		N24	F24	A28		DB24 (0–70F)
83C751	S	N	3.5 to16	X	X		N24		A28		DB24 (0–70F)
87C751	S	Y	3.5 to16	X	X		N24	F24	A28		DB24 (0–70F)
83C749	S	N	3.5 to 16	X	X		N28		A28		DB28 (0–70F)
87C749	S	Y	3.5 to 16	X	X		N28	F28	A28		DB28 (0–70F)
83C752	S	N	3.5 to 16	X	X	X	N28		A28		DB28 (0–70F)
87C752	S	Y	3.5 to 16	X	X	X	N28	F28	A28		DB28 (0–70F)
8051AH (8031AH)	S	N	3.5 to 15	X	X		N40		A44		
SC80C51 (80C31)	S	Y	3.5 to 33	X	X	X	N40		A44		B44 (5)
PCx80C51 (80C31)	H	N	1.2 to 30	X	X	X	P (40)		WP (44)		H (44)
87C51	S	Y	3.5 to 33	X	X	X	N40	F40	A44	K44	B44 (5)
80CL51 (80CL31)	Z	N	0 to 16 (1)		X		N40 (2)				B44
83CL410(80CL410)	Z	N	0 to 12 (1)		X		N40 (2)				B44
83C451 (80C451)	S	N	3.5 to 16	X	X	X	N64 (4)		A68		
87C451	S	Y	3.5 to16	X	X	X	N64 (4)		A68		
83C550 (80C550)	S	Y	3.5 to 16	X	X		N40		A44		
87C550	S	Y	3.5 to 16	X	X	–40 to +125	N40	F40	A44	K44	
83C851 (80C851)	H	Y	1.2 to 16	X	X		N40		A44		B44
83C542	S	Y	3.5 to 16	X					A44		
87C542	S	Y	3.5 to 16	X					A44	K44	
83C852	H	Y	1 to 12	X			SO28 or die				
83CL580 (80CL580)	Z	N	0 to 12 (1)		X		(3)				B64
8052AH (8032AH)	S	N	3.5 to 15	X	X		N40		A44		
80C52 (80C32)	S	Y	3.5 to 24	X	X		N40		A44		B44 (5)
87C52	S	Y	3.5 to 24	X	X	X	N40	F40	A44	K44	B44 (5)
83C652 (80C652)	H	Y	1.2 to 24	X	X	–40 to +125	N40		A44		B44
87C652	S	Y	1.2 to 20	X	X	X	N40	F40	A44	K44	
83C453 (80C453)	S	N	3.5 to 16	X	X				A68		
87C453	S	Y	3.5 to16	X	X				A68		
83C51FA (80C51FA)	S	Y	3.5 to 24	X	X		N40		A44		B44
87C51FA	S	Y	3.5 to 24	X	X		N40	F40	A44	K44	B44
83L51FA	S	Y	3.5 to 20	X	X		N40		A44		B44
87L51FA	S	Y	3.5 to 20	X	X		N40	F40	A44	K44	B44
83C575 (80C575)	S	Y	4 to 16	X		X	N40		A44		B44
87C575	S	Y	4 to 16	X		X	N40	F40	A44	K44	B44
83C576 (80C576)	S	Y	4 to 16	X		X	N40		A44		B44
87C576	S	Y	4 to 16	X		X	N40	F40	A44	K44	B44
83C562 (80C562)	H	N	1.2 to 16	X	X	–40 to +125			A68		B80
83C552 (80C552)	H	N	1.2 to 30	X	X	–40 to +125			A68		B80
87C552	S	Y	1.2 to 16	X					A68	K68	

Notes: Production Centers are indicated in the second column: H – Hamburg, S – Sunnyvale, Z – Zurich.
All combinations of part type, speed, temperature and package may not be available.
1) Oscillator options start from 32kHz.
2) Also available in VSO40 package.
3) Also available in VSO56 Package.
4) Not recommended for new design.
5) Package available up to 16 MHz only.

80C51 microcontroller family features guide

Part Number (ROMless)		Memory			Counter Timers	I/O Port	Serial Interfaces	External Interrupt	Comments/ Special Features
		ROM	EPRM	RAM					
P	83CL267	12K		256	3	2 5/8	I²C	–	OSD, 8 PWM Outputs, 3 Software A/D Inputs, 8 LED Drivers
P	83CL268	12K		256	3	2 5/8	I²C, 1M Baud	–	(see above)
P	83C055	16K		256	2 (16-bit)	3 1/2	–	2	On-Screen Display, 9 PWM Outputs, 3 Software A/D Inputs
P	87C055		16K	256	2 (16-bit)	3 1/2	–	2	(see above)
P	80C54	16K		256	3	4	UART	2	Standard; 80C51 compatible
P	87C54		16K	256	3	4	UART	2	Standard; 87C51 compatible
P	83C504 (80C504)	16K		256	2	4	UART	2	'654 with Hardware Divide (no I²C)
P	87C504		16K	256	2	4	UART	2	(see above)
P	83C654	16K		256	2	4	UART, I²C	2	80C51 Pin Compatible
S	87C654		16K	256	2	4	UART, I²C	2	(see above)
P	83CE654	16K		256	2	4	UART, I²C	2	83C654 with Reduced EMI
P	83CL781	16K		256	3	4	UART, I²C	10	Low Voltage (1.8V to 6V), Low Power
P	83CL782	16K		256	3	4	UART, I²C	10	83CL781 Optimized 12MHz @ 3.1V
S	83C51FB	16K		256	3 + PCA	4	UART	2	Enhanced UART, 3 timers + PCA
S	87C51FB		16K	256	3 + PCA	4	UART	2	Enhanced UART, 3 timers + PCA
S	83L51FB	16K		256	3 + PCA	4	UART	2	Low Voltage 83C51FB (3V @ 20MHz)
S	87L51FB		16K	256	3 + PCA	4	UART	2	Low Voltage OTP 87C51FB (3V @ 20MHz)
P	83CL167	16K		256	3	6 1/8	I²C	–	OSD, 8 PWM Outputs, 4 Software A/D Inputs, 8 LED Drivers
P	83CL168	16K		256	3	6 1/8	I²C, 1M Baud	–	(see above)
P	83C524	16K		512	3 + Watchdog	4	UART, I²C-bit	2	512 RAM
P	87C524		16K	512	3 + Watchdog	4	UART, I²C-bit	2	512 RAM
P	83C592 (80C592)	16K		512	3 + Watchdog	6	UART, CAN	6	CAN Bus Controller with 8 x 10-bit A/D, 2 PWM outputs, Capture/Compare Timer
P	87C592		16K	512	3 + Watchdog	6	UART, CAN	6	(see above)
P	80C58	32K		256	3	4	UART	2	Standard; 80C51 compatible
P	87C58		32K	256	3	4	UART	2	Standard; 87C51 compatible
S	83C51FC	32K		256	3 + PCA	4	UART	2	Enhanced UART, 3 timers + PCA
S	87C51FC		32K	256	3 + PCA	4	UART	2	Enhanced UART, 3 timers + PCA
P	83C528 (80C528)	32K		512	3 + Watchdog	4	UART, I²C-bit	2	Large Memory for High Level Languages
P	87C528		32K	512	3 + Watchdog	4	UART, I²C-bit	2	Large Memory for High Level Languages
P	83CE528 (80CE528)	32K		512	3 + Watchdog	4	UART, I²C-bit	2	8XC528 with Reduced EMI
P	83CE598 (80CE598)	32K		512	3 + Watchdog	6	UART, CAN	6	CAN Bus Controller, 8 x 10-bit A/D, 2 PWM outputs, WD, T2, Reduced EMI
P	87CE598		32K	512	3 + Watchdog	6	UART, CAN	6	(see above)
P	83CE558(80CE558)	32K		1024	3 + Watchdog	6	UART, I²C	2	Low EMI, 8 Channel 10-bit A/D, 2 PWM Outputs, Capture/Compare Timer
P	89CE558		32K	1024	3 + Watchdog	6	UART, I²C	2	32K FLash EEPROM plus above

Notes: Part number prefixes are noted in the first column.
All combinations of part type, speed, temperature and package may not be available.

80C51 microcontroller family features guide

Part Number (ROMless)		Program Security?	Clock Freq (MHz)	Temperature Ranges (°C)			Package				
				0 to 70	–40 to +85	–55 to +125	PDIP	CDIP	PLCC	CLCC	PQFP/SSOP
83CL267	T	N	4.0 to 12	X			R42				B64
83CL268	T	N	4.0 to 12	X			R42				B64
83C055	S	N	3.5 to 20	X			NB42				
87C055	S	N	3.5 to 20	X			NB42				
80C54	S	Y	3.5 to 24	X	X		N40		A44		B44
87C54	S	Y	3.5 to 24	X	X		N40	F40	A44	K44	B44
83C504 (80C504)	S	Y	1.2 to 20	X	X	X	N40		A44		B44
87C504	S	Y	1.2 to 20	X	X	X	N40	F40	A44	K44	B44
83C654 (80C654)	H	Y	1.2 to 24	X	X	–40 to +125	R42, N40		A44		B44
87C654	S	Y	1.2 to 20	X	X	X	N40	F40	A44	K44	B44
83CE654	H	Y	1.2 to 16	X	X						B44
83CL781	Z	N	0 to 12 (1)		X		N40				B44
83CL782	Z	N	0 to 12 (1)		–25 to +55		N40				B44
83C51FB	S	Y	3.5 to 24	X	X		N40		A44		B44
87C51FB	S	Y	3.5 to 24	X	X		N40	F40	A44	K44	B44
83L51FB	S	Y	3.5 to 20	X			N40		A44		B44
87L51FB	S	Y	3.5 to 20	X			N40	F40	A44	K44	B44
83CL167	T	N	4.0 to 12	X			R42				B64
83CL168	T	N	4.0 to 12	X			R42				B64
83C524	H	Y	1.2 to 16	X	X		N40		A44		B44
87C524	S	Y	3.5 to 20	X	X		N40	F40	A44	K44	B44
83C592 (80C592)	H	Y	1.2 to 16		X	–40 to +125			A68	K68	
87C592	H	Y	1.2 to 16	X			R42		A68	K68	
80C58	S	Y	3.5 to 16	X	X		N40		A44		B44
87C58	S	Y	3.5 to 16	X	X		N40	F40	A44	K44	B44
83C51FC	S	Y	3.5 to 24	X	X		N40		A44		B44
87C51FC	S	Y	3.5 to 24	X	X		N40	F40	A44	K44	B44
83C528 (80C528)	H	Y	1.2 to 16	X	X	–40 to +125	N40		A44		B44
87C528	S	Y	3.5 to 20	X	X		N40	F40	A44	K44	B44
83CE528 (80CE528)	H	Y	1.2 to 16	X	X	–40 to +125			A44		B44
83CE598 (80CE598)	H	Y	1.2 to 16		X	–40 to +125					B80
87CE598	H	Y	3.5 to 16	X	X						B80
83CE558 80CE558	H	Y	1.2 to 16	X	X	–40 to +125					B80
89CE558	H	Y	1.2 to 16	X	X					Q80	B80

Notes: Production Centers are indicated in the second column: H – Hamburg, S – Sunnyvale, Z – Zurich.
All combinations of part type, speed, temperature and package may not be available.
1) Oscillator options start from 32kHz.
2) Also available in VSO40 package.
3) Also available in VSO56 Package.
4) Not recommended for new design.
5) Package available up to 16 MHz only.

CMOS and NMOS 8-bit microcontroller family

80C51 FAMILY CMOS

TYPE	ROM/ EPROM	RAM	SPEED (MHz)	PACKAGE	FUNCTIONS	REMARKS	PHILIPS PROBES	THIRD PARTY PODs
80C31 80C51 87C51	0 4k ROM 4k EPROM	128 128 128	33 33 33	 DIL40, LCC44 QFP44	UART, 2 timers	87C51:QFP package up to 16MHz	OM1092 + OM1097 (16MHz) OM4120S	8052PC(M) POD-C51B(N)
83C51FA 87C51FA	8k ROM 8k EPROM	256 256	24 24	DIL40, LCC44 QFP44	Enhanced UART, 3 timers, PCA		PDS51FBSD	8351FX(M) POD-C51FX(N)
83L51FA 87L51FA	8k ROM 8k EPROM	256 256	20 20	DIL40, LCC44 QFP44	Enhanced UART, 3 timers, PCA	3V to 4.5V operation		POD-L51P(N)
87C51FB 83C51FB	16k ROM 16k EPROM	256 256	24 24	DIL40, LCC44 QFP44	Enhanced UART, 3 timers, PCA		PDS51FBSD	8351FX(M) POD-C51FX(N)
87L51FB 83L51FB	16k ROM 16k EPROM	256 256	20 20	DIL40, LCC44 QFP44	Enhanced UART, 3 timers, PCA	3V to 4.5V operation		POD-L51P(N)
87C51FC 83C51FC	32k ROM 32k EPROM	256 256	24 24	DIL40, LCC44 QFP44	Enhanced UART, 3 timers, PCA			8351FX(M) POD-C51FX(N)
80C32 80C52 87C52	0 8k ROM 8k EPROM	256 256 256	24 24 24	DIL40, LCC44 QFP44	UART, 3 timers		OM1079 OM5012	8052PC(M) POD-C32(N)
80C54 87C54	16k ROM 16k EPROM	256 256	24 24	DIL40, LCC44 QFP44	UART, 3 timers		OM1079 OM5012	8052PC(M) POD-C32(N)
80C58 87C58	32k ROM 32k EPROM	256 256	24 24	DIL40, LCC44 QFP44	UART, 3 timers		OM1079 OM5012	8052PC(M) POD-C32(N)
80C451 83C451 87C451	0 4k ROM 4k EPROM	128 128 128	16 16 16	 DIP64/LCC68	UART, 2 timers Extended I/O		OM4123	83C451PC(M) POD-C451B(N)
83C504 87C504	16K ROM 16K EPROM	256 256	24 24	DIL40, LCC44 QFP44	24 by 8 divide, 2 timers			
87C524 83C524	16K EPROM 16k ROM	512 512	20 12	DIL40/LCC44 QFP44	UART, 3 timers Watchdog timer Bit I^2C		OM4111 + OM4110 + OM4120S	83528PC(M) POD-C528(N)
83C528 87C528 83CE528	32k ROM 32k EPROM 32kROM	512 512 512	16 16, 20 16	DIL40/LCC44 (QFP44) CE ONLY QFP	UART, 3 timers Watchdog timer Bit I^2C		OM4111 + OM4110 + OM4120S	83C528PC(M) POD-C528(N)
80C550 83C550 87C550	0 4k ROM 4k EPROM	128 128 128	16 16 16	LCC44 DIL40	UART, 2 timers 8 8-bit ADC inputs, watchdog timer		OM5055 + OM4110	83550(M) POD-C550(N)
80C552 83C552 87C552	0 8k ROM 8k EPROM	256 256 256	16, 24 16, 24 16	LCC68/QFP80	UART, 2 timers Timer with compare and capture, 2 PWM outputs, 8 10-bit ADC inputs, Byte I2C		OM1092 + OM1095 + OM4120S OM4128	83C552PC(M) POD–C552B(N)
83CE558 89CE558 80CE558	32K ROM 32K FLASH 0	1K 1K	16 16	QFP80	As 8xC552 with PLL-oscillator Auto scan ADC	89C: Q4-92 83C: Q2/3-93	OM4247	
80C562 83C562	0 8k ROM	256 256	16 16	LCC68/QFP80	UART, 2 timers Timer with compare and capture, 2 PWM outputs, 8 8-bit ADC inputs		OM1092 + OM1095 + OM4120S	83C552PC(M) POD-C552B(N)
80C575 83C575 87C575	0 8k 8k EPROM	256 256 256	16 16 16	DIL40, LCC44 QFP44	3 timers 1 Enh. UART, PCA, 4 analog comparators			POD-C575(N)
83C576 87C576	8k ROM 8k EPROM	256 256	16 16	DIL40, LCC44, SDIL42	10-bit A/D, 3 timers, PCA, Watchdog timer			
80C592 83C592 87C592	0 16k ROM 16k EPROM	512 512 512	16 16 16	LCC68/QFP80	8XC552 + CAN interface		OM4110 + OM4112 + OM4120S	POD-592(N)

M = Metlink
N = Nohau

80C51 FAMILY CMOS (Continued)

TYPE	ROM/ EPROM	RAM	SPEED (MHz)	PACKAGE	FUNCTIONS	REMARKS	PHILIPS PROBES	THIRD PARTY PODs
87CE598 87CE598 80CE598	32K ROM 32K EPROM 0	512 512 512	16 16 16	QFP80	8xC552 + CAN interface. No I^2C	87CE: prod: Q2'94		
80C652 83C652 87C652	0 8k ROM 8k EPROM	256 256 256	16, 24 16, 24 16, 20	DIL40/LCC44 QFP44	UART, 2 timers Byte I^2C		OM1092 + OM1096 + OM4120S	83652PC(M) POD-C51B(N)
83C654 87C654	16k ROM 16k EPROM	256 256	16,24 16,20	DIL40/LCC44 QFP44	UART, 2 timers Byte I^2C		OM1092 + OM1096 + OM4120S	83654(M) POD-C51B(N)
83CE654 80CE654	16k ROM 0	256 256	16 16	QFP44	UART, 2 timers Byte I^2C	83C654 with Electromagnetic Compatibility improvements	OM1092 + OM1096 + OM4120S	83654(M) POD-C51B(N)
83C750 87C750	1K ROM 1KEPROM	64 64	40 40	SDIP24 skinny	1 timer		OM1094	83751PC(M)
83C751 83C748 87C751 87c748	2k ROM 2k EPROM	64 64	16 16	DIP24 skinny LCC28 DIP24 skinny	1 timer Bit I^2C (8XC751 only)		OM1094P	83751PC(M) POD-C751(N)
83C752 83C749 87C752 87c752	2k ROM 2k EPROM	64 64	16 16	DIP28, LCC28 DIP 28, LCC28	1 timer, PWM output, 5 8-bit ADC inputs, Bit I^2C (8XC752 only)		OM5072	83752A(M) POD-C752(N)
80C851 83C851	0 4k ROM	128 128	16 16	DIL40/LCC44 QFP44	UART, 2 timers 256 byte		OM1092 + OM4120S	80851PC(M) POD-C51(N)
83C852	6k ROM	256	6		2k byte EEPROM smart card hardware CU			
83C055 87C055	16k ROM 16k EPROM	256 256	12 12	DIP42 Shrunk DIP42 Shrunk	As 8XC053	In dev.	OM5054	

* The following microcontollers have no external memory access: 8XC751, 8XC752, 8XC053, 87C054, 83C852.
M = Metlink
N = Nohau

80CLXXX FAMILY CMOS

TYPE	ROM	RAM	SPEED (MHz)	PACKAGE	FUNCTIONS	REMARKS	PROBE SDS	REMARKS
85CL000	0	256	12	Piggyback	Piggyback CL410, CL411, CL51, P80C51			
85CL580	0	256	12	Piggyback	Piggyback CL580			
85CL781	0	256	12	Piggyback	Piggyback CL781, CL782, CL52			
80CL51 80CL31	4K 0	128 128	16 16	DIL40 VSO40	2 timers, UART		OM1079	QFP: OM5020
83CL410 80CL410	4k 0	128 128	12 12	DIL40 VSO40	2 timers Byte I^2C		OM1079	QFP: OM5020
83CL580	6k	256	16	QFP64/ VSO56	3timers, UART Watchdog timer Byte I^2C, 1 PWM 4*8 bit ADC		OM1079 + OM5004	OM1079: Probe base OM5004: Probe adap
83CL781 83CL782	16k 16k	256 256	12 @ 4.5V 12 @ 3V	DIL40 QFP44	3timers, UART Byte I^2C		OM1079 + OM5004 + tbd	OM1079: Probe base OM5004: Probe adap
83CL167 83CL267	16K 12K	256 256	12 12	SDIL64 QFP64	3timers 1-14 bit PWM 4-6 bit PWM 4-7 bit PWM 4*4 bit ADC Byte I^2C 160 char OSD 126 char fonts 4 char sizes Shadow modes ODS PLL osc. 10MHz Blinking	In Dev	OM4840 OM1079	
83CL168 83CL268	16K 12K	256 256	12 12	SDIL64 QFP64	3timers 1-14 bit PWM 4-6 bit PWM 4-7 bit PWM 4*4 bit ADC RC preprocessor Byte I^2C 3 wire serial I/O 160 char OSD 126 char fonts 4 char sizes Shadow modes ODS PLL osc. 10MHz Blinking	In Dev	OM4840 + OM1079	

8051 FAMILY NMOS

TYPE	ROM	RAM	SPEED (MHz)	PACKAGE	FUNCTIONS	REMARKS	PROBE SDS	THIRD PARTY EMULATOR
8051 8031	4k 0	128 128	15 15	DIL40/PLCC44 DIL40/PLCC44	UART, 2 timers		OM1092 + OM1097 + OM4120S	8052PC(M) OPD-C51B(N)
8052 8032	8k 0	256 256	15 15	DIL40/PLCC44 DIL40/PLCC44	UART, 3 timers UART, 3 timers		OM4111 + OM4110 + OM4120S	8052PC(M) OPD-C51B(N)

CMOS and NMOS 8-bit microcontroller family

8400 FAMILY CMOS

TYPE	ROM	RAM	SPEED (MHz)	PACKAGE	FUNCTIONS	REMARKS	PROBE SDS	REMARKS
84C21A 84C41A 84C81A	2k 4k 8k	64 128 256	10 10 10	DIL28/SO28 DIL28/SO28 DIL28/SO28	20 I/O lines 8-bit timer Byte I^2C		OM1083	OM1025 (LSDS)
84C22A 84C42A 84C12A	2k 4k 1k	64 64 64	10 10 16	DIL20/SO20 DIL20/SO20 DIL20/SO20 DIL20/SO20	13 I/O lines 8-bit timer		OM1083 + Adapter_1	OM1025 (LSDS)
84C00B 84C00T	0 0	256 256	10 10	28 pins VSO-56	20 I/O lines 8-bit timer Byte I^2C	Piggyback ROMless	OM1080 OM1080	
84C121 84C121B	1k 0	64 64	10 10	DIL20/SO20	13 I/O lines 2 8-bit timers 8 bytes EEPROM	 Piggyback	OM1073	OM1025(LEDS) OM1027
84C122A 84C122B 84C422A 84C422B 84C822A 84C822B 84C822C	1k 4K 8K	32 32 32	10	A: SO20 B: SO24 C: SO28	Controller for remote control A: 12 I/O B: 16 I/O C: 20 I/O		OM4830	
84C230	2I	64	10	DIL40/VSO40	12 I/O lines 8-bit timer 16*4 LCD drive		OM1072	
84C430 84C430BH	4k 0	128 128	10 10	QFP64	24 I/O lines 8-bit timer Byte I^2C 24*4 LCD drive	 Piggyback for C230 and C430	OM1072	
84C633 84C633B	6k 0	256 256	16 16	VSO56	28 I/O lines 8-bit timer 16-bit up/down counter 16-bit timer with compare and capture 16*4 LCD drive		OM1086	
84C440 84C441 84C443 84C444 84C640 84C641 84C643 84C644 84C840 84C841 84C843 84C844	4k 4k 4k 4k 6k 6k 6k 6k 8k 8k 8k 8k	128 128 128 128 128 128 128 128 192 192 192 192	10 10 10 10 10 10 10 10 10 10 10 10	DIP42 shrunk	RC: 29 I/O lines LC: 28 I/O lines 8-bit timer 1 14-bit PWM 5 6-bit PWM 3-bit ADC OSD 2L-16	I^2C, RC I^2C, LC RC LC I^2C, RC I^2C, LC RC LC I^2C, RC I^2C, LC RC LC	OM1074	For emulation of LC versions, use OM1074 + adapter_3 + 2 adapter_5 Baud for LCDS OM4831

CMOS and NMOS 8-bit microcontroller family

8400 FAMILY CMOS (Continued)

TYPE	ROM	RAM	SPEED (MHz)	PACKAGE	FUNCTIONS	REMARKS	PROBE SDS	REMARKS
84C646 84C846	6k 8k	192 192	10 10	DIP42 shrunk	30 I/O lines DOS clock = PLL 8 bit timer 1-14 bit PWM 4-6 bit PWM 4-7 bit PWM 3-4 bit ADC DOS: 64 disp. RAM 62 char. fonts Char. blinking Shadow modes 8 foreground colors/char. 8 background colors/word DOS: clock: 8 . . 20MHz	I^2C, RC I^2C, RC	OM4829 + OM4832	OM4833 for LCD584
84C85 84C85B	8k 0	256 256	10 10	DIL40/VSO40	32 I/O lines 8-bit timer Byte I^2C	 Piggyback for C85	OM1070	
84C853 84C853B	8k 0	256 256	16 16	DIL40/VSO40	33 I/O lines 8-bit timer 16-bit up/down counter 16-bit timer with compare and capture	 Piggyback for C853	OM1081	
84C270 84C470 84C270B 84C470B	2k 4k 0 0	128 128 128 128	10 10 10 10	DIL40/VSO40 DIL40/VSO40	8 I/O lines 16*8 capture keyboard matrix 8-bit timer 470 also handles mech. keys	 Piggyback for C270 Piggyback for C470	OM1077	
84C271	2k	128	10	DIL40	8 I/O lines 16*8 mech. keyboard matrix 8-bit timer		OM1078	

8400 FAMILY NMOS

TYPE	ROM	RAM	SPEED (MHz)	PACKAGE	FUNCTIONS	REMARKS	EMULATOR TOOLS	REMARKS
8411 8421 8441 8461	1k 2k 4k 6k	64 64 128 128	6 6 6 6	DIL28/SO28 DIL28/SO28 DIL28/SO28 DIL28/SO28	20 I/O lines 8-bit timer Byte I^2C			OM1025 (LCDS) + OM1026
8422 8442	2k 4k	64 128	6 6	DIL20 DIL20	13 I/O lines 8-bit timer Bit I^2C			
8401B	0	128	6	28-pin		Piggyback for 84X1		

3300 FAMILY CMOS

TYPE	ROM	RAM	SPEED (MHz)	PACKAGE	FUNCTIONS	REMARKS	PROBE SDS	REMARKS
3315A	1.5k	160	10	DIL28/SO28	20 I/O lines 8-bit timer V_{DD} > 1.8V		OM1083	OM1025(LCDS)
3343	3k	224	10	DIL28/SO28	20 I/O lines 8-bit timer V_{DD} > 1.8V Byte I^2C		OM1083	OM1025(LCDS)
3344A	2k	224	3.58	DIL28/SO28	20 I/O lines 8-bit timer DTMF generator		OM1071	OM1025(LCDS) + OM1028
3346A	4k	128	10	DIL28/SO28	20 I/O lines 8-bit timer Byte I^2C 256 bytes EEPROM V_{DD} < 1.8V		OM1076	
3347	1.5k	64	3.58	DIL20/SO20	12 I/O lines 8-bit timer DTMF generator		OM1071 + Adapter_2	OM1025(LCDS) + OM1028
3348A	8k	256	10	DIL28/SO28	20 I/O lines 8-bit timer Byte I^2C V_{DD} < 1.8V		OM1083	OM1025(LCDS)
3349A	4k	224	3.58	DIL28/SO28	20 I/O lines 8-bit timer DTMF generator		OM1071	OM1025(LCDS) + OM1028
3350A	8k	128	3.58	VSO64	30 I/O lines 8-bit timer DTMF generator 256 bytes EEPROM			
3351A	2k	64	3.58	DIL28/SO28	20 I/O lines 8-bit timer DTMF generator 128 bytes EEPROM		OM5000	
3352A	6k	128	3.58	DIL28/SO28	20 I/O lines 8-bit timer DTMF generator 128 byte EEPROM		OM5000	
3353A	6k	128	16	DIL28/SO28	20 I/O lines 8-bit timer DTMF generator Ringer out 128 bytes EEPROM	March '92	OM5000	
3354A	8k	256	16	QFP64	36 I/O lines 8-bit timer DTMF generator Ringer out 256 bytes EEPROM	June '92	OM4829 + OM5003	OM4829: Probe base
8755A	0	128	16	DIL28/SO28	8k OTP 20 I/O lines 8-bit timer DTMF generator Melody output 128 bytes EEPROM	In Development		
3301B						Piggyback for 3315, 3343, 3348	OM1083	
3344B						Piggyback for 3344, 3347, 3349	OM1071	
3346B						Piggyback for 3346	OM1076	

3300 FAMILY CMOS (Continued)

TYPE	ROM	RAM	SPEED (MHz)	PACKAGE	FUNCTIONS	REMARKS	PROBE SDS	REMARKS
3350B						Piggyback for 3350A	OM4829+ OM5003	
3351B						Piggyback for 3351A, 3352A, 3353A	OM5000	
3354B						Piggyback for 3354A	OM4829+ OM5010	

CMOS 16-bit microcontroller family

16-BIT CONTROLLERS (68000 ARCHITECTURE)

TYPE	(EP)ROM	RAM	SPEED (MHz)	FUNCTIONS	REMARKS	PHILIPS TOOLS	THIRD-PARTY TOOLS
68070	–	–	17.5	2 DMA channels, MMU, UART, 16-bit timer, I^2C, 68000 bus interface, 16Mb address range		OM4160 Microcore 1 OM4160/2 Microcore 2 OM4161 (SBE68070) OM4767/2 XRAY68070SBE high level symbolic debugger OM4222 68070DS development system OM4226 XRAY68070DS high level symbolic debugger	TRACE32-ICE68070 (Lauterbach)
93C101	34k	512	15	Derivative with low power modes	Not for new design		
90CE201	16MB external ROM	16MB external RAM	24	UART, fast I^2C, 3 timers (16 bit), Watchdog timer. 68000 software compatible, EMC, QFP64	–25 to +85°C	OM4162 Microcore 4	TRACE32 – (Lauterbach)

16-BIT CONTROLLERS (XA ARCHITECTURE)

TYPE	(EP)ROM	RAM	SPEED (MHz)	FUNCTIONS	REMARKS	DEVELOPMENT TOOLS
XA-G1	8k	512	30	3 timers, watchdog, 2 UARTs	–40 to +125°C	Nohau Ceibo MacCraiger Systems
XA-G2	16k	512	30	3 timers, watchdog, 2 UARTs	–40 to +125°C	Nohau Ceibo MacCraiger Systems
XA-G3	32k	512	30	3 timers, watchdog, 2 UARTs	–40 to +125°C	Nohau Ceibo MacCraiger Systems

TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

BASIC TYPE NUMBER

This type designation code applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick film and hybrid integrated circuits. The basic type number comprises three letters followed by a serial number.

First and second letters

DIGITAL FAMILY CIRCUITS

The first two letters identify the family.(1)

SOLITARY CIRCUITS

The first letter divides solitary circuits into:

S Solitary digital circuits

T Analog circuits

U Mixed analog/digital circuits.

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits.(2)

MICROPROCESSORS

The first two letters identify microprocessors and related circuits:

MA Microcomputer or central processing unit

MB Slice processor (functional slice of microprocessor)

MD Related memories

ME Other related circuits such as interfaces, clocks, peripheral controllers, etc.

CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

The first two letters identify:

NH Hybrid circuits

NL Logic circuits

NM Memories

NS Analog signal processing using switched capacitors

NT Analog signal processing using charge-transfer devices

NX Imaging devices

NY Other related circuits.

(1) A logic family is an assembly of digital circuits designed to be interconnected and defined by its base electrical characteristics, such as supply voltage, power consumption, propagation delay, noise immunity.

(2) The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added, for example, SH for bubble memories.

Third letter

The third letter indicates the operating ambient temperature range:

A temperature range not specified below

B 0 to +70 °C

C −55 to +125 °C

D −25 to +70 °C

E −25 to +85 °C

F −40 to +85 °C

G −55 to +85 °C.

If a device has another temperature range, the letter 'A' or a letter indicating a narrower temperature may be used, for example, the range of 0 to +75 °C can be indicated by 'A' or 'B'. Should two devices with the same basic type number both have temperature ranges other than those specified, one would use the letter 'A' and the other the letter 'X'.

SERIAL NUMBER

This may be a four-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

VERSION LETTER

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. The version letter has no fixed meaning except for 'Z' which means customized wiring. The following letters are recommended for package variants:

C Cylindrical

D Ceramic dual in-line (CERDIL, CERDIP)

F Flat pack (two leads)

G Flat pack (four leads)

H Quad flat pack (QFP)

L Chip on tape (foil)

P Plastic dual in-line (DIL)

Q Quad in-line (QUIL)

T Mini pack (SOL, SO, VSO)

U Uncased chip.

TWO-LETTER SUFFIX

A two-letter suffix may be used instead of a single package version letter to give more information. To avoid confusion with serial numbers that end with a letter, a hyphen should precede the suffix.

First letter (general shape)

C Cylindrical
D Dual in-line (DIL)
E Power DIL (with external heatsink)
F Flat pack (leads on two sides)
G Flat pack (leads on four sides)
H Quad flat pack (QFP)
K Diamond (TO-3 family)
M Multiple in-line (except dual, triple and quad)
Q Quad in-line (QUIL)
R Power QUIL (with external heatsink)
S Single in-line (SIL)
T Triple in-line
W Leaded chip carrier (LCC)
X Leadless chip carrier (LLCC)
Y Pin grid array (PGA).

Second letter (material)

C Metal-ceramic
G Glass-ceramic
M Metal
P Plastic.

EXAMPLES

PCF1105WP: digital IC; PC family; operating temperature range −40 to +85 °C; serial number 1105; plastic leaded chip carrier.

GMB74LS00A-DC: digital IC; GM family; operating temperature range 0 to +70 °C; company number 74LS00A; ceramic DIL package.

TDA1000P: analog IC; operating temperature range non-standard; serial number 1000; plastic DIL package.

SAC2000: solitary digital circuit; operating temperature range −55 to +125 °C; serial number 2000.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor.
- All mains-powered electrical equipment should be connected via an earth leakage switch.
- Equipment cases should be earthed.
- Relative humidity should be maintained between 50 and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.

RECEIPT AND STORAGE

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

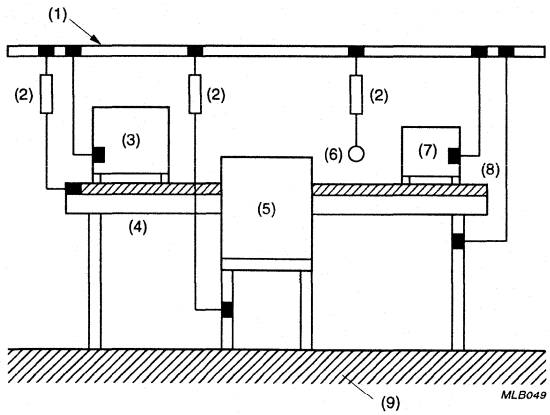
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.
(9) Antistatic floor.

Fig.1 Protected work station.

I²C SPECIFIC INFORMATION

APPLICATIONS NOTES

The following abstracts are of the application notes that can be found printed in-full in Philips Semiconductor's Data Handbook "Application Notes and Development Tools for 80C51 Microcontrollers", ordering code 9397 750 00013.

AN422 – Using the 8XC751 microcontroller as an I²C-bus master

The 83C751/87C751 combines the benefits of a high-performance microcontroller with on-board hardware supporting the I²C-bus interface, and thus allows systems to be completely software defined. This article shows how best to connect the microcontroller to an I²C-bus configuration, describes the 8XC751 I²C hardware and gives a programming example demonstrating a bus-master code.

AN425 – Interfacing the PCD8584 I²C-bus controller to 80C51 family microcontrollers

This application note describes how to use the PCD8584 I²C-bus controller with the 80C51 family of microcontrollers. A typical way of connecting the PCD8584 to an 80C31 is given, and some basic software routines are described showing how to transmit and receive bytes in a single master system. There is also an example of how to use these routines in an application that uses the I²C circuits on an I²C demonstration board.

AN430 – Using the 8XC751/752 in multimaster I²C applications

This article discusses the most important technical features of the I²C-bus and describes the special I²C hardware interface of the 8XC751/752. The author gives an example of how the microcontroller can be programmed for a multimaster environment along with details of the software interface for the communications routes.

AN433 – I²C slave routines for the 83C751

The 8XC751 microcontroller can be programmed as an I²C-bus master, slave, or both. This article focuses on its use as a slave and gives a programming example demonstrating the communications routes of the 8XC751 as a slave on the I²C-bus. This example complements the program given in article AN422.

AN434 – Connecting a PC keyboard to the I²C-bus

This application note illustrates the use of the 8XC751 microcontroller to interface a standard PC/AT keyboard to the I²C bus. The application software example easily fits within the 2K-bytes code and 64-bytes data memory provided on the 8XC751.

AN438 – I²C routines for 8XC528

This article presents a set of software routines to drive the I²C interface in 8XC528-type microcontrollers. A description of the I²C interface is given along with examples of how to use these routines in PL/M-51, C and assembly source code.

AN444 – Using the P82B715 I²C extender on long cables

The P82B715 I²C buffer was designed to extend the range of the logical I²C-bus out to 50 m. This application note describes the results of testing the buffer on several different types of cables to determine the maximum operating distance possible. The results are summarized in a table for easy reference.

ETV/AN89004 – PLM51 I²C software interface IIC51 (version 0.5)

This document is a user manual for the I²C software module IIC51, and is intended for Intel PLM51 users who need to control an I²C-bus. There is a general description on the IIC51 software module, although some basic knowledge about I²C and Intel PLM51 is assumed.

EIE/AN91007 – I²C driver routines for 8XC751/1 microcontrollers

This report described the I²C drivers that are written for the 8XC751/2 and explains the structure of the software and how to use the routines. The software is written around a set of basic routines and a message handler. The message handles contain no specific 8XC751 code so, by rewriting a set of basic routines, the software example can easily be modified for any other bit level I²C interface .

Programming the I²C interface

This article is taken from Dr. Dobb's Journal and gives a good overview of I²C-bus basics. It describes hardware requirements, building a framework and how to connect to the I²C-bus.

I²C Specific information — Application notes

The following application note is printed separately. The full version can be ordered from Philips Semiconductors.

AN94078 – P90CL301 I²C DRIVER ROUTINES

This application note shows how to write an I²C-bus driver for the Philips P90CL301 microcontroller and includes a set of application interface software routines to quickly implement a complete I²C multimaster system application.

The driver allows you to link modules to your application software and includes a head-file into the application source programs. A programming example on how to use the driver is also listed in the article.

The driver supports polled or interrupt driven message handling, slave message transfer and multimaster system applications. It is also suitable for use in conjunction with real-time operating systems such as pSOS+.

The I²C-bus and how to use it

(including specifications)

1.0 THE I²C-BUS BENEFITS DESIGNERS AND MANUFACTURERS

In consumer electronics, telecommunications and industrial electronics, there are often many similarities between seemingly unrelated designs. For example, nearly every system includes:

- Some intelligent control, usually a single-chip microcontroller
- General-purpose circuits like LCD drivers, remote I/O ports, RAM, EEPROM, or data converters
- Application-oriented circuits such as digital tuning and signal processing circuits for radio and video systems, or DTMF generators for telephones with tone dialling.

To exploit these similarities to the benefit of both systems designers and equipment manufacturers, as well as to maximize hardware efficiency and circuit simplicity, Philips developed a simple bidirectional 2-wire bus for efficient inter-IC control. This bus is called the Inter IC or I²C-bus. At present, Philips' IC range includes more than 150 CMOS and bipolar I²C-bus compatible types for performing functions in all three of the previously mentioned categories. All I²C-bus compatible devices incorporate an on-chip interface which allows them to communicate directly with each other via the I²C-bus. This design concept solves the many interfacing problems encountered when designing digital control circuits.

Here are some of the features of the I²C-bus:

- Only two bus lines are required; a serial data line (SDA) and a serial clock line (SCL)
- Each device connected to the bus is software addressable by a unique address and simple master/ slave relationships exist at all times; masters can operate as master-transmitters or as master-receivers
- It's a true multi-master bus including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer
- Serial, 8-bit oriented, bidirectional data transfers can be made at up to 100 kbit/s in the standard mode or up to 400 kbit/s in the fast mode
- On-chip filtering rejects spikes on the bus data line to preserve data integrity
- The number of ICs that can be connected to the same bus is limited only by a maximum bus capacitance of 400 pF.

Figure 1 shows two examples of I²C-bus applications.

1.1 Designer benefits

I²C-bus compatible ICs allow a system design to rapidly progress directly from a functional block diagram to a prototype. Moreover, since they 'clip' directly onto the I²C-bus without any additional external interfacing, they allow a prototype system to be modified or upgraded simply by 'clipping' or 'unclipping' ICs to or from the bus.

Here are some of the features of I²C-bus compatible ICs which are particularly attractive to designers:

- Functional blocks on the block diagram correspond with the actual ICs; designs proceed rapidly from block diagram to final schematic
- No need to design bus interfaces because the I²C-bus interface is already integrated on-chip
- Integrated addressing and data-transfer protocol allow systems to be completely software-defined
- The same IC types can often be used in many different applications
- Design-time reduces as designers quickly become familiar with the frequently used functional blocks represented by I²C-bus compatible ICs
- ICs can be added to or removed from a system without affecting any other circuits on the bus
- Fault diagnosis and debugging are simple; malfunctions can be immediately traced
- Software development time can be reduced by assembling a library of reusable software modules.

In addition to these advantages,the CMOS ICs in the I²C-bus compatible range offer designers special features which are particularly attractive for portable equipment and battery-backed systems.

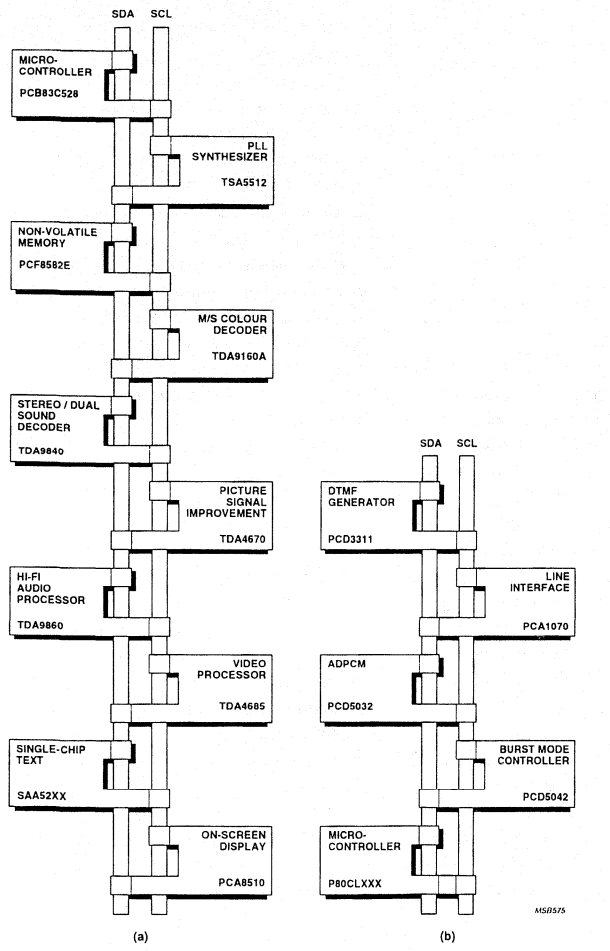


Fig.1 Two examples of I²C-bus applications (a) a high performance highly-integrated TV set (b) DECT cordless phone base-station

They all have:

- Extremely low current consumption
- High noise immunity
- Wide supply voltage range
- Wide operating temperature range.

1.2 Manufacturer benefits

I²C-bus compatible ICs don't only assist designers, they also give a wide range of benefits to equipment manufacturers because:

- The simple 2-wire serial I²C-bus minimizes interconnections so ICs have fewer pins and there are not so many PCB tracks; result - smaller and less expensive PCBs
- The completely integrated I²C-bus protocol eliminates the need for address decoders and other 'glue logic'
- The multi-master capability of the I²C-bus allows rapid testing and alignment of end-user equipment via external connections to an assembly-line computer
- The availability of I²C-bus compatible ICs in SO (small outline), VSO (very small outline) as well as DIL packages reduces space requirements even more.

These are just some of the benefits. In addition, I²C-bus compatible ICs increase system design flexibility by allowing simple construction of equipment variants and easy upgrading to keep designs up-to-date. In this way, an entire family of equipment can be developed around a basic model. Upgrades for new equipment, or enhanced-feature models (i.e. extended memory, remote control, etc.) can then be produced simply by clipping the appropriate ICs onto the bus. If a larger ROM is needed, it's simply a matter of selecting a micro-controller with a larger ROM from our comprehensive range. As new ICs supersede older ones, it's easy to add new features to equipment or to increase its performance by simply unclipping the outdated IC from the bus and clipping on its successor.

1.3 The ACCESS.bus

Another attractive feature of the I²C-bus for designers and manufacturers is that its simple 2-wire nature and capability of software addressing make it an ideal platform for the ACCESS.bus (Fig.2). This is a lower-cost alternative for an RS-232C interface for connecting peripherals to a host computer via a simple 4-pin connector (see Section 19).

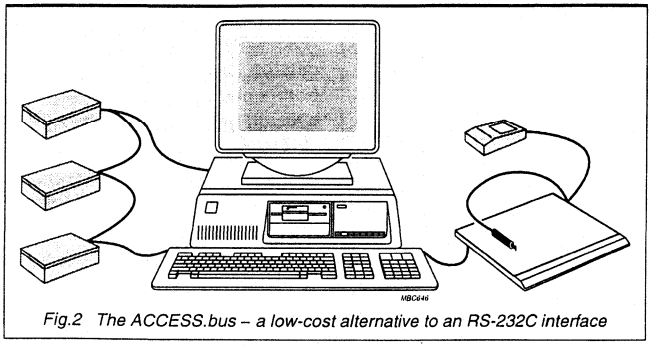


Fig.2 The ACCESS.bus – a low-cost alternative to an RS-232C interface

2.0 INTRODUCTION TO THE I²C-BUS SPECIFICATION

For 8-bit digital control applications, such as those requiring microcontrollers, certain design criteria can be established:

- A complete system usually consists of at least one microcontroller and other peripheral devices such as memories and I/O expanders
- The cost of connecting the various devices within the system must be minimized
- A system that performs a control function doesn't require high-speed data transfer
- Overall efficiency depends on the devices chosen and the nature of the interconnecting bus structure.

In order to produce a system to satisfy these criteria, a serial bus structure is needed. Although serial buses don't have the throughput capability of parallel buses, they do require less wiring and fewer IC connecting pins. However, a bus is not merely an interconnecting wire, it embodies all the formats and procedures for communication within the system.

Devices communicating with each other on a serial bus must have some form of protocol which avoids all possibilities of confusion, data loss and blockage of information. Fast devices must be able to communicate with slow devices. The system must not be dependent on the devices connected to it, otherwise modifications or improvements would be impossible. A procedure has also to be devised to decide which device will be in control of the bus and when. And, if different devices with different clock speeds are connected to the bus, the bus clock source must be defined. All these criteria are involved in the specification of the I²C-bus.

3.0 THE I²C-BUS CONCEPT

The I²C-bus supports any IC fabrication process (NMOS, CMOS, bipolar). Two wires, serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus. Each device is recognised by a unique address - whether it's a microcontroller, LCD driver, memory or keyboard interface - and can operate as either a transmitter or receiver, depending on the function of the device. Obviously an LCD driver is only a receiver, whereas a memory can both receive and transmit data. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers (see Table 1). A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The I²C-bus is a multi-master bus. This means that more than one device capable of controlling the bus can be connected to it. As masters are usually micro-controllers, let's consider the case of a data transfer between two microcontrollers connected to the I²C-bus (Fig.3). This highlights the master-slave and receiver-transmitter relationships to be found on the I²C-bus. It should be noted that these relationships are not permanent, but only depend

Table 1 Definition of I²C-bus terminology

Term	Description
Transmitter	The device which sends the data to the bus
Receiver	The device which receives the data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by a master
Multi-master	More than one master can attempt to control the bus at the same time without corrupting the message
Arbitration	Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
Synchronization	Procedure to synchronize the clock signals of two or more devices

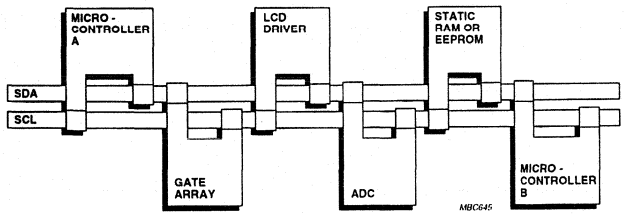


Fig.3 Example of an I²C-bus configuration using two microcontrollers

on the direction of data transfer at that time. The transfer of data would proceed as follows:

1) Suppose microcontroller A wants to send information to microcontroller B:

- microcontroller A (master), addresses microcontroller B (slave)
- microcontroller A (master-transmitter), sends data to microcontroller B (slave-receiver)
- microcontroller A terminates the transfer.

2) If microcontroller A wants to receive information from microcontroller B:

- microcontroller A (master) addresses microcontroller B (slave)
- microcontroller A (master-receiver) receives data from microcontroller B (slave-transmitter)
- microcontroller A terminates the transfer.

Even in this case, the master (microcontroller A) generates the timing and terminates the transfer.

The possibility of connecting more than one microcontroller to the I²C-bus means that more than one master could try to initiate a data transfer at the same time. To avoid the chaos that might ensue from such an event - an arbitration procedure has been developed. This procedure relies on the wired-AND connection of all I²C interfaces to the I²C-bus.

If two or more masters try to put information onto the bus, the first to produce a 'one' when the other produces a 'zero' will lose the arbitration. The clock signals during arbitration are a synchronized combination of the clocks generated by the masters using the wired-AND connection to the SCL line (for more detailed information concerning arbitration see Section 7.0).

Generation of clock signals on the I²C-bus is always the responsibility of master devices; each master generates its own clock signals when transferring data on the bus. Bus clock signals from a master can only be altered when they are stretched by a slow-slave device holding-down the clock line, or by another master when arbitration occurs.

4.0 GENERAL CHARACTERISTICS

Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor (see Fig.4). When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector in order to perform the wired-AND function. Data on the I²C-bus can be transferred at a rate up to 100 kbit/s in the standard-mode, or up to 400 kbit/s in the fast-mode. The number of interfaces connected to the bus is solely dependent on the bus capacitance limit of 400 pF.

5.0 BIT TRANSFER

Due to the variety of different technology devices (CMOS, NMOS, bipolar) which can be connected to the I²C-bus, the levels of the logical '0' (LOW) and '1' (HIGH) are not fixed and depend on the associated level of V_{DD} (see Section 15.0 for Electrical Specifications). One

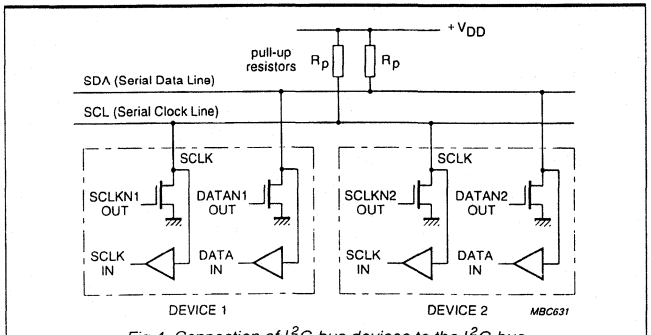


Fig.4 Connection of I²C-bus devices to the I²C-bus

clock pulse is generated for each data bit transferred.

5.1 Data validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (see Fig.5).

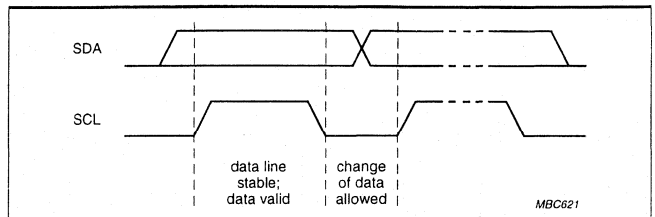


Fig.5 Bit transfer on the I²C-bus

5.2 START and STOP conditions

Within the procedure of the I²C-bus, unique situations arise which are defined as START and STOP conditions (see Fig.6).

A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition.

A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition. This bus free situation is specified in Section 15.0.

Detection of START and STOP conditions by devices connected to the bus is easy if they incorporate the necessary interfacing hardware. However, microcontrollers with no such interface have to sample the SDA line at least twice per clock period in order to sense the transition.

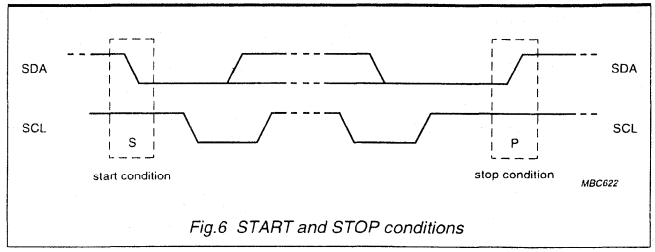


Fig.6 START and STOP conditions

6.0 TRANSFERRING DATA

6.1 Byte format

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (Fig.7). If a receiver can't receive another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the transmitter into a wait state. Data transfer then continues when the receiver is ready for another byte of data and releases clock line SCL.

In some cases, it's permitted to use a different format from the I²C-bus format (for CBUS compatible devices for example). A message which starts with such an address can be terminated by generation of a STOP condition, even during the transmission of a byte. In this case, no acknowledge is generated (see Section 9.1.3).

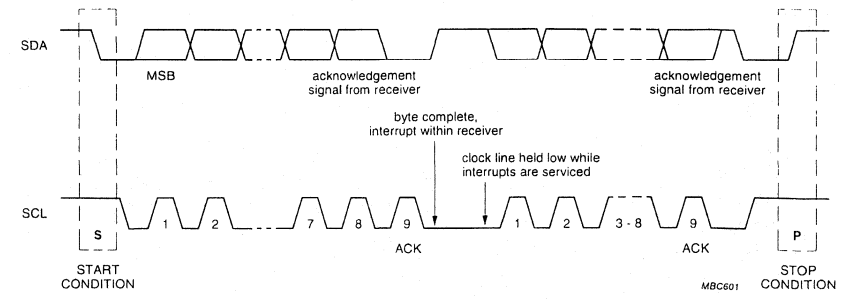


Fig.7 Data transfer on the I²C-bus

6.2 Acknowledge

Data transfer with acknowledge is obligatory. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse.

The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse (Fig.8). Of course, set-up and hold times (specified in Section 15) must also be taken into account.

Usually, a receiver which has been addressed is obliged to generate an acknowledge after each byte has been received, except when the message starts with a CBUS address (see Section 9.1.3).

When a slave-receiver doesn't acknowledge the slave address (for example, it's unable to receive because it's performing some real-time function), the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer.

If a slave-receiver does acknowledge the slave address but, some time later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

If a master-receiver is involved in a transfer, it must signal the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter must release the data line to allow the master to generate a STOP or repeated START condition.

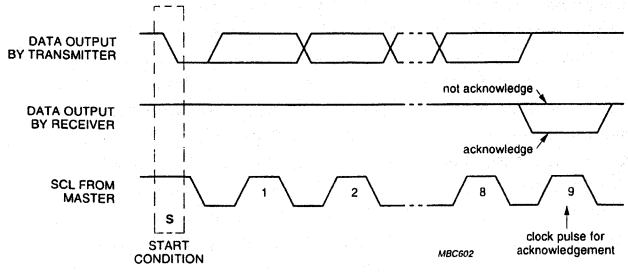


Fig.8 Acknowledge on the I²C-bus

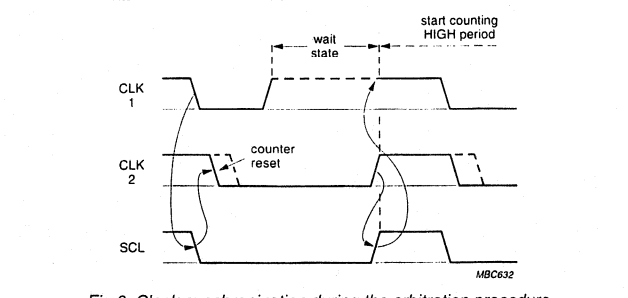


Fig.9 Clock synchronization during the arbitration procedure

7.0 ARBITRATION AND CLOCK GENERATION

7.1 Synchronization

All masters generate their own clock on the SCL line to transfer messages on the I²C-bus. Data is only valid during the HIGH period of the clock. A defined clock is therefore needed for the bit-by-bit arbitration procedure to take place.

Clock synchronization is performed using the wired-AND connection of I²C interfaces to the SCL line. This means that a HIGH to LOW transition on the SCL line will cause the devices concerned to start counting off their LOW period and, once a device clock has gone LOW, it will hold the SCL line in that state until the clock HIGH state is reached (Fig.9). However, the LOW to HIGH transition of this clock may not change the state of the SCL line if another clock is still within its LOW period. The SCL line will therefore be held LOW by the device with the longest LOW period. Devices with shorter LOW periods enter a HIGH wait-state during this time.

When all devices concerned have counted off their LOW period, the clock line will be released and go HIGH. There will then be no difference between the device clocks and the state of the SCL line, and all the devices will start counting their HIGH periods. The first device to complete its HIGH period will again pull the SCL line LOW.

In this way, a synchronized SCL clock is generated with its LOW period determined by the device with the longest clock LOW period, and its HIGH period determined by the one with the shortest clock HIGH period.

7.2 Arbitration

A master may start a transfer only if the bus is free. Two or more masters may generate a START condition within the minimum hold time ($t_{HD;STA}$) of the START condition which results in a defined START condition to the bus.

Arbitration takes place on the SDA line, while the SCL line is at the HIGH level, in such a way that the master which transmits a HIGH level, while another master is transmitting a LOW level will switch off its DATA output stage because the level on the bus doesn't correspond to its own level.

Arbitration can continue for many bits. Its first stage is comparison of the address bits (addressing information is in Sections 9.0 and 13.0). If the masters are each trying to address the same device, arbitration continues with comparison of the data. Because address and data information on the I²C-bus is used for arbitration, no information is lost during this process.

A master which loses the arbitration can generate clock pulses until the end of the byte in which it loses the arbitration.

If a master also incorporates a slave function and it loses arbitration during the addressing stage, it's possible that the winning master is trying to address it. The losing master must therefore switch over immediately to its slave-receiver mode.

Figure 10 shows the arbitration procedure for two masters. Of course, more may be involved (depending on how many masters are connected to the bus). The moment there is a difference between the internal data level of the master generating DATA 1 and the actual level on the SDA line, its data output is switched off, which means that a HIGH output level is then connected to the bus. This will not affect the data transfer initiated by the winning master.

Since control of the I²C-bus is decided solely on the address and data sent by competing masters, there is no central master, nor any order of priority on the bus.

Special attention must be paid if, during a serial transfer, the arbitration procedure is still in progress at the moment when a repeated START condition or a STOP condition is transmitted to the I²C-bus. If it's possible for such a situation to occur, the masters involved must send this repeated START condition or STOP condition at the same position in the format frame. In other words, arbitration isn't allowed between:

- A repeated START condition and a data bit
- A STOP condition and a data bit
- A repeated START condition and a STOP condition.

7.3 Use of the clock synchronizing mechanism as a handshake

In addition to being used during the arbitration procedure, the clock synchronization mechanism can be used to enable receivers to cope with fast data transfers, on either a byte level or a bit level.

On the byte level, a device may be able to receive bytes of data at a fast rate, but needs more time to store a received byte or prepare another byte to be transmitted. Slaves can then hold the SCL line LOW after reception and acknowledgement of a byte to force the master into a wait state until the slave is ready for the next byte transfer in a type of handshake procedure.

On the bit level, a device such as a microcontroller without, or with only a limited hardware I²C interface on-chip can slow down the bus clock by extending each clock LOW period. The speed of any master is thereby adapted to the internal operating rate of this device.

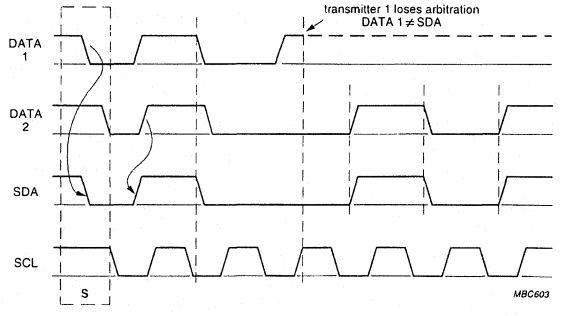


Fig.10 Arbitration procedure of two masters

8.0 FORMATS WITH 7-BIT ADDRESSES

Data transfers follow the format shown in Fig.11. After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/$\overline{W}$) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition. Various combinations of read/write formats are then possible within such a transfer.

Possible data transfer formats are:

- **Master-transmitter transmits to slave-receiver. The transfer direction is not changed (Fig.12)**
- **Master reads slave immediately after first byte (Fig.13)**. At the moment of the first acknowledge, the master-transmitter becomes a master-receiver and the slave-receiver becomes a slave-transmitter. This acknowledge is still generated by the slave. The STOP condition is generated by the master
- **Combined format (Fig.14)**. During a change of direction within a transfer, the START condition and the slave address are both repeated, but with the R/$\overline{W}$ bit reversed. If a master receiver sends a repeated START condition, it has previously sent a not acknowledge ($\overline{A}$).

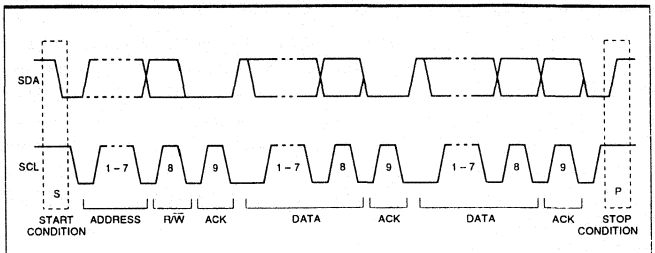


Fig.11 A complete data transfer

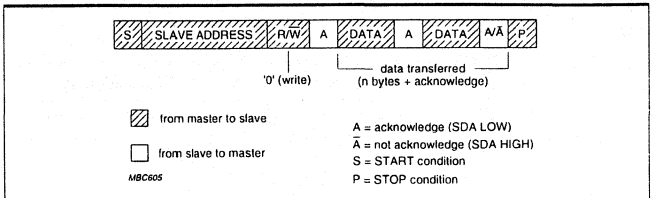


Fig.12 A master-transmitter addresses a slave receiver with a 7-bit address. The transfer direction is not changed

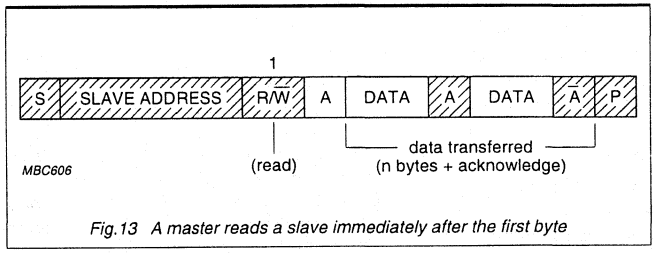


Fig.13 A master reads a slave immediately after the first byte

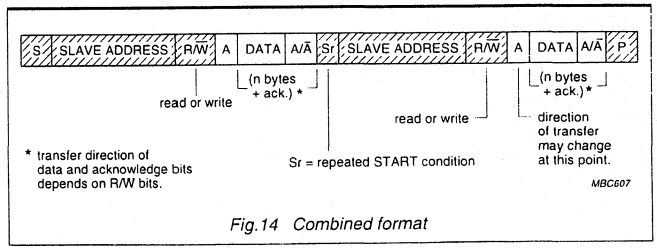


Fig.14 Combined format

NOTES:

1) Combined formats can be used, for example, to control a serial memory. During the first data byte, the internal memory location has to be written. After the START condition and slave address is repeated, data can be transferred.
2) All decisions on auto-increment or decrement of previously accessed memory locations etc. are taken by the designer of the device.
3) Each byte is followed by an acknowledgement bit as indicated by the A or $\overline{A}$ blocks in the sequence.
4) I²C-bus compatible devices must reset their bus logic on receipt of a START or repeated START condition such that they all anticipate the sending of a slave address.

9.0 7-BIT ADDRESSING (see Section 13 for 10-bit addressing)

The addressing procedure for the I²C-bus is such that the first byte after the START condition usually determines which slave will be selected by the master. The exception is the 'general call' address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge. However, devices can be made to ignore this address. The second byte of the general call address then defines the action to be taken. This procedure is explained in more detail in Section 9.1.1.

9.1 Definition of bits in the first byte

The first seven bits of the first byte make up the slave address (Fig.15). The eighth bit is the LSB (least significant bit). It determines the direction of the message. A 'zero' in the least significant position of the first byte means that the master will write information to a selected slave. A 'one' in this position means that the master will read information from the slave.

When an address is sent, each device in a system compares the first seven bits after the START condition with its address. If they match, the device considers itself addressed by the master as a slave-receiver or slave-transmitter, depending on the R/$\overline{W}$ bit.

A slave address can be made-up of a fixed and a programmable part. Since it's likely that there will be several identical devices in a system, the programmable part of the slave address enables the maximum possible number of such devices to be connected to the I²C-bus. The number of programmable address bits of a device depends on the number of pins available. For example, if a device has 4 fixed and 3 programmable address bits, a total of 8 identical devices can be connected to the same bus.

The I²C-bus committee coordinates allocation of I²C addresses. Further information can be obtained from the Philips representatives listed on the back cover. Two groups of eight addresses (0000XXX and 1111XXX) are reserved for the purposes shown in Table 2. The bit combination 11110XX of the slave address is reserved for 10-bit addressing (see Section 13).

Table 2 Definition of bits in the first byte

Slave address	R/$\overline{W}$ bit	Description
0000 000	0	General call address
0000 000	1	START byte
0000 001	X	CBUS address
0000 010	X	Address reserved for different bus format
0000 011	X	Reserved for future purposes
0000 1XX	X	
1111 1XX	X	
1111 0XX	X	10-bit slave addressing

NOTES:

1) No device is allowed to acknowledge at the reception of the START byte.
2) The CBUS address has been reserved to enable the inter-mixing of CBUS compatible and I²C-bus compatible devices in the same system. I²C-bus compatible devices are not allowed to respond on reception of this address.
3) The address reserved for a different bus format is included to enable I²C and other protocols to be mixed. Only I²C-bus compatible devices that can work with such formats and protocols are allowed to respond to this address.

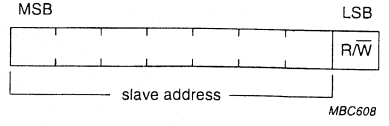


Fig.15 The first byte after the START procedure

9.1.1 General call address

The general call address is for addressing every device connected to the I²C-bus. However, if a device doesn't need any of the data supplied within the general call structure, it can ignore this address by not issuing an acknowledgement. If a device does require data from a general call address, it will acknowledge this address and behave as a slave- receiver. The second and following bytes will be acknowledged by every slave-receiver capable of handling this data. A slave which cannot process one of these bytes must ignore it by not acknowledging. The meaning of the general call address is always specified in the second byte (Fig.16).

There are two cases to consider:

- When the least significant bit B is a 'zero'
- When the least significant bit B is a 'one'.

When bit B is a 'zero'; the second byte has the following definition:

- 00000110 (H'06'). Reset and write programmable part of slave address by hardware. On receiving this 2-byte sequence, all devices designed to respond to the general call address will reset and take in the programmable part of their address. Precautions have to be taken to ensure that a device is not pulling down the SDA or SCL line after applying the supply voltage, since these low levels would block the bus
- 00000100 (H'04'). Write programmable part of slave address by hardware. All devices which define the programmable part of their address by hardware (and which respond to the general call address) will latch this programmable part at the reception of this two byte sequence. The device will not reset.
- 00000000 (H'00'). This code is not allowed to be used as the second byte.

Sequences of programming procedure are published in the appropriate device data sheets.

The remaining codes have not been fixed and devices must ignore them.

When bit B is a 'one'; the 2-byte sequence is a 'hardware general call'. This means that the sequence is transmitted by a hardware master device, such as a keyboard scanner, which cannot be programmed to transmit a desired slave address. Since a hardware master doesn't know in advance to which device the message has to be transferred, it can only generate this hardware general call and its own address - identifying itself to the system (Fig.17).

The seven bits remaining in the second byte contain the address of the hardware master. This address is recognised by an intelligent device (e.g. a microcontroller) connected to the bus which will then direct the information from the hardware master. If the hardware master can also act as a slave, the slave address is identical to the master address.

In some systems, an alternative could be that the hardware master transmitter is set in the slave-

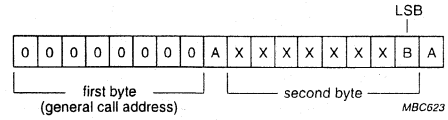


Fig.16 General call address format

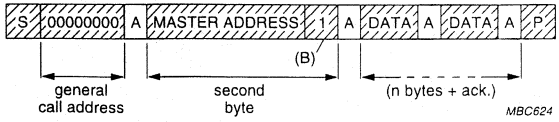


Fig.17 Data transfer from a hardware master-transmitter

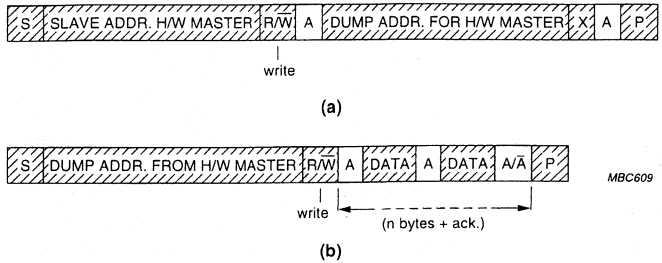


Fig.18 Data transfer by a hardware-transmitter capable of dumping data directly to slave devices (a) Configuring master sends dump address to hardware master (b) Hardware master dumps data to selected slave

receiver mode after the system reset. In this way, a system configuring master can tell the hardware master-transmitter (which is now in slave-receiver mode) to which address data must be sent (Fig.18). After this programming procedure, the hardware master remains in the master-transmitter mode.

9.1.2 START byte

Microcontrollers can be connected to the I²C-bus in two ways. A microcontroller with an on-chip hardware I²C-bus interface can be programmed to be only interrupted by requests from the bus. When the device doesn't have such an interface, it must constantly monitor the bus via software. Obviously, the more times the microcontroller monitors, or polls the bus, the less time it can spend carrying out its intended function. There is therefore a speed difference between fast hardware devices and a relatively slow microcontroller which relies on software polling.

In this case, data transfer can be preceded by a start procedure which is much longer than normal (Fig.19). The start procedure consists of:

- A START condition (S)
- A START byte (00000001)
- An acknowledge clock pulse (ACK)
- A repeated START condition (Sr).

After the START condition S has been transmitted by a master which requires bus access, the START byte (00000001) is transmitted. Another microcontroller can therefore sample the SDA line at a low sampling rate until one of the seven zeros in the START byte is detected. After detection of this LOW level on the SDA line, the microcontroller can switch to a higher sampling rate to find the repeated START condition Sr which is then used for synchronization.

A hardware receiver will reset on receipt of the repeated START condition Sr and will therefore ignore the START byte.

An acknowledge-related clock pulse is generated after the START byte. This is present only to conform with the byte handling format used on the bus. No device is allowed to acknowledge the START byte.

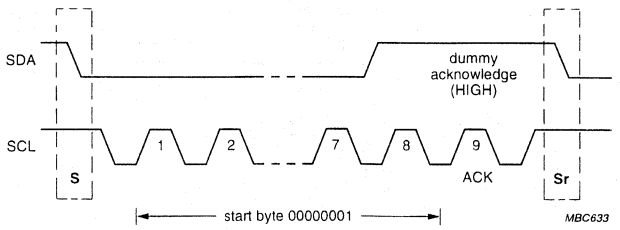


Fig.19 START byte procedure

9.1.3 CBUS compatibility

CBUS receivers can be connected to the I²C-bus. However, a third bus line called DLEN must then be connected and the acknowledge bit omitted. Normally, I²C transmissions are sequences of 8-bit bytes; CBUS compatible devices have different formats.

In a mixed bus structure, I²C-bus devices must not respond to the CBUS message. For this reason, a special CBUS address (0000001X) to which no I²C-bus compatible device will respond, has been reserved. After transmission of the CBUS address, the DLEN line can be made active and a CBUS-format transmission (Fig.20) sent. After the STOP condition, all devices are again ready to accept data.

Master-transmitters can send CBUS formats after sending the CBUS address. The transmission is ended by a STOP condition, recognised by all devices.

NOTE: If the CBUS configuration is known, and expansion with CBUS compatible devices isn't foreseen, the designer is allowed to adapt the hold time to the specific requirements of the device(s) used.

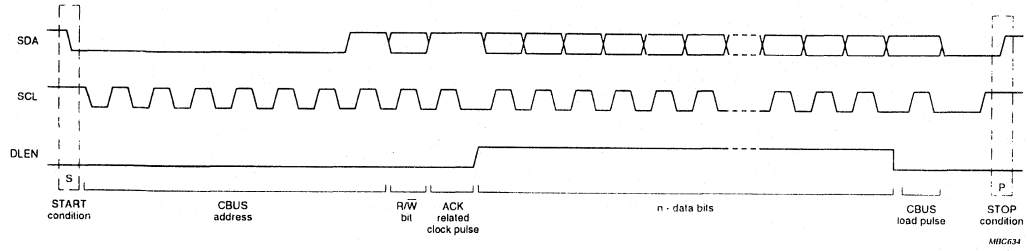


Fig.20 Data format of transmissions with CBUS transmitter/receiver

10.0 ELECTRICAL CHARACTERISTICS FOR I²C-BUS DEVICES

The electrical specifications for the I/Os of I²C-bus devices and the characteristics of the bus lines connected to them are given in Tables 3 and 4 in Section 15.

I²C-bus devices with fixed input levels of 1.5 V and 3 V can each have their own appropriate supply voltage. Pull-up resistors must be connected to a 5 V ± 10% supply (Fig.21). I²C-bus devices with input levels related to V_{DD} must have one common supply line to which the pull-up resistor is also connected (Fig.22).

When devices with fixed input levels are mixed with devices with input levels related to V_{DD}, the latter devices must be connected to one common supply line of 5 V ± 10% and must have pull-up resistors connected to their SDA and SCL pins as shown in Fig.23.

Input levels are defined in such a way that:

- The noise margin on the LOW level is 0.1 V_{DD}
- The noise margin on the HIGH level is 0.2 V_{DD}
- As shown in Fig.24, series resistors (R_S) of e.g. 300 Ω can be used for protection against high-voltage spikes on the SDA and SCL lines (due to flash-over of a TV picture tube, for example).

10.1 Maximum and minimum values of resistors R_p and R_s

For standard-mode I²C-bus devices, the values of resistors R_p and R_s in Fig.24 depend on the following parameters:

- Supply voltage
- Bus capacitance
- Number of connected devices (input current + leakage current).

The supply voltage limits the minimum value of resistor R_p due

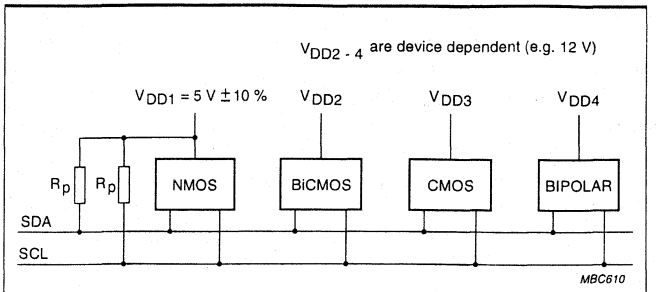


Fig.21 Fixed input level devices connected to the I²C-bus

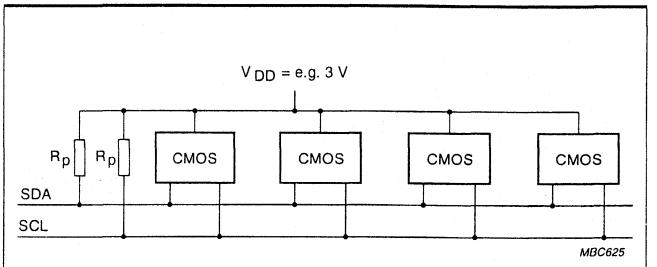


Fig.22 Devices with wide supply voltage range connected to the I²C-bus

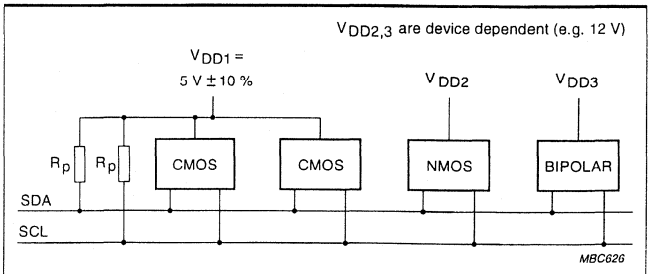


Fig.23 Devices with input levels related to V_{DD} (supply V_{DD1}) mixed with fixed input level devices (supply $V_{DD2,3}$) on the I²C-bus

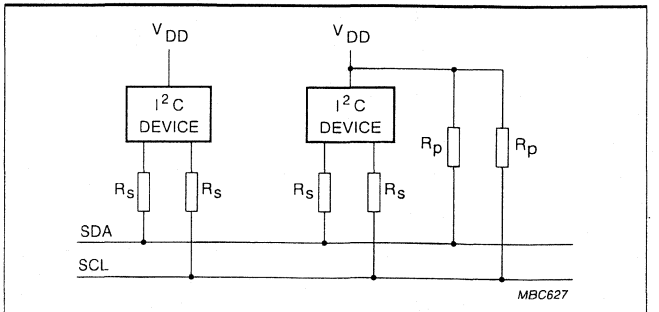


Fig.24 Series resistors (R_s) for protection against high-voltage spikes

to the specified minimum sink current of 3 mA at V_{OLmax} = 0.4 V for the output stages. V_{DD} as a function of $R_{p\ min}$ is shown in Fig.25. The desired noise margin of $0.1V_{DD}$ for the LOW level, limits the maximum value of R_s. $R_{s\ max}$ as a function of R_p is shown in Fig.26.

The bus capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of R_p due to the specified rise time. Fig.27 shows $R_{p\ max}$ as a function of bus capacitance.

The maximum HIGH level input current of each input/output connection has a specified maximum value of 10 μA. Due to the desired noise margin of $0.2V_{DD}$ for the HIGH level, this input current limits the maximum value of R_p. This limit depends on V_{DD}. The total HIGH level input current is shown as a function of $R_{p\ max}$ in Fig.28.

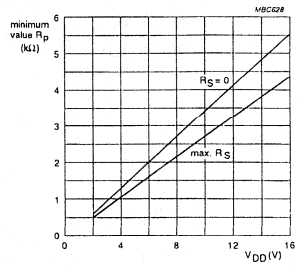


Fig.25 Minimum value of R_p as a function of supply voltage with the value of R_s as a parameter

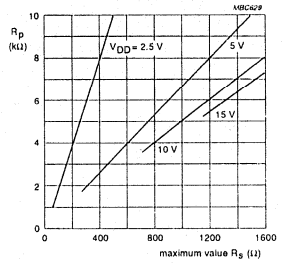


Fig.26 Maximum value of R_s as a function of the value of R_p with supply voltage as a parameter

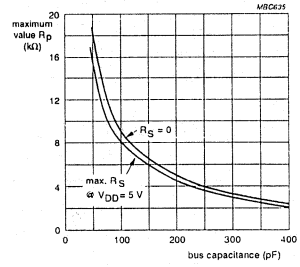


Fig.27 Maximum value of R_p as a function of bus capacitance for a standard-mode I^2C-bus

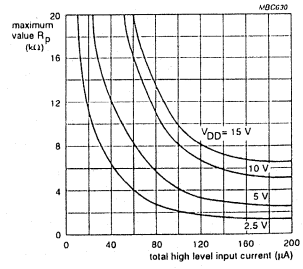


Fig.28 Total HIGH level input current as a function of the maximum value of R_p with supply voltage as a parameter

11.0 EXTENSIONS TO THE I²C-BUS SPECIFICATION

The I²C-bus with a data transfer rate of up to 100 kbit/s and 7-bit addressing has now been in existence for more than ten years with an unchanged specification. The concept is accepted world-wide as a de facto standard and hundreds of different types of I²C-bus compatible ICs are available from Philips and other suppliers. The I²C-bus specification is now extended with the following two features:

- A **fast-mode** which allows a fourfold increase of the bit rate to 0 to 400 kbit/s
- **10-bit addressing** which allows the use of up to 1024 additional addresses.

There are two reasons for these extensions to the I²C-bus specification:

- New applications will need to transfer a larger amount of serial data and will therefore demand a higher bit rate than 100 kbit/s. Improved IC manufacturing technology now allows a fourfold speed increase without increasing the manufacturing cost of the interface circuitry
- Most of the 112 addresses available with the 7-bit addressing scheme have been issued more than once. To prevent problems with the allocation of slave addresses for new devices, it is desirable to have more address combinations. About a tenfold increase of the number of available addresses is obtained with the new 10-bit addressing.

All new devices with an I²C-bus interface are provided with the fast-mode. Preferably, they should be able to receive and/or transmit at 400 kbit/s. The minimum requirement is that they can synchronize with a 400 kbit/s transfer; they can then prolong the LOW period of the SCL signal to slow down the transfer. Fast-mode devices must be downward-compatible which means that they must still be able to communicate with 0 to 100 kbit/s devices in a 0 to 100 kbit/s I²C-bus system.

Obviously, devices with a 0 to 100 kbit/s I²C-bus interface cannot be incorporated in a fast-mode I²C-bus system because, since they cannot follow the higher transfer rate, unpredictable states of these devices would occur.

Slave devices with a fast-mode I²C-bus interface can have a 7-bit or a 10-bit slave address. However, a 7-bit address is preferred because it is the cheapest solution in hardware and it results in the shortest message length. Devices with 7-bit and 10-bit addresses can be mixed in the same I²C-bus system regardless of whether it is a 0 to 100 kbit/s standard-mode system or a 0 to 400 kbit/s fast-mode system. Both existing and future masters can generate either 7-bit or 10-bit addresses.

12.0 FAST-MODE

In the fast-mode of the I²C-bus, the protocol, format, logic levels and maximum capacitive load for the SDA and SCL lines quoted in the previous I²C-bus specification are unchanged. Changes to the previous I²C-bus specification are:

- The maximum bit rate is increased to 400 kbit/s
- Timing of the serial data (SDA) and serial clock (SCL) signals has been adapted. There is no need for compatibility with other bus systems such as CBUS because they cannot operate at the increased bit rate
- The inputs of fast-mode devices must incorporate spike suppression and a Schmitt trigger at the SDA and SCL inputs
- The output buffers of fast-mode devices must incorporate slope control of the falling edges of the SDA and SCL signals
- If the power supply to a fast-mode device is switched off, the SDA and SCL I/O pins must be floating so that they don't obstruct the bus lines
- The external pull-up devices connected to the bus lines must be adapted to accommodate the shorter maximum permissible rise time for the fast-mode I²C-bus. For bus loads up to 200 pF, the pull-up device for each bus line can be a resistor; for bus loads between 200 pF and 400 pF, the pull-up device can be a current source (3 mA max.) or a switched resistor circuit as shown in Fig.37.

13.0 10-BIT ADDRESSING

The 10-bit addressing does not change the format in the I²C-bus specification. Using 10 bits for addressing exploits the reserved combination 1111XXX for the first seven bits of the first byte following a START (S) or repeated START (Sr) condition as explained in Section 9.1. The 10-bit addressing does not affect the existing 7-bit addressing. Devices with 7-bit and 10-bit addresses can be connected to the same I²C-bus, and both 7-bit and 10-bit addressing can be used in a standard-mode system (up to 100 kbit/s) or a fast-mode system (up to 400 kbit/s).

Although there are eight possible combinations of the reserved address bits 1111XXX, only the four combinations 11110XX are used for 10-bit addressing. The remaining four combinations 11111XX are reserved for future I²C-bus enhancements.

13.1 Definition of bits in the first two bytes

The 10-bit slave address is formed from the first two bytes following a START condition (S) or a repeated START condition (Sr).

The first seven bits of the first byte are the combination 11110XX of which the last two bits (XX) are the two most-significant bits (MSBs) of the 10-bit address; the eighth bit of the first byte is the R/$\overline{W}$ bit that determines the direction of the message. A 'zero' in the least significant position of the first byte means that the master will write information to a selected slave. A 'one' in this position means that the master will read information from the slave.

If the R/$\overline{W}$ bit is 'zero', then the second byte contains the remaining 8 bits (XXXXXXXX) of the 10-bit address. If the R/$\overline{W}$ bit is 'one', then the next byte contains data transmitted from a slave to a master.

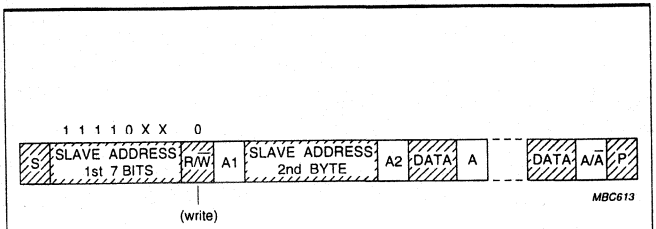


Fig.29 A master-transmitter addresses a slave-receiver with a 10-bit address

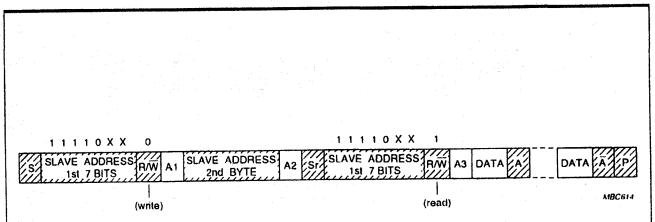


Fig.30 A master-receiver addresses a slave-transmitter with a 10-bit address

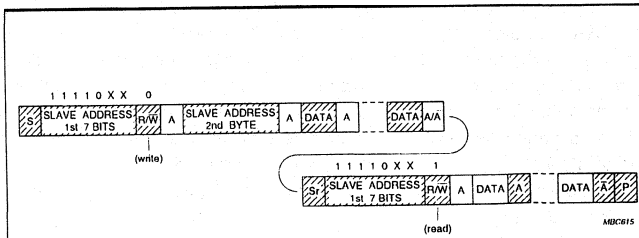


Fig.31 Combined format. A master addresses a slave with a 10-bit address, then transmits data to this slave and reads data from this slave

13.2 Formats with 10-bit addresses

Various combinations of read/write formats are possible within a transfer that includes 10-bit addressing. Possible data transfer formats are:

- **Master-transmitter transmits to slave-receiver with a 10-bit slave address. The transfer direction is not changed (Fig.29).** When a 10-bit address follows a START condition, each slave compares the first seven bits of the first byte of the slave address (11110XX) with its own address and tests if the eighth bit (R/$\overline{W}$ direction bit) is 0. It is possible that more than one device will find a match and generate an acknowledge (A1). All slaves that found a match will compare the eight bits of the second byte of the slave address (XXXXXXXX) with their own addresses, but only one slave will find a match and generate an acknowledge (A2). The matching slave will remain addressed by the master until it receives a STOP condition (P) or a repeated START condition (Sr) followed by a different slave address
- **Master-receiver reads slave-transmitter with a 10-bit slave address. The transfer direction is changed after the second R/$\overline{W}$ bit (Fig.30).** Up to and including acknowledge bit A2, the procedure is the same as that described for a master-transmitter addressing a

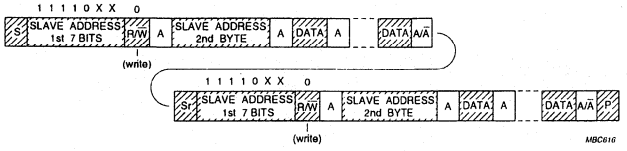


Fig.32 Combined format. A master transmits data to two slaves, both with 10-bit addresses

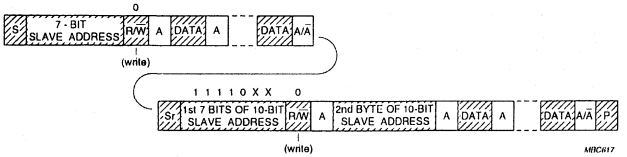


Fig.33 Combined format. A master transmits data to two slaves, one with a 7-bit address, and one with a 10-bit address

slave-receiver. After the repeated START condition (Sr), a matching slave remembers that it was addressed before. This slave then checks if the first seven bits of the first byte of the slave address following Sr are the same as they were after the START condition (S), and tests if the eighth (R/$\overline{W}$) bit is 1. If there is a match, the slave considers that it has been addressed as a transmitter and generates acknowledge A3.

The slave-transmitter remains addressed until it receives a STOP condition (P) or until it receives another repeated START condition (Sr) followed by a different slave address. After a repeated START condition (Sr), all the other slave devices will also compare the first seven bits of the first byte of the slave address (11110XX) with their own addresses and test the eighth (R/$\overline{W}$) bit. However, none of them will be addressed because R/$\overline{W}$ = 1 (for 10-bit devices), or the 11110XX slave address (for 7-bit devices) does not match)

- **Combined format. A master transmits data to a slave and then reads data from the same slave (Fig.31)**. The same master occupies the bus all the time. The transfer direction is changed after the second R/$\overline{W}$ bit
- **Combined format. A master transmits data to one slave and then transmits data to another slave (Fig.32)**. The same master occupies the bus all the time
- **Combined format. 10-bit and 7-bit addressing combined in one serial transfer (Fig.33)**. After each START condition (S), or each repeated START condition (Sr), a 10-bit or 7-bit slave address can be transmitted. Figure 33 shows how a master-transmits data to a slave with a 7-bit address and then transmits data to a second slave with a 10-bit address. The same master occupies the bus all the time.

NOTES:

1) Combined formats can be used, for example, to control a serial memory. During the first data byte, the internal memory location has to be written. After the START condition and slave address is repeated, data can be transferred.
2) All decisions on auto-increment or decrement of previously accessed memory locations etc. are taken by the designer of the device.
3) Each byte is followed by an acknowledgement bit as indicated by the A or $\overline{A}$ blocks in the sequence.
4) I²C-bus compatible devices must reset their bus logic on receipt of a START or repeated START condition such that they all anticipate the sending of a slave address.

14.0 GENERAL CALL ADDRESS AND START BYTE

The 10-bit addressing procedure for the I²C-bus is such that the first two bytes after the START condition (S) usually determine which slave will be selected by the master. The exception is the 'general call' address 00000000 (H'00'). Slave devices with 10-bit addressing will react to a 'general call' in the same way as slave devices with 7-bit addressing (see Section 9.1.1).

Hardware masters can transmit their 10-bit address after a 'general call'. In this case, the 'general call' address byte is followed by two successive bytes containing the 10-bit address of the master-transmitter. The format is as shown in Fig.17 where the first DATA byte contains the eight least-significant bits of the master address.

The START byte 00000001 (H'01') can precede the 10-bit addressing in the same way as for 7-bit addressing (see Section 9.1.2).

15.0 ELECTRICAL SPECIFICATIONS AND TIMING FOR I/O STAGES AND BUS LINES

The I/O levels, I/O current, spike suppression, output slope control and pin capacitance for I²C-bus devices are given in Table 3. The I²C-bus timing is given in Table 4. Figure 34 shows the timing definitions for the I²C-bus.

The noise margin for HIGH and LOW levels on the bus lines for fast-mode devices are the same as those specified in Section 10.0 for standard-mode I²C-bus devices.

The minimum HIGH and LOW periods of the SCL clock specified in Table 4 determine the maximum bit transfer rates of 100 kbit/s for standard-mode devices and 400 kbit/s for fast mode devices. Standard-mode and fast-mode I²C-bus devices must be able to follow transfers at their own maximum bit rates, either by being able to transmit or receive at that speed or by applying the clock synchronization procedure described in Section 7 which will force the master into a wait state and stretch the LOW period of the SCL signal. Of course, in the latter case the bit transfer rate is reduced.

Table 3 Characteristics of the SDA and SCL I/O stages for I²C-bus devices

Parameter	Symbol	standard-mode devices		fast-mode devices		Unit
		Min.	Max.	Min.	Max.	
LOW level input voltage: fixed input levels V_{DD}-related input levels	V_{IL}	 −0.5 −0.5	 1.5 $0.3V_{DD}$	 −0.5 −0.5	 1.5 $0.3V_{DD}$	V
HIGH level input voltage: fixed input levels V_{DD}-related input levels	V_{IH}	 3.0 $0.7V_{DD}$	 *1) *1)	 3.0 $0.7V_{DD}$	 *1) *1)	V
Hysteresis of Schmitt trigger inputs: fixed input levels V_{DD}-related input levels	V_{hys}	 n/a n/a	 n/a n/a	 0.2 $0.05V_{DD}$	 - -	V
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	n/a	n/a	0	50	ns
LOW level output voltage (open drain or open collector): at 3 mA sink current at 6 mA sink current	 V_{OL1} V_{OL2}	 0 n/a	 0.4 n/a	 0 0	 0.4 0.6	V
Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance from 10 pF to 400 pF: with up to 3 mA sink current at V_{OL1} with up to 6 mA sink current at V_{OL2}	t_{of}	 - n/a	 250[3] n/a	 $20 + 0.1C_b$[2] $20 + 0.1C_b$[2]	 250 250[3]	ns
Input current each I/O pin with an input voltage between 0.4 V and $0.9V_{DDmax}$	I_i	−10	10	−10[4]	10[4]	µA
Capacitance for each I/O pin	C_i	-	10	-	10	pF

n/a = not applicable

1) maximum $V_{IH} = V_{DDmax} + 0.5$ V

2) C_b = capacitance of one bus line in pF.

3) The maximum t_f for the SDA and SCL bus lines quoted in Table 4 (300 ns) is longer than the specified maximum t_{of} for the output stages (250 ns). This allows series protection resistors (R_s)to be connected between the SDA/SCL pins and the SDA/SCL bus lines as shown in Fig.37 without exceeding the maximum specified t_f.

4) I/O pins of fast-mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.

Table 4 Characteristics of the SDA and SCL bus lines for I²C-bus devices

Parameter	Symbol	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	µs
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	-	0.6	-	µs
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	µs
Data hold time: for CBUS compatible masters (see NOTE, Section 9.1.3) for I²C-bus devices	$t_{HD;DAT}$	 5.0 0[1]	 - -	 - 0[1]	 - 0.9[2]	 µs µs
Data set-up time	$t_{SU;DAT}$	250	-	100[3]	-	ns
Rise time of both SDA and SCL signals	t_r	-	1000	20 + 0.1C_b[4]	300	ns
Fall time of both SDA and SCL signals	t_f	-	300	20 + 0.1C_b[4]	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	µs
Capacitive load for each bus line	C_b	-	400	-	400	pF

All values referred to V_{IHmin} and V_{ILmax} levels (see Table 3).

1) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

2) The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

3) A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\,max} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the standard-mode I²C-bus specification) before the SCL line is released.

4) C_b = total capacitance of one bus line in pF.

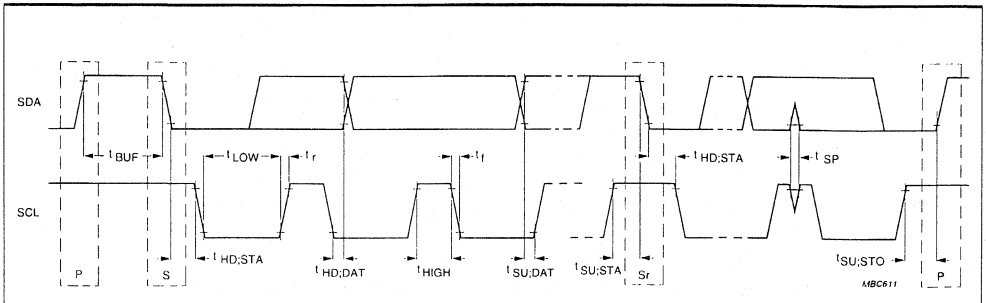


Fig.34 Definition of timing on the I²C-bus

16.0 APPLICATION INFORMATION

16.1 Slope-controlled output stages of fast-mode I²C-bus devices

The electrical specifications for the I/Os of I²C-bus devices and the characteristics of the bus lines connected to them are given in Tables 3 and 4 in Section 15.

Figures 35 and 36 show examples of output stages with slope control in CMOS and bipolar technology. The slope of the falling edge is defined by a Miller capacitor (C1) and a resistor (R1). The typical values for C1 and R1 are indicated on the diagrams. The wide tolerance for output fall time t_{of} given in Table 3 means that the design is not critical. The fall time is only slightly influenced by the external bus load (C_b) and external pull-up resistor (R_p). However, the rise time (t_r) specified in Table 4 is mainly determined by the bus load capacitance and the value of the pull-up resistor.

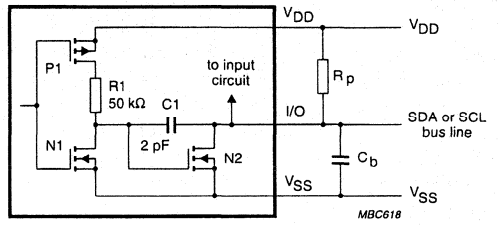


Fig.35 Slope-controlled output stage in CMOS technology

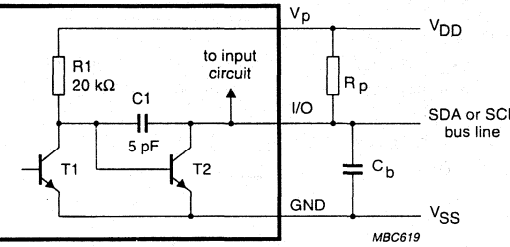
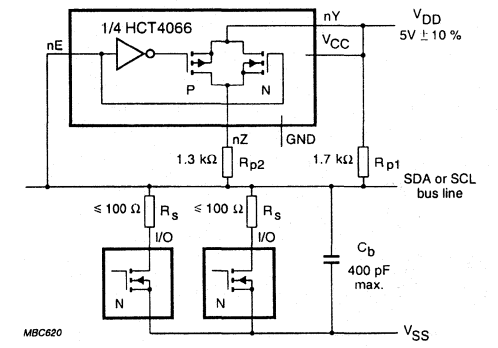


Fig.36 Slope-controlled output stage in bipolar technology

16.2 Switched pull-up circuit for fast-mode I²C-bus devices

The supply voltage (V_{DD}) and the maximum output LOW level determine the minimum value of pull-up resistor R_p (see Section 10.1). For example, with a supply voltage of V_{DD} = 5 V ± 10% and V_{OLmax} = 0.4 V at 3 mA, $R_{p\ min}$ = (5.5 − 0.4)/0.003 = 1.7 kΩ. As shown in Fig.38, this value of R_p limits the maximum bus capacitance to about 200 pF to meet the maximum t_r requirement of 300 ns. If the bus has a higher capacitance than this, a switched pull-up circuit as shown in Fig.37 can be used.

The switched pull-up circuit in Fig.37 is for a supply voltage of V_{DD} = 5 V ± 10 % and a maximum capacitive load of 400 pF. Since it is controlled by the bus levels, it needs no



FAST-MODE I²C BUS DEVICES

Fig.37 Switched pull-up circuit

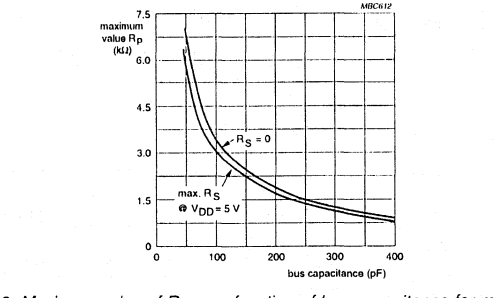


Fig.38 Maximum value of R_p as a function of bus capacitance for meeting the $t_{r\ max}$ requirement for a fast-mode I²C-bus

additional switching control signals. During the rising/falling edges, the bilateral switch in the HCT4066 switches pull-up resistor R_{p2} on/off at bus levels between 0.8 V and 2.0 V. Combined resistors R_{p1} and R_{p2} can pull-up the bus line within the maximum specified rise time (t_r) of 300 ns. The maximum sink current for the driving I²C-bus device will not exceed 6 mA at V_{OL2} = 0.6 V, or 3 mA at V_{OL1} = 0.4 V.

Series resistors R_s are optional. They protect the I/O stages of the I²C-bus devices from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus line signals. The maximum value of R_s is determined by the maximum permitted voltage drop across this resistor when the bus line is switched to the LOW level in order to switch off R_{p2}.

16.3 Wiring pattern of the bus lines

In general, the wiring must be so chosen that crosstalk and interference to/from the bus lines is minimized. The bus lines are most susceptible to crosstalk and interference at the HIGH level because of the relatively high impedance of the pull-up devices.

If the length of the bus lines on a PCB or ribbon cable exceeds 10 cm and includes the V_{DD} and V_{SS} lines, the wiring pattern must be:

SDA _____
V_{DD} _____
V_{SS} _____
SCL _____

If only the V_{SS} line is included, the wiring pattern must be:

SDA _____
V_{SS} _____
SCL _____

These wiring patterns also result in identical capacitive loads for the SDA and SCL lines. The V_{SS} and V_{DD} lines can be omitted if a PCB with a V_{SS} and/or V_{DD} layer is used.

If the bus lines are twisted-pairs, each bus line must be twisted with a V_{SS} return. Alternatively, the SCL line can be twisted with a V_{SS} return, and the SDA line twisted with a V_{DD} return. In the latter case, capacitors must be used to decouple the V_{DD} line to the V_{SS} line at both ends of the twisted pairs.

If the bus lines are shielded (shield connected to V_{SS}), interference will be minimized. However, the shielded cable must have low capacitive coupling between the SDA and SCL lines to minimize crosstalk.

16.4 Maximum and minimum values of resistors R_p and R_s for fast-mode I²C-bus devices

The maximum and minimum values for resistors R_p and R_s connected to a fast-mode I²C-bus can be determined from Fig.25, 26 and 28 in Section 10.1. Because a fast-mode I²C-bus has faster rise times (t_r) the maximum value of R_p as a function of bus capacitance is less than that shown in Fig.27 The replacement graph for Fig.27 showing the maximum value of R_p as a function of bus capacitance (C_b) for a fast mode I²C-bus is given in Fig.38.

17.0 DEVELOPMENT TOOLS

17.1 Development tools for 8048 and 8051-based systems

Product	Description
OM1016	I²C-bus demonstration board with microcontroller, LCD, LED, Par. I/O, SRAM, EEPROM, Clock, DTMF generator, AD/DA conversion, infrared link.
OM1018	manual for OM1016
OM1020	LCD and driver demonstration board
OM4151	I²C-bus evaluation board (similar to OM1016 above but without infrared link).
OM5027	I²C-bus evaluation board for low-voltage, low-power ICs & software

17.2 Development tools for 68000-based systems

Product	Description
OM4160	Microcore-1 demonstration/evaluation board: SCC68070, 128K EPROM, 512K DRAM, I²C, RS-232C, VSC SCC66470, resident monitor
OM4160/3	Microcore-3 demonstration/evaluation board: 128K EPROM, 64K SRAM, I²C, RS-232C, 40 I/O (inc. 8051-compatible bus), resident monitor
OM4160/3QFP	Microcore-3 demonstration/evaluation board for 9XC101 (QFP80 package)

17.3 Development tools for all systems

Product	Description
OM1022	I²C-bus analyzer. Hardware and software (runs on IBM or compatible PC) to experiment with and analyze the behaviour of the I²C-bus (includes documentation)

18.0 SUPPORT LITERATURE

Data handbooks	Ordering code
Semiconductors for radio and audio systems IC01a 1995 IC01b 1995	 9398 652 61011 9398 652 62011
Semiconductors for television and video systems IC02a 1995 IC02b 1995 IC02c 1995	 9398 652 63011 9398 652 64011 9398 652 65011
Semiconductors for telecom systems IC03 1995	 9398 652 66011
Display drivers and microcontroller peripherals IC12	 planned
8048-based 8-bit microcontrollers IC14 1994	 9398 652 40011
RF/wireless communications IC17 1994	 9398 652 60011 98-2000-290-05 (USA)
Semiconductors for in-car electronics and general industrial electronics IC18	 planned
80C51-based 8-bit microcontrollers IC20 1994	 9398 652 70011 98-8080-390-03 (USA)
68000-based 16-bit microcontrollers IC21	 planned
ICs for multimedia systems IC22 1995	 planned
Desktop video data handbook	9398 652 84011
Brochures/leaflets/lab. reports	
I²C-bus compatible ICs and support overview	9398 706 38011
I²C-bus control programs for consumer applications	9398 380 30011
Microcontrollers, microprocessors and support overview	9398 706 37011
Application notes for 80C51-based 8-bit microcontrollers	9398 652 57011
OM5027 I²C-bus evaluation board for low-voltage, low-power ICs & software	9398 706 98011
P90CL301 I²C driver routines	AN94078
User manual of Microsoft Pascal I²C-bus driver (MICDRV4.OBJ)	ETV/IR8833
User's guide to I²C-bus control programs	ETV8835

19.0 APPLICATION OF THE I²C-BUS IN THE ACCESS.bus SYSTEM

The ACCESS.bus (bus for connecting ACCESSory devices to a host system) is an I²C-bus based open-standard serial interconnect system jointly developed and defined by Philips and Digital Equipment Corporation. It is a lower-cost alternative to an RS-232C interface for connecting up to 14 inputs/outputs from peripheral equipment to a desk-top computer or workstation over a distance of up to eight metres. The peripheral equipment can be relatively low speed items such as keyboards, hand-held image scanners, cursor positioners, bar-code readers, digitizing tablets, card readers or modems.

All that's required to implement an ACCESS.bus is an 8051-family microcontroller with an I²C-bus interface, and a 4-wire cable carrying a serial data (SDA) line, a serial clock (SCL) line, a ground wire and a 12 V supply line (500 mA max.) for powering the peripherals.

Important features of the ACCESS.bus are that the bit rate is only about 20% less than the maximum bit rate of the I²C-bus, and the peripherals don't need separate device drivers. Also, the protocol allows the peripherals to be changed by 'hot-plugging' without re-booting.

As shown in Fig.39, the ACCESS.bus protocol comprises three levels: the I²C-bus protocol, the base protocol, and the application protocol.

The base protocol is common to all ACCESS.bus devices and defines the format of the ACCESS.bus message. Unlike the I²C-bus protocol, it restricts masters to sending and slaves to receiving data. One item of appended information is a checksum for reliability control. The base protocol also specifies seven types of control and status messages which are used in the system configuration which assigns unique addresses to the peripherals without the need for setting jumpers or switches on the devices.

The application protocol defines the message semantics that are specific to the three categories of peripheral device (keyboards, cursor locators, and text devices which generate character streams e.g. card readers) which are at present envisaged.

Philips offers computer peripheral equipment manufacturers technical support, a wide range of I²C-bus devices and development kits for the ACCESS.bus. Hardware, software and marketing support is also offered by DEC.

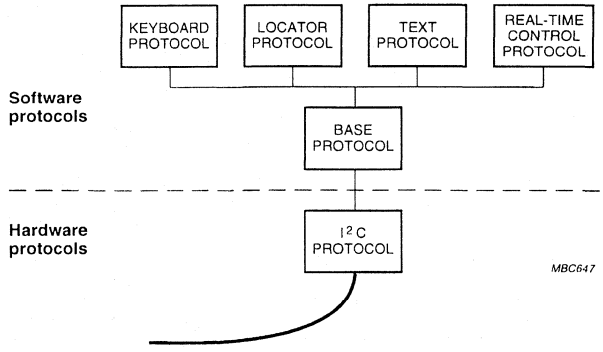


Fig.39 ACCESS.bus protocol hierarchy

EMBEDDED SYSTEMS

Programming the I²C Interface

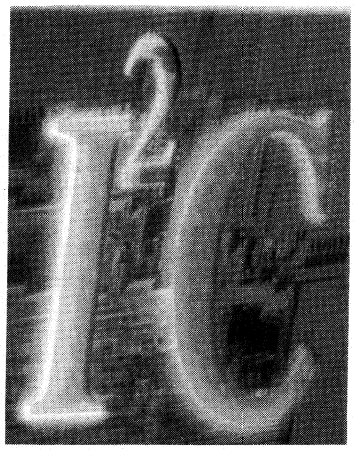
When intelligent devices need to communicate

Mitchell Kahn

The Inter-Integrated Circuit Bus ("I²C Bus" for short) is a two-wire, synchronous, serial interface designed primarily for communication between intelligent IC devices. The I²C bus offers several advantages over "traditional" serial interfaces such as Microwire and RS-232. Among the advanced features of I²C are multimaster operation, automatic baud-rate adjustment, and "plug-and-play" network extensions.

Mention the I²C bus to a group of American engineers and you'll likely get hit with an abundance of blank stares. I say American engineers because until recently the I²C bus was primarily a European phenomenon. Within the last year, however, interest in I²C in the United States has risen dramatically. Embedded systems designers are realizing the cost, space, and power savings afforded by robust serial interchip protocols.

The idea of serial interconnect between integrated circuits is not new. Many semiconductor vendors offer devices designed to "talk" via serial links with other processors. Current examples include Microwire (National Semiconductor), SPI (Motorola), and most recently Echelon's Neuron chips. In all cases, the goal is the same: to reduce the wiring and pincount necessary for a parallel data bus. It simply does not make economic sense to route a full-speed parallel bus to a slow peripheral.



Unfortunately for most serial-bus-capable devices, the choice of a bus protocol will dictate the CPU architecture. For example, only two CPU architectures implement an on-chip I²C port. If your choice of architecture precludes use of these architectures, then your only option is to implement the protocol in software.

The software implementation of the I²C protocol discussed in this article came about as a result of an implicit challenge during a staff meeting. One of our managers proposed that we hire a consultant to write a software I²C driver for the Intel 80C186EB embedded processor. Being somewhat new to the group, I took exception (although not verbally!) to his suggestion. A weekend of intense hacking later, I presented the first prototype of the driver. My reward? I got to write a generic version of the driver for general distribution.

Design Trade-offs

Three distinct tasks are involved in implementing the I²C protocol: watching the bus, waiting for a specific amount of time, and driving the bus. This became apparent when I flowcharted 1 byte of a typical bus transaction; see Figure 1. The time delays associated with creating the bus waveforms would normally have been relegated to the 80C186EB's on-chip timers. I could not, however, assume that the end users of my code would be able to spare a timer for the software I²C port. I had to forego the elegance (and to some extent accuracy) of the on-chip timers for the sledgehammer approach of software timing loops. Luckily, the I²C protocol is extremely forgiving with regard to timing accuracy. The decision to use assembly instead of a high-level language stemmed directly from the need to control program-execution time. I had neither the time nor the inclination to hand-tune high-level code.

Having made the decision to use assembly language, I faced my next problem: Could I make the code portable? Intel offers a plethora of CPU and embedded-controller architectures. Would it be possible to make the code somewhat portable between disparate assembly languages? I found my answer in the use of macros.

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All the basic building blocks of the I²C protocol (watching, waiting, and doing) can be compartmentalized into distinct macros. The algorithms that make up the I²C driver are written with these macros as the framework. You don't need to understand the intricacies of the I²C protocol to port these routines—you just need to know how to make your CPU watch, wait, and do.

For example, a 4.7_uS delay is a common event during a transfer. The macro *%Wait_4_7_uS* implements just such a delay by using the 8086 LOOP instruction with a couple of NOPs for tuning; see Example 1(a). Total execution time is readily calculated from instruction timing tables. The same macro is ported to the i960 architecture in Example 1(b). Although I am a neophyte when it comes to i960 programming, I had no problems porting the core macros.

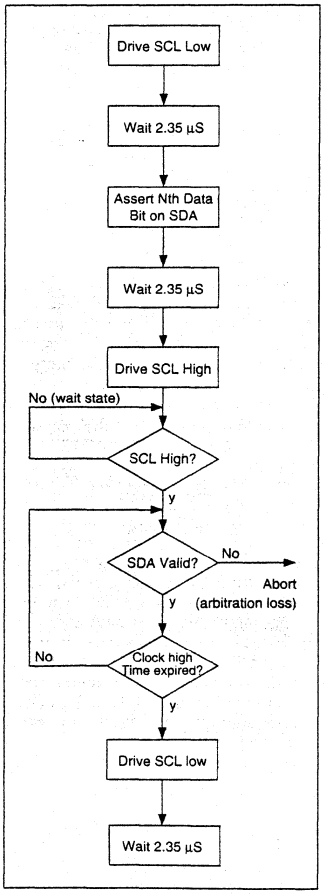


Figure 1: *Flowchart of process for transmission of a single bit.*

Hardware Dependencies

A few words about the target hardware are in order before I discuss the code. Any implementation of the I²C protocol requires two open-drain (or open-collector), bidirectional port pins for the Serial Clock (SCL) and Serial Data (SDA) lines. The code in this article was designed for the 80C186EB embedded processor, which has two open-drain ports on-chip. The two pins, P2.6 (SCL) and P2.7 (SDA), are part of a larger 8-bit port. Processors without open-drain I/O ports can easily implement I²C with the addition of an external open-collector latch.

Two special-function registers, P2PIN and P2LTCH, are used to read and write the state of the port pins. The 80C186EB allows the special-function registers to be located anywhere in either memory or I/O space. For this implementation, I chose to leave the registers in I/O space, even though this limited my choice of instructions. The 80186 architecture does not provide for read-modify-write instructions in I/O space (an AND to I/O, for example); it can only load and store (IN and OUT). So why did I limit myself? Again, I had to assume the lowest common denominator for our customers when designing my code.

Building the Framework

Early on in development, I decided to partition my code macros according to physical processes involved in the I²C protocol. Code not directly involved in mimicking the actions of a hardware I²C port was not written as macros. For example, the code necessary to access the stack frame is not written as a macro, whereas the code needed to toggle the clock line is. This was done to isolate architecture-dependent code sequences from the more generic I²C functions. Macros were also not used for "gray areas" such as the shifting of serial data, which is both architecture dependent and physical in nature. The I²C functions that passed the litmus test fell into the three aforementioned categories of watching, waiting, and doing.

The "waiting" macros provide a fixed-minimum time delay. They are implemented using a simple LOOP $ delay. The LOOP instruction decrements the CX register, then branches to the target (in this case itself) if the result is nonzero. The delay is (n−1)*15+5 clocks, where n is the starting value in the CX register. All the delays were calculated assuming a 16-MHz clock rate (62.5 nanoseconds per clock). The code still works at lower CPU speeds because the I²C protocol only specifies minimum timings. In fact, the delay macros are only "accurate enough," providing timings as close as I could get to the specified minimum without undue tuning.

The "watching" macros are "spin-on-bit" polling loops. These pieces of code wait for a transition on the appropriate I²C line to occur before allowing execution to continue. There are two polling macros for each of the two I²C signal lines; one for high-to-low transitions and one for low-to-high transitions. The

(a)

```
%*DEFINE(Wait_4_7_uS)(
        mov     cx, 5           ; 4 clocks
        loop    $               ; 4*15+5 = 65 clocks
        nop                     ; 3 clocks
        nop                     ; 3 clocks
                                ; total = 75 clocks
                                ; 75 * 62.5ns = 4.69uS (close enough)

        )
```

(b)

```
define(Wait_4_7_uS,'

        lda     0x17, r4        # instruction may be issued in parallel
                                # so assume no clocks.
0b:     cmpdeco 0, r4           # compare and decrement counter in r4
        bne.t   0b              # if !=0 branch back (predict taken
                                # branch)
                                #
                                # The cmpdeco and bne.t together take 3
                                # clocks in parallel minimum.
                                #
                                # 0x17 (25 decimal) * 3 = 75 clocks
                                # at 16MHz this is 4.69uS
')
```

Example 1: *(a) 80C186 implementation of 4.7_uS wait macro; (b) 80960CA implementation of 4.7_uS wait macro.*

polling of the SCL line that gives rise to an important feature of I²C: automatic, bit-by-bit baud-rate adjustment. Any device on the I²C bus may hold the clock line low in order to stall the bus for more time (a serial wait state). The other devices on the bus are then forced to poll the SCL line until the slow device releases control of the clock.

The *%Get_SDA_Bit* macro also falls under the category of "watching." Its function is simply to return the state of the SDA line without waiting for a transition. *%Get_SDA_Bit* is used primarily to pull the serial data off the bus when the clock is valid.

The "doing" macros control the state of the clock and data lines. As with the polling macros, there are four types—one for each transition of the SCL or SDA lines. The "doing" macros are named to reflect the physical operations they perform. For example, *%Drive_SCL_Low* always drives the SCL line to a low state. *%Release_SCL_High*, on the other hand, relinquishes control of the SCL line, which may then be pulled high or driven low by another device on the bus. A read-modify-write operation is used for the bit manipulation so that the other 6 bits of Port 2 are not affected by the I²C operations.

Getting on the Bus

Three procedures were created using the macro framework. I'll describe only the master transmit (Listing One, page 106) and master receive functions (Listing Two, page 108), as they represent the needs of most I²C users. The slave procedure is long and intricate and will not be described here.

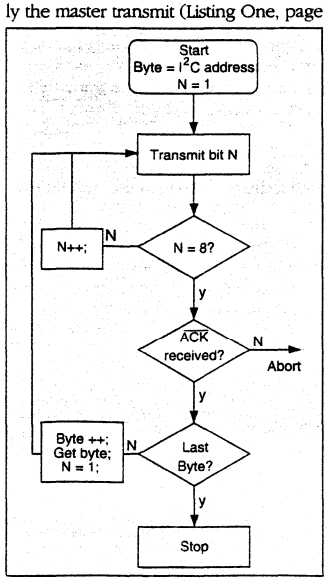


Figure 2: *Flowchart for I²C transmit procedure.*

An I²C master transmission proceeds as follows:

1. The master polls the bus to see if it is in use.
2. The master generates a start condition on the bus.
3. The master broadcasts the slave address and expects an acknowledge (ACK) from the addressed slave.
4. The master transmits 0 or more bytes of data, expecting an ACK following each byte.
5. The master generates a stop condition and releases the bus.

The stack frame for the master transmit procedure, I2CXA.A86, includes a far pointer to the message for transmission, the byte count for the message, and the slave address. Far pointers and far procedure calls are used in all the procedures. No attempt was made to conform to a specific high-level language calling convention, although such a conversion would be trivial. The procedures save only the state of the modified segment registers.

The master transmit procedure performs error checking on the passed parameters before attempting to send the message. The maximum message length is set at 64 Kbytes by the segmentation of the 80186 memory space. This restriction could be removed by including code to handle segment boundaries. The transmit procedure also checks the direction bit in the slave address to ensure that a reception was not erroneously indicated. Errors are reported back to the calling procedure through the AX register. (The exact code is in Listing One.)

The first step in sending a message is getting on the I²C bus. The macro *%Check_For_Bus_Free* simply polls the bus to determine if any transactions are in progress. If so, the transmit procedure aborts with the appropriate error code. If the bus is free, a start condition is generated. The start condition is defined as a high-to-low transition of SDA with SCL high followed by a 4.7_uS pause. These waveforms are easily generated with the *%Drive_SDA_Low* and *%Wait_4_7_uS* macros.

All communication on the I²C bus between the stop and start conditions, including addressing and data, takes place as an 8-bit data value followed by an acknowledge bit. This lead to the natural nested loop structure for the body of the procedure; see Figure 2.

The inner loop is responsible for transmitting the 8 bits of each data byte. Each transmitted bit generates the appropriate data (SDA) and clock (SCL) waveforms while checking for both serial wait states and potential bus collisions. A bus collision occurs when two masters attempt to gain control of the bus simultaneously. The I²C protocol handles collisions with the simple rule: "He who transmits the first 0 on the SDA line wins the bus." To ensure that we (the master transmit procedure) own the bus, the SDA line is checked whenever transmitting a 1. If a 0 is present, then a collision has occurred (because another master is pulling the line low), and the transfer must be aborted.

Three distinct tasks are involved in implementing the I²C protocol: watching the bus, waiting for a specific amount of time, and driving the bus

Control is turned over to the outer loop after the 8 bits of data (or address) have been transmitted. The outer loop immediately checks for an acknowledge from the addressed slave. The transfer is aborted if an acknowledge is not received. At the end of the ACK bit the message length counter is decremented. Control is returned to the inner loop if more data remains, otherwise a stop condition is generated and the master transmit procedure terminates.

Registers are used for intermediate result storage throughout the body of the procedure. For example, the AH register is used to hold the current value (either address or data) being shifted onto the SDA line. This eliminates the need for local data storage within the procedure.

On the Receiving End

The steps involved in an I²C master receive transaction are almost identical to those in transmission:

1. The master polls the bus to see if it is in use.
2. The master generates a start condi-

tion on the bus.
3. The master broadcasts the slave address and expects an ACK from the addressed slave.
4. The master receives 0 or more bytes of data and sends an ACK to the slave after each byte. The master signals the last byte by not sending an ACK.
5. The master generates a stop condition and releases the bus.

A far pointer to the receive buffer is passed on the stack to the master receive procedure. The remainder of the parameters—slave address and message count—are identical between the two procedures. The received message length is fixed at 64 Kbytes, again because of segmentation. The error-checking, bus-availability sensing, and start-condition generation sections of the receive procedure are lifted verbatim from the transmit code.

The structure of the receive procedure differs slightly once the start condition has been generated; see Figure 3. The slave address is transmitted using one iteration of the transmit procedure's outer loop. Control is passed to the receive loop once the slave acknowledges its address.

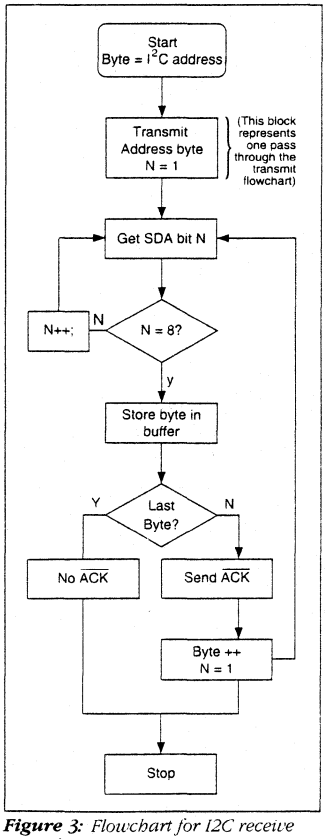


Figure 3: *Flowchart for I2C receive procedure.*

The receive loop structure is patterned after that of the transmit procedure. The inner loop controls the clocking of the SCL line and the shifting of the serial data off the SDA line into the CPU. Eight iterations of the inner loop are performed to receive each byte. The outer loop stores the received byte in the buffer, decrements the byte count, then sends an ACK to the slave. The last data byte is signalled by not sending an ACK.

Using the Procedures

Listing Three (page 110) shows a short program that uses both the master transmit and master receive procedures. The call to procedure I2C_XMIT displays the word "bUS-" on a four-character, seven-segment display controlled by the SAA1064 I²C compatible display driver. The time of day is read from the PCF8583 real-time clock by the call to procedure I2C_RECV.

Please note that interrupts must be disabled during the execution of both procedures. An interruption at an inopportune time (when the master is not in control of the clock) could cause the bus to hang. If you need to service interrupts periodically, then enable them only when the clock is driven low.

These procedures have been tested on a wide array of I²C devices ranging from serial EEPROMs to voice synthesizers. No compatibility problems have been seen to date.

Enhancing the Code

I've kicked around many ideas for enhancing the I²C procedures. You could, for example, replace the timing loops with timed interrupts. That way, the CPU could perform useful work during the pauses. Along the same lines, the pauses could be scheduled using a real-time kernel, again improving CPU throughput. Finally, you could add a high-level language calling structure.

The use of timed interrupts adds an order of magnitude to the complexity of the code, but would be worth it for high-performance, real-time systems.

All the basic building blocks of the I²C protocol (watching, waiting, and doing) can be compartmentalized into distinct macros

Conclusion

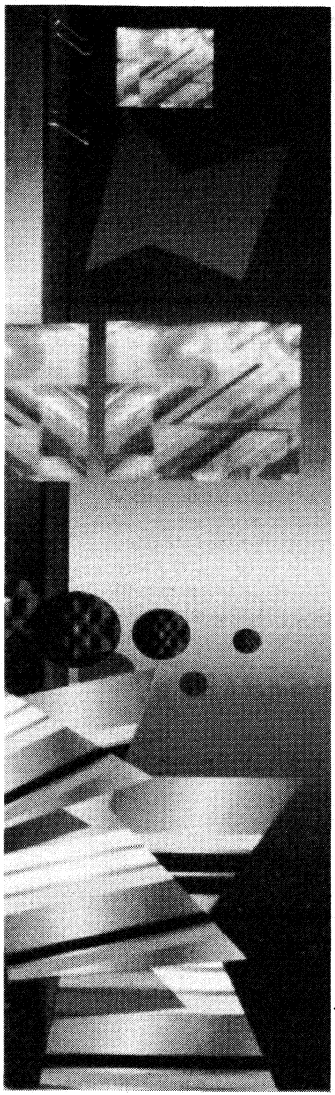
I²C is not the only game in town when in comes to serial protocols. Hopefully, some of the techniques presented here will carry over into the development of other "simulated" serial protocols, such as those targeted at the home-automation market. Who knows, maybe someday a snippet of my code may find its way into a truly intelligent dishwasher. I'll be waiting....

References

I²C Bus Specification, Philips Corporation (undated).

DDJ

Exploring I²C



FirstGraphics

Serial data buses are a well-proven tool in embedded systems. When you are communicating with slow peripheral devices, serial buses are often often more convenient and less expensive than parallel buses. Additionally, a serial interface featuring a UART or similar intermediary chip can also serve to isolate the CPU from noise and line glitches that might bring down the house if they were to occur on the processor bus. Peripherals can usually be controlled over a much greater distance by a serial bus. The serial approach offers greater resilience and noise immunity.

The price you pay for the convenience is a slower transmission rate and, possibly, the need for added interface circuitry at higher voltages. Many peripheral devices, however, are not in constant communication with the CPU and are not greatly affected by a slower bus. On the hardware side, any added interface circuitry required for serial-bus support is frequently compensated for by the resulting simplicity and tighter pinout of the serial peripherals.

CHOOSING THE PROPER ROUTE

Having decided that a serial bus makes sense for your application, your next task is to select the most appropriate bus and protocol. Here, as with rapid transit, your choice should be determined by your destination. Contrary to what some people may tell you, the choice of bus and protocol depends at least as much on the nature of the system's software as it does on the manufacturer's data sheets.

Consider, for example, the serial-peripheral interface (SPI) and multidrop serial buses. Both buses are popular, but each exhibits severly constrained performance in large networks. SPI, as embodied in the Motorola 6800 family, was designed primarily for one-on-one exchanges between two devices. Similarly, the multidrop approach used in various 8051 family members as well as in the 68HC11 and various UART chips finds its broadest expression in RS485/422 half-duplex transmissions. Multidrop has no deterministic arbitration scheme between multiple masters, leaving it mainly suitable for single-master multiple-slave situations. *(For more on multidrop, see Jack Woehr's article, "Multidrop Processing," Embedded Systems Programming, March 1990, pp 58-67—ed.)* A different approach is to use a three-wire protocol called MicroWire, available from National Semiconductor in Santa Clara, Calif., which is fine for use with addressable peripherals, but requires an individual chip select for each device ad-

The choice of bus and protocol depends at least as much on the system's software as it does on the manufacturer's data sheets.

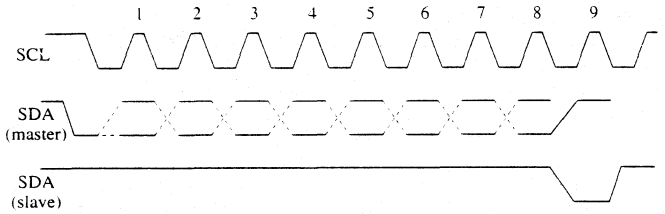
Exploring I²C

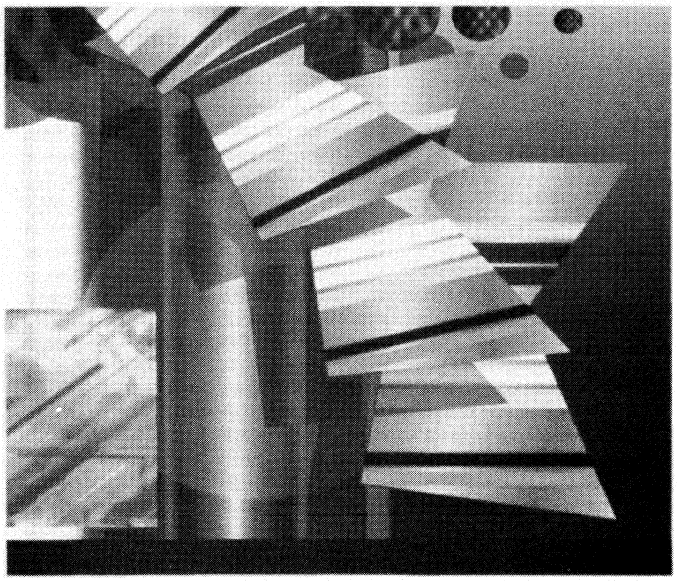
dressed. The added wiring offers no advantage to developers, and the bus offers nothing towards achieving multiple-mastering capabilities.

One of the more versatile options available to developers is the I²C bus promulgated by Philips/Signetics in Sunnyvale, Calif. I²C allows you to set up a multiple-master, multiple-slave communications bus with conflict arbitration, using only twisted-pair wiring to connect the processors and peripherals. Philips/Signetics has moved to support this protocol (which is quite popular in Europe) with a large assortment of interesting doodads, and is actively encouraging other manufacturers to join in the fun. If your next design features a microprocessor that supports I²C or you are prepared to implement I²C in software using a PIA as this article illustrates, your reward could be a decreased chip count and lower power consumption—along with a comfortable distributed-programming model for peripheral devices.

Open-collector configuration means that the output stage can only pull the node to ground.

Figure 1
Generation of acknowledge.





I²C is more flexible than the protocols noted above, since only two wires are required to service a large network of addressable masters and addressable slaves. A third wire may be added if interrupt service is required, though Philips/Signetics microprocessors featuring I²C support feature on-chip circuitry and are capable of interrupting the processor upon receipt of a valid address.

HOW I²C WORKS

The I²C bus consists of two lines: serial clock (SCL) and serial data (SDA). The beauty of the I²C bus is that each of these lines is bidirectional. Bidirectional means that everything on the bus is equal, unlike most other serial-peripheral busses such as SPI or MicroWire, which have dedicated inputs and outputs. Each I²C transaction line (SCL and SDA) is an open collector of output and input. The

pullup resistor is external.

Open-collector (actually, they are CMOS, so "open drain" is more appropriate) configuration means that the output stage can only pull the node to ground. A passive resistor pulls the node high, which means that any number of open collector outputs can be connected together with no deliterious results, because it is impossible to pull more current through the resistor than any one output will produce. Tying outputs together will produce disastrous results if the same procedure is tried with standard TTL outputs. If some of the outputs go high and some are low, the current is unlimited and the logic level of the output will be in an indeterminate state. Tying open-collector outputs together is also known as "wire ORing" because if either A or B goes low, so does the single-output line.

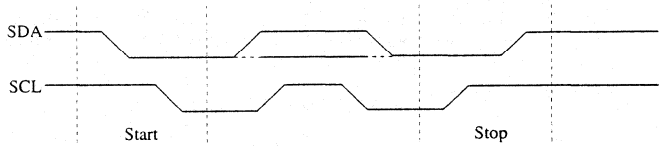
The I²C bus speed is specified at a maximum SCL rate of 100kHz SCL, which, admittedly, is not blazingly fast. The speed limit stems from the meager ability of a pullup resistor to source current to a long distributed line of peripherals. The 10-microsecond period allows plenty of time to charge the parasitic capacitance of the wires. (The maximum specified wire capacitance is 400 pF.)

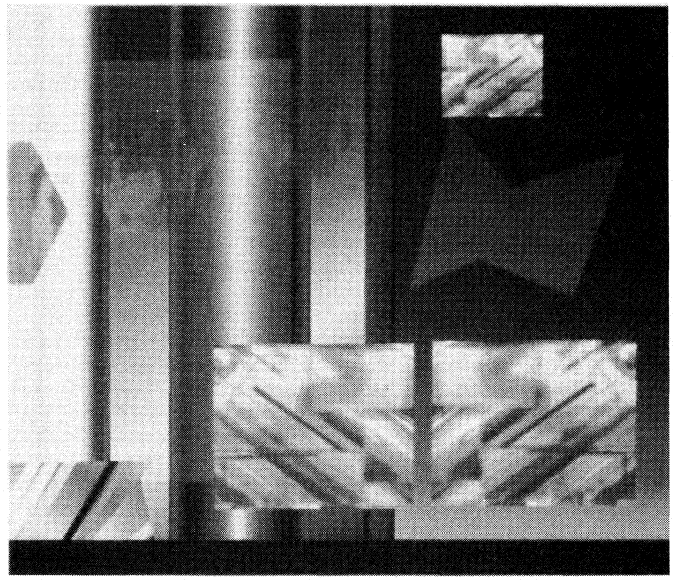
PUTTING IT TOGETHER

Although I²C supports multiple-master operation, here we use single-master, single-slave transactions to keep the example code simple. The master, as you might imagine, is defined as the unit that initiates the data transfer and generates the SCL signal. (In a multimaster system, each master would be responsible for generating its own SCL signal.) In our example, based strongly on the design of one of our company's single-board computers, the processor doesn't directly support I²C. Instead, we've implemented the I²C bus using a couple of the pins on an 8255 peripheral I/O chip. Consequently, the bulk of the example application code is simple setup and housekeeping routines. *(Steven R. Wheeler's example application listing was a bit too long to run in this issue. Interested readers may download it from the library 12 of CLMFORUM on CompuServe or from the* Embedded Systems Programming *bulletin board service at (415) 905-2689—ed.)*

By definition, a slave can be any processor or peripheral that responds to the master. Slaves all have unique, 7-bit addresses that are based on the device type and the wiring of address pins on the chip. All I²C peripherals have the top nibble of an address built in. For the PCF8574 I/O-port expanders we're us-

Figure 2
Start and stop conditions.





Exploring I²C

ing as examples, the address is 0100*xxx*. The *xxx* indicates the address selected by the state of the three address pins on the peripheral.

I²C serial transactions are always eight bits of data from the transmitter followed by a ninth ACK bit from the receiver. The first step in any I²C data transfer is to send the address of the slave on the SDA line. This act might seem confusing, since we seem to be mixing 7-bit addresses with 8-bit data. In practice, it's quite easy to work with: addresses are always seven bits long, and the eighth bit is used to determine whether the operation is a read or a write. For example, upon transmitting 01000001 to the PCF8574, the slave, assuming it exists on the bus and is strapped to address 000, will respond with a low on the SDA line after the master has finished with its last (eighth) data bit. The master leaves the line high. If it doesn't find a slave with address 10000, the data line will remain high and a failed communication attempt can be detected.

If a slave is connected, it begins putting data on the SDA line as soon as it has detected that the eighth bit is set (which is a read request). The SDA line is driven to the data level when the SCL line is low. Data is read when SCL is high, so SDA must not change when SCL is high. This protocol leads to a simple definition of the start of an I²C transaction—SDA goes from high to low when the clock is high.

The end of a transaction is equally simple to detect: SDA goes from low to high when SCL is high. This cycle leaves SDA and SCL in the high state, which is necessary if any other open-collector I²C peripheral wants access to the bus. Figure 2 illustrates the start and stop conditions of an I²C bus transaction.

ADDITIONAL DESIGN ROUTES

As you've seen, the I²C protocol is easy to work with and relatively simple to implement, even if you're not using a processor that directly implements it. If you're not planning to use Philips/Signetics microprocessors with onboard I²C support (such as the 68070 or various members of the 8051 family), you can still use the wide variety of available peripheral chips.

The number of integrated circuits using the I²C serial bus is increasing all the time. Application-oriented integrated circuits that support I²C include a voice sythesizer, a transcoder for IR remote control, several digital tuning circuits for computer-controlled television, several audio processors, PLL frequency synthesizers, tone generators, and frequency synthesizers. General-purpose integrated circuits using I²C include LCD drivers, digital-to-analog converters, SRAMs, EEPROMs, and a RAM clock/calender.

I²C is very popular in Europe, where Philips has been aggressively marketing this flexible method of extending peripheral support to control projects, and it is currently catching fire on this side of the Atlantic. It seems reasonable to expect that, given the burden of printed-wire requirements for embedded systems based on increasingly wider chip buses, more and more designers seeking economy of means will be attracted to the economy of I²C.

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EMBEDDED SYSTEMS PROGRAMMING, September 1991

BY MARK GARDNER

Bit-Banging Serial Ports

They say that necessity is the mother of invention, and it certainly seems to be the case in embedded systems work. No sooner do you accomplish the impossible in one project than your boss or customer asks you to do it again, only faster and cheaper this time. Even when you're working with low-cost microcontrollers, there's still that incentive to make things cheaper through magic software.

Performing miracles through software trickery is a skill that all embedded developers must cultivate. An opportunity for me to practice such tricks came in the form of a project using the Signetics 8x751 microcontroller. The 8x751 is an 8051 derivative that has no internal serial port—no attachment of SBUF shift registers to RxD and TxD, no diversion of timers to baud rate pacing, no serial interrupts. But the chip is low-priced and offers a small-footprint, and hence is desirable in many applications. Where the price or size outweighs the need for a simple serial port, one must be built out of firmware by appropriately controlling a single bit in a port. The practice is affectionately known as "bit-banging."

The approach I'll describe here has the advantages of being simple and fast. There is no transmit state-machine, no special provision for start and stop bits, and it takes less than two dozen machine cycles for each bit. It has a further advantage that the data doesn't need to be specially organized for transmitting. That is, the bits that are adjacent in the transmit data stream don't need to be adjacent when they are stored in memory. This solution is for a transmitter only, but I have used a similar procedure for receiving.

The shift (or rotate) operation is the first thing that comes to mind when you're designing code to provide a serial data output.

My project was required to operate at 9600 baud. This rate gives a per-bit time of 104 microseconds, or 104 cycles if you're using a 12-MHz part. The application in question had plenty of other activities as well as a serial port (such as reading a serial analog-to-digital converter, performing averages, and so on), so it was imperative that the serial port handling take an absolute minimum of time. Since I chose to execute in a fixed-time loop (to avoid interrupt overhead), it was also a goal that the code take a fixed amount of time regardless of the current transmit state.

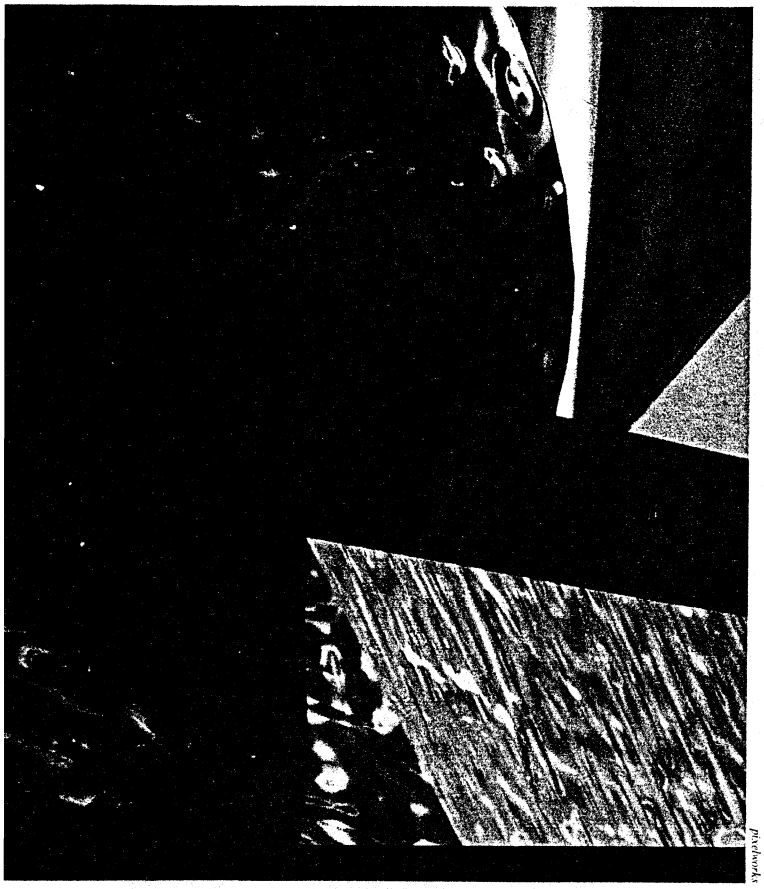
THE STRUCTURE POINTER SOLUTION

Generally, the shift (or rotate) operation is the first thing that comes to mind when you're designing code to provide a serial data output—the format of the data suggests such a scheme. With this approach, however, special states and a counter are needed to provide the start and stop bits and to sequence through the set of bytes to be transmitted.

The method presented here provides an array of structures (in the code or PROM space) that defines the transmit sequence bit by bit and uses a pointer to this array as the only controlling element. This means that only two bytes of scarce internal RAM is used.

The structures are referenced consecutively. Each gives the source of a bit to be transmitted and a flag to indicate whether the pointer should be increased to point to a new bit. The transmission is terminated by having a structure that refers to an "idle" bit and does not increase the pointer. Transmission is initiated by changing the pointer to point to the first structure. Start and stop bits are not distinguished from data bits. The bit update portion of the code is constant-time, and the pointer update can be easily padded if necessary to achieve this part of the goal.

Franklin's C51 compiler was used for the work described here. The 8x751 does not support external RAM, so the small model is used. (If the transmit data resided in external RAM, the algorithm could be applied, but would be expected to take a little longer to execute.)



Photonica

THE DECLARATIONS

The structure that provides individual bit definitions is:

```
// transmit bit-reference structure
struct BR {
        unsigned char index ;
        unsigned char mask ;
        unsigned char bump ;
} ;
```

No memory is allocated by this definition—it is essentially a `typedef`. The actual allocation and initialization are provided by the definition (in a header file, send_seq.h, in this case) of the `BitRef` array:

```
code struct BR BitRef[41] = { ... } ;
```

where the details will be given in a moment. The pointer is defined as:

```
// pointer to BitRef structure array
data struct BR code *BR_ptr ;
```

In Franklin's C51, the declaration tokens are interpreted as follows. In the struct `BR` declaration, the token `code` assigns the `BitRef` array to program memory (which is then accessed with the `movc` instruction). In the `*BR_ptr` declaration, the token `code` implies that `BR_ptr` is exclusively a pointer to the program space, so it requires only two bytes to be completely defined. The token `data` causes the compiler to store the pointer value in

internal RAM. (Since I was using the small model, this would have been the default storage anyway.)

The index entry in each structure allows the serial bit to be selected from an array of bytes called transmit[4] in my case. The transmit array can, if desired, be set up to literally overlay all of the internal memory, so that the maximum "random access" can be achieved. This was not necessary in my case.

The physical port pin to be exercised is defined:

```
/*     transmit is on P3.3 */
sbit TransBit = 0xB3 ;
```

THE STRUCTURE INITIALIZATION

Each bit to be transmitted is defined by an index and mask. These are initialized in the BitRef structure so that characters can be formed as desired in the output bit stream. The index is the offset within the transmit array. The initialization in my case, for a sequence of 40 bits making up four characters, was:

```
code struct BR BitRef[41] = {
//  index   mask      bump    comment

    3 , b01000000 , 1,    //  0 start bit

    1 , b00000001 , 1,    //  D6
    1 , b00000010 , 1,    //  D7
    1 , b00000100 , 1,    //  D8
    1 , b00001000 , 1,    //  D9
    1 , b00010000 , 1,    //  D10
    1 , b00100000 , 1,    //  D11

    3 , b10000000 , 1,    //  1 fixed
    3 , b10000000 , 1,    //  1 fixed
    3 , b10000000 , 1,    //  1 stop bit

    3 , b01000000 , 1,    //  0 start bit
    ...
    ...
    ...
    3 , b01000000 , 1,    //  0 fixed
    3 , b10000000 , 1,    //  1 stop bit
    3 , b10000000 , 0     //  1 idle bit
} ;
```

(The "masks" are given in binary notation. [*See "A Binary Upgrade for C," pp. 60-62.—Ed.*] Because of my assembler and hardware background, this notation is natural for me in bit mask references.)

The "bump" is a flag that continues the transmission. When it finally reaches 0, the serial output sequence will stop.

The "index" refers, as mentioned, to the element of "transmit" in which the bit resides. Some initialization code has guaranteed that the upper two bits of transmit[3] will be 10, so that they can be referred to for start and stop bits and for any fixed-value bits that happen to be in the data stream (in my case, the fixed bits are used to indicate data byte order).

The "bump" is a flag that continues the transmission. When it is finally 0, the serial output sequence will stop.

THE CODE

The code fragment that accomplishes the transmission is:

```
(a) TransBit =
  (bit)( transmit[ BR_ptr->index ]
    & BR_ptr->mask ) ;
(b) if ( BR_ptr->bump )
  BR_ptr++ ;
```

The program sequence for section (a) looks like this:

```
BR_ptr->index
  -- looks up current index, then used in
transmit[index]
  -- to get byte with desired bit,
     then ANDed with mask
BR_ptr->mask
  -- to get zero/nonzero value, which
(bit)(value & value)
  -- is then cast to a bit for output
TransBit = bit
  -- to port pin, the ultimate goal.
```

The pointer is increased in (b), depending on the value of BR_ptr->bump. As indicated earlier, this is *always* one except in the last structure, so the serial transmission always proceeds to the defined end. The statement:

```
BR_ptr = &BitRef[40] ;
```

in initialization will keep the transmitter off during startup, and:

```
BR_ptr = BitRef ;
```

is used to initiate a transmission sequence.

Bit-Banging Serial Ports

The previous transmitting code compiles, with only a little manual assistance, to:

```
; TransBit = (bit)( transmit[
  BR_ptr->index ] & BR_ptr->mask ) ;
    MOV     DPL,BR_ptr+01H
    MOV     DPH,BR_ptr
    CLR     A
    MOVC    A,@A+DPTR
    ADD     A,#transmit
    MOV     R0,A
    MOV     A,@R0
    MOV     R7,A
    INC     DPTR
    CLR     A
    MOVC    A,@A+DPTR
    ANL     A,R7
    ADD     A,#0FFH
    MOV     TransBit,C
; if ( BR_ptr->bump )
    INC     DPTR
    CLR     A
    MOVC    A,@A+DPTR
    JZ      ?C0011
;     BR_ptr++ ;
    MOV     A,#03H
    ADD     A,BR_ptr+01H
    MOV     BR_ptr+01H,A
    CLR     A
    ADDC    A,BR_ptr
    MOV     BR_ptr,A
?C0011:
```

The assembly language code reveals that the mechanism is pretty efficient. This method is in use in one of my clients' products and has proved effective.

BIT-BANGING WORKS

This bit-banging solution serves to provide serial transmission in an embedded system that has no hardware specifically dedicated to the function. Although alternate and more traditional solutions would have worked, the need for speed encouraged development of a code-pointer-based solution that works fast enough in this case and takes up only two internal RAM bytes for operation. I hope that this presentation will prove to be useful for you.

Mark Gardner is a consultant based in Acton, CA. He has been designing hardware and writing firmware for embedded systems for over 15 years. He has an MS in electronic engineering from the University of Illinois.

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Philips Semiconductors
811 E. Arques Avenue
P.O. Box 3409
Sunnyvale, CA 94088-3409
(408) 991-3552

I²C-BUS DEVELOPMENT TOOLS FOR ALL SYSTEMS

OM1022

This Philips Semiconductors support tool, called the I²C-analyzer (or in the US, Port MSC) is a PC board that can be connected with a cable to the Centronics printer port via a 25-pin sub-D connector. The I²C has a 4-stake connector for convenient use in the laboratory. There are several "flavours" to this board, with the latest version supporting multimaster operation. A Philips 8400-series microcontroller executes the low-level I²C tasks on this board, and the Centronics port is used for two-way communications between the PC software and the microcontroller. Control programs for the Philips interface will run on any IBM-compatible PC. The software is mainly intended for interactive control of devices on the I²C-bus. The user can interactively construct, send and receive I²C messages. A database, which comes with the software, contains information about many specific devices, thus making operation is even easier for many Philips devices. The user is prompted to enter control data for the specific registers that are relevant to the device, and the software takes care of the routines by checking the validity of the input data and constructing the correct I²C message. An illustrated description of the internals of the controlled device and its status is available for some devices.

Currently, four programs are supplied with the OM1022 that provide various control options for specific and general purpose I²C devices.

I²C TV version 3.5
I²C radio version 2.6
I²C PLL version 2.3
I²C CELL version 1.5

The "Users Guide to I²C-bus Control Programs" and "The I²C-bus and how to use it" brochures are also included with each OM1022.

I²C/ACCESS.bus Monitor MIIC-101

The MIIC-101 is a stand-alone trouble shooting tool for the I²C and ACCESS.bus. When connected to an I²C-bus or ACCESS.bus network, the 101 bus monitor can collect, display or upload information on all bus activity. Its key features are:

- I²C and ACCESS.bus compatible
- operating modes: line status, forward/backwards trace, view and remote
- monitoring of all or selected bus addresses
- trace buffer stores up to 2700 messages
- easy to read alphanumeric display (byte, message and buffer scrolling)
- hand-held portable unit (battery, external supply or bus-powered)
- RS-232 port supports remote data capture and uploading.

The MIIC-101 is manufactured by:
Micro Computer Control Corporation
PO Box 275
17 Model Ave
Hopewell
New Jersey 08525
USA

Tel. +001 609 466 1751
Fax +001 609 466 4116

PF8681 I²C-bus and ACCESS.bus Analysis Support Package

The PF8681 has been designed for use with the PM3580 family of logic analyzers. It provides facilities for analyzing and troubleshooting data streams on the I²C-bus and ACCESS.bus.

Captured data from either bus can be displayed on a logical analyzer screen in various number systems. The PF8681 includes a disassembler for both the I²C-bus and ACCESS.bus. The adapter allows simultaneous measurements in the timing and state domain without any reconnection or multiple probing of the I²C signal lines. This single probing approach avoids additional DC and AC loading of the I²C and ACCESS.bus signal lines.

The I²C-bus disassembler supports all present day features of the I²C-bus system including 10-bit and "fast-mode". The ACCESS.bus disassembler supports the BASE-protocol specifications as mentioned in the ACCESS.bus specifications version 2.0.

The PF8681 I²C/ACCESS.bus package includes an adaptor, disassembler and special ACCESS.bus interface cable. Pricing and delivery is available from Fluke.

Calibre ICA-90 plug-in, half length IMB-PC compatible I²C adapter card

This PC card interfaces to the I²C-bus via a 9-pin D-connector. It is based on Philip's PCF8584 I²C-bus controller IC, which can interface the bus at high speeds. Calibre supplies the board with a library of I²C-control routines in both C and Turbo BASIC, which can be retrieved by the user's application software. These routines support both master and slave operation. The software is not interactive (i.e. users must write and compile their own programs) but the interface to the library routines is straightforward, and examples are supplied. They also supply a stand-alone monitor program with the ICA-90. This allows non-intrusive, real-time tracing of I²C-bus activity. Captured data is stored in PC memory and until the buffer is full, when the trace stops and the data is formatted and moved onto a disk file. Data presentation includes occurrences of Start, Stop and Acknowledge conditions. Users can display and analyze the data with any word processor or browsing program. The monitor program requires at least a 6 MHz 286-based PC or faster. This board is recommended for speed-critical or complex I²C-systems (i.e. Multimaster) due to its real-time monitor capability.

You can purchase the ICA-90 from Calibre Electronics Ltd, England, or Saelig Co., USA (see page on "Addresses of I²C-bus hardware manufactures").

I²C-BUS DEVELOPMENT TOOLS FOR 8048 AND 8051-BASED SYSTEMS

OM1016

I²C-bus demonstration board with microcontroller, LCD, LED, Par. I/O, SRAM, EEPROM, Clock, DTMF generator, AD/DA conversion, infrared link.

OM1018

Manual for OM1016.

OM1020

LCD and driver demonstration board.

OM4151

I²C-bus evaluation board (similar to OM1016 above but without infrared link).

OM5027

I²C-bus evaluation board for low-voltage, low-power ICs & software. (A fuller description of the OM527 evaluation board is included in this Data Handbook. See relevant section for details).

I²C-BUS DEVELOPMENT TOOLS FOR 68000-BASED SYSTEMS

OM4160

Microcore-1 demonstration/evaluation board: SCC68070, 128K EPROM, 512K DRAM, I²C, RS-232C, VSC SCC66470, resident monitor.

OM4160/3

Microcore-3 demonstration/evaluation board: 128K EPROM, 64K SRAM, I²C, RS-232C, 40 I/O (inc. 8051-compatible bus), resident monitor.

OM4160/3QFP

Microcore-3 demonstration/evaluation board for 9XC101 (QFP80 package).

ADDRESSES OF I²C-BUS HARDWARE MANUFACTURES

In Germany:
ART Automatisierung & Rechnertechnik GmbH
Johnann-Kraus Str. 8A
7770 Ueberlingen
Deutschland

Tel. +49 75514056
Fax +49 75514058

In United Kingdom:
Calibre Electronics Ltd
Broomfield House
Bolling Road
Bradford BD4 7BG
England

Tel. +44 1274 394125
Fax +44 1274 723861

In France:
COGEMA
B.P. 1515 - 87020 Limoges CEDEX
France

Tel. +33 55 383184
Fax +33 55 371639

In USA:
Saelig Co.
1193 Moseley Rd
Victor
New York 14564
USA

Tel. +001 716 425 3753
Fax +001 716 425 3835

DEVICE DATA

I²C bus extender 82B715

DESCRIPTION

The 82B715 is a bipolar integrated circuit intended for application in I²C bus systems.

While retaining all the operating modes and features of the I²C system it permits extension of the practical separation distance between components on the I²C bus by buffering both the data (SDA) and the clock (SCL) lines.

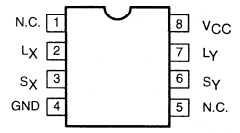
The I²C bus capacitance limit of 400pF restricts practical communication distances to a few meters. Using one 82B715 at each end of longer cables reduces the cable loading capacitance on the I²C bus by a factor of 10 times and may allow the use of low cost general purpose wiring to extend bus lengths.

FEATURES

- Dual, bi-directional, unity voltage gain buffer
- I²C bus compatible
- Logic signal levels may include both supply and ground
- X10 impedance transformation
- Wide supply voltage range

PIN CONFIGURATIONS

8-Pin Dual In-Line or SO
82B715



SU00290

PINNING

PIN	SYMBOL	FUNCTION
1	N.C.	
2	L_X	Buffered Bus, LDA or LCL
3	S_X	I²C Bus, SDA or SCL
4	GND	Negative Supply
5	N.C.	
6	S_Y	I²C Bus, SCL or SDA
7	L_Y	Buffered Bus, LCL or LDA
8	V_{CC}	Positive Supply

QUICK REFERENCE DATA

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.	MAX.	
V_{CC}	Supply voltage	4.5		12	V
I_{CC}	Quiescent current		16		mA
I_{line}	Output sink capability	30			mA
V_{in}	Input voltage range	0		V_{CC}	V
V_{out}	Output voltage range	0		V_{CC}	V
Z_{in}/Z_{out}	Impedance transformation	8	10	13	
T_{amb}	Temperature range	–40		+85	°C

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
8-Pin Plastic Dual In-Line (N/P) Package	P82B715P N	SOT97
8-Pin Plastic SOL (Small Outline Large) Dual In-Line (D/T) Package	P82B715T D	SOT96A
82B715 is available in chip form		

FUNCTIONAL DESCRIPTION

The 82B715 bipolar integrated circuit contains two identical buffer circuits which enable I²C and similar bus systems to be extended over long distances without degradation of system performance or requiring the use of special cables.

The buffer has an effective current gain of ten from I²C bus to Buffered bus. Whatever current is flowing out of the I²C bus side, ten times that current will be flowing into the Buffered bus side (see Figure 2).

As a consequence of this amplification the system is able to drive capacitive loads up to ten times the standard limit on the Buffered bus side. This current based buffering approach preserves the bi-directional, open-collector/open-drain characteristic of the I²C SDA/SCL lines.

To minimize interference and ensure stability, current rise and fall rates are internally controlled.

APPLICATION NOTES

By using two (or more) 82B715 ICs, a sub-system can be built which retains the interface characteristics of an I²C device so that it may be included in, or optionally added to, any I²C or related system.

The sub-system features a low impedance or "Buffered" bus, capable of driving large wiring capacities (see Figure 3).

I²C Systems

As with the standard I²C system, pull-up resistors are required to aprovide the logic HIGH levels on the Buffered bus. (Standard open-collector configuration of the I²C bus). The size and number of these pull-up resistors depends on the system.

If the buffer is to be permanently connected into the system, the circuit should be configured with only one pull-up resistor on the Buffered bus and none on the I²C bus.

Alternatively a buffer may be connected to an existing I²C system. In this case the Buffered bus pull-up will act in parallel with the I²C bus pull-up.

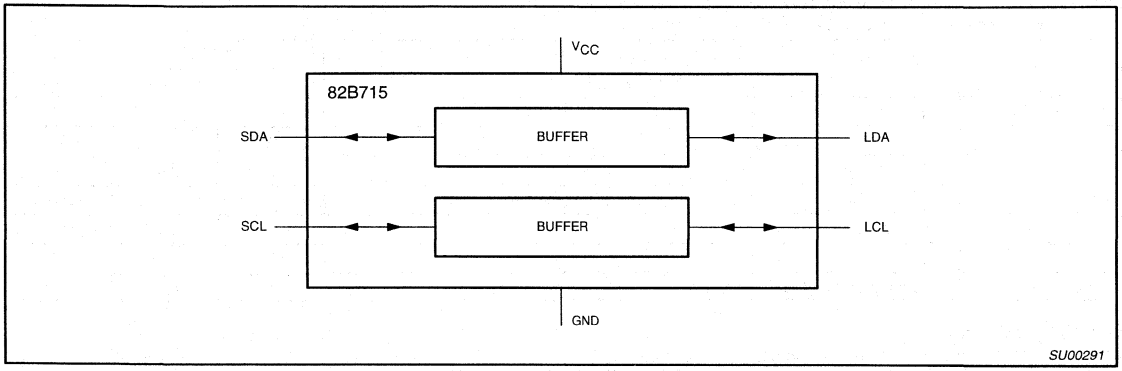


Figure 1. Block Diagram: 82B715

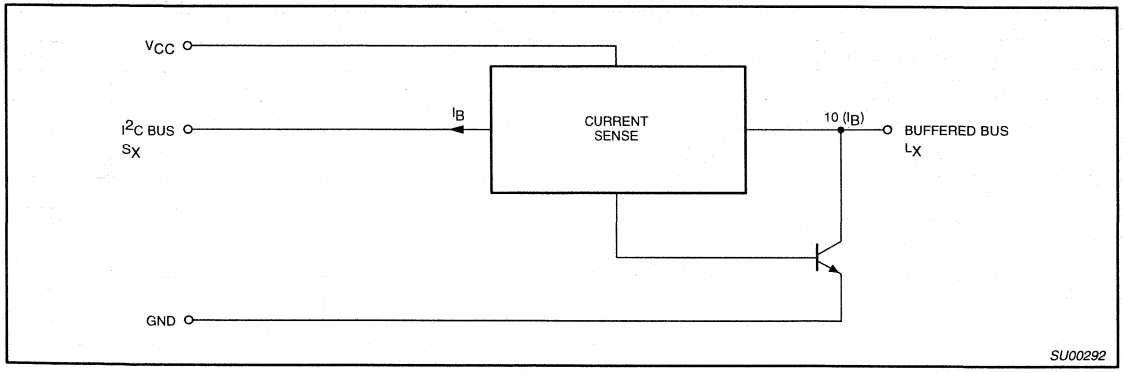


Figure 2. Equivalent Circuit: One Half 82B715

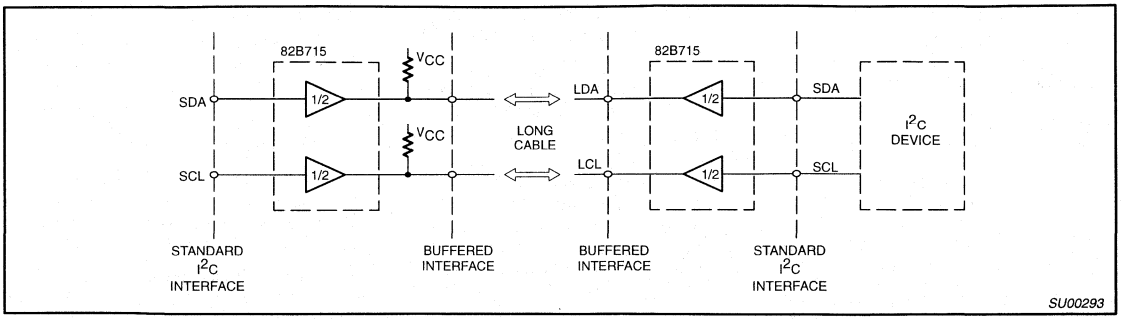


Figure 3. Minimum Sub-System with 82B715

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
Voltages with respect to pin GND (DIL-8 pin 4).

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN.	MAX.	
V_{CC} to GND	Supply voltage range V_{CC}	−0.3	+12	V
V_{bus}	Voltage range I²C Bus, SCL or SDA	0	V_{CC}	V
V_{buff}	Voltage range Buffered Bus	0	V_{CC}	V
I	DC current (any pin)		60	mA
P_{tot}	Power dissipation		300	mW
T_{stg}	Storage temperature range	−55	+125	°C
T_{amb}	Operating ambient temperature range	−40	+85	°C

CHARACTERISTICS

At T_{amb} = +25°C and V_{CC} = 5 Volts, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.	MAX.	
Power Supply					
V_{CC}	Supply voltage (operating)	4.5	—	12	V
I_{CC}	Supply current	—	16	—	mA
I_{CC}	Supply current at V_{CC} = 12V	—	22	—	mA
I_{CC}	Supply current, both I²C inputs LOW, both buffered outputs sinking 30mA.	—	28	—	mA
Drive Currents					
I_{Sx}, I_{Sy}	Output sink on I²C bus V_{Sx}, V_{Sy} LOW = 0.4V V_{Lx}, V_{Ly} LOW on Buffered bus = 0.3V	3	—	—	mA
I_{Lx}, I_{Ly}	Output sink on Buffered bus V_{Lx}, V_{Ly} LOW = 0.4V V_{Sx}, V_{Sy} LOW on I²C bus = 0.3V	30	—	—	mA
Input Currents					
I_{Sx}, I_{Sy}	Input current from I²C bus when I_{Lx}, I_{Ly} sink on Buffered bus = 30mA	—	—	3	mA
I_{Lx}, I_{Ly}	Input current from Buffered bus when I_{Sx}, I_{Sy} sink on I²C bus = 3mA	—	—	3	mA
I_{Lx}, I_{Ly}	Leakage current on Buffered bus V_{Lx}, V_{Ly} = V_{CC}, and V_{Sx}, V_{Sy} = V_{CC}	—	—	200	µA
Impedance Transformation					
Z_{in}/Z_{out}	Input/Output impedance	8	10	13	

Pull-Up Resistance Calculation
In calculating the pull-up resistance values, the gain of the buffer introduces scaling factors which must be applied to the system components. Viewing the system from the Buffered bus, all I²C bus capacitances have effectively 10 times their I²C bus value.

In practical systems the pull-up resistance is determined by the rise time limit for I²C systems. As an approximation this limit will be satisfied if the time constant (product of the net resistance and net capacitance) of the total system is set to 1 microsecond.

The total time constant may either be set by considering each bus node individually (i.e., the I²C nodes, and the Buffered bus node) and choosing pull-up resistors to give time constants of 1 microsecond for each node; or by combining the capacitances into an equivalent capacitive loading on the Buffered bus, and calculating the Buffered bus pull-up resistor required by this equivalent capacitance.

For each separate bus the pull-up resistor may be calculated as follows:

$$R = \frac{1\mu sec}{C_{device} + C_{wiring}}$$

Where: C_{device} = sum of device capacitances connected to each bus, and C_{wiring} = total wiring and stray capacitance on each bus.

If these capacitances are not known then a good approximation is to assume that each device presents 10pF of load capacitance and 10pF of wiring capacitance.

The capacitance figures for one or more individual I²C bus nodes should be multiplied by a factor of 10 times, and then added to the Buffered bus capacitance. Calculation of a new Buffered bus pull-up resistor will alllow this single pull-up resistor to act for both the included I²C bus nodes and the Buffered bus. Thus it is possible to combine some or all of these separate pull-up resistors into a single resistor on the Buffered bus (the value of which is calculated from the sum of the scaled capacitances on the Buffered bus). If the buffer is to be permanently connected into the system then all the separate pull-up resistors should be combined. But if it is to be connected by adding it onto an existing system, then only those on the additional I²C bus system can be combined onto the Buffered bus if the original system is required to be able to still operate on a stand-alone basis.

A further restriction is that the maximum pull-up current, with the bus LOW, should not exceed the I²C bus specification maximum of 3mA, or 30mA on the Buffered bus. The following formula applies:

$$30mA > \frac{V_{CC} - 0.4}{R_P}$$

Where: R_P = scaled parallel combination of all pull-up resistors.

If this condition is met, the fall time specifications will also be met.

Figure 4 shows typical loading calculations for the expanded I²C bus.

Sx, Sy, I²C Bus, SDA or SCL

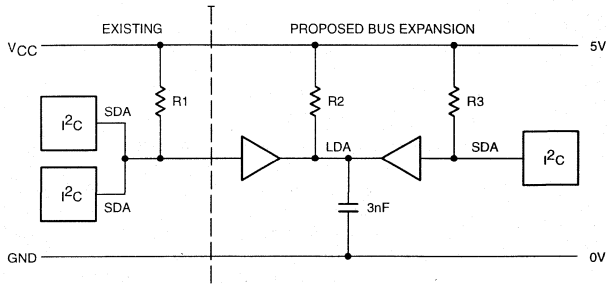
Because the two buffer circuits in the 82B715 are identical either input pin can be used as the I²C Bus SDA data line, or the SCL clock line.

Lx, Ly, Buffered Bus, LDA or LCL

On the buffered low impedance line side, the corresponding output becomes LDA and LCL.

V_{CC}, GND — Positive and Negative Supply Pins

In normal use the power supply voltages at each end of the low impedance line should be comparable. If these differ by a significant amount, noise margin is sacrificed.



EFFECTIVE CAPACITANCE NEAR I²C DEVICES

2 × I²C Devices	20pF
Strays	20pF
82B715 Buffer	10pF
TOTAL CAP.	50pF

I²C pull-up

$$R1 = \frac{1\mu sec}{50pF} = 20K\Omega$$

EFFECTIVE CAPACITANCE BUFFERED LINE

Wiring Cap.	3000pF
TOTAL CAP.	3000pF

Buffered Bus pull-up

$$R2 = \frac{1\mu sec}{3000pF} = 333\Omega$$

EFFECTIVE CAPACITANCE REMOTE I²C DEVICES

1 × I²C Devices	10pF
Strays	10pF
82B715 Buffer	10pF
TOTAL CAP.	30pF

I²C pull-up

$$R3 = \frac{1\mu sec}{30pF} = 33K\Omega$$

AS AN ADDITION TO AN EXISTING SYSTEM * :

R1 = 20KΩ

$$R2' = \frac{R2 \times 0.1R3}{R2 + 0.1R3} = 300\Omega$$

R3 not required since buffer always connected

FOR A PERMANENT SYSTEM * :

R1 not required since buffer always connected

$$R2' = \frac{0.1R1 \times R2 \times 0.1R3}{0.1R1 + R2 + 0.1R3} = 260\Omega$$

R3 not required since buffer always connected

*** NOTE:**
R1, R2 and R3 are calculated from the capacitive loading and a 1µsec time constant on each bus node. For an addition to an existing system, R2' (the new value for R2) is shown as being calculated from the parallel combination of R2 and the scaled value of R3; while for a permanent system R2, and scaled values of R1 and R3 have been used. Note that this example has used scaled resistor values and combined the node and cable capacitances.

CHECK FOR MAXIMUM PULL-UP CURRENT:

$$\frac{(5 - 0.4)V}{260\Omega} = 17.6mA < 30mA$$

SU00294

Figure 4. Typical Loading Calculation: I²C Bus with 82B715

128 × 8-bit EEPROM with I²C-bus interface PCA8581; PCA8581C

FEATURES

- Operating supply voltage:
  - 4.5 to 5.5 V (PCA8581)
  - 2.5 to 6.0 V (PCA8581C)
- Integrated voltage multiplier and timer for writing (no external components required)
- Automatic erase before write
- Low standby current; maximum 10 μA
- 8-byte page write mode
- Serial input/output bus (I²C-bus)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Designed for minimum 10000 write cycles per byte
- 10 years minimum non-volatile data retention
- Infinite number of read cycles
- Pin and address compatibility to PCF8570, PCF8571 and PCF8582
- Operating temperature: −25 to +85 °C.

GENERAL DESCRIPTION

The PCA8581 and PCA8581C are low power CMOS EEPROMs with standard and wide operating voltages:

4.5 to 5.5 V (PCA8581)

2.5 to 6.0 V (PCA8581C).

In the following text, the generic term 'PCA8581' is used to refer to both types in all packages except when otherwise specified.

The PCA8581 is organized as 128 words of 8-bytes.

Addresses and data are transferred serially via a two-line bidirectional bus (I²C-bus). The built-in word address register is incremented automatically after each written or read data byte. All bytes can be read in a single operation. Up to 8 bytes can be written in one operation, reducing the total write time per byte. Three address pins, A0, A1 and A2 are used to define the hardware address, allowing the use of up to 8 devices connected to the bus without additional hardware.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage				
	PCA8581		4.5	5.5	V
	PCA8581C		2.5	6.0	V
I_{DD}	supply current (standby)	f_{SCL} = 0 Hz	–	10	μA
T_{amb}	operating ambient temperature		−25	+85	°C
T_{stg}	storage temperature	without EEPROM retention	−65	+150	°C
		with EEPROM retention	−65	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCA8581P	8	DIP	plastic	SOT97-1
PCA8581CP	8	DIP	plastic	SOT97-1
PCA8581T	8	SO8	plastic	SOT96-1
PCA8581CT	8	SO8	plastic	SOT96-1

BLOCK DIAGRAM

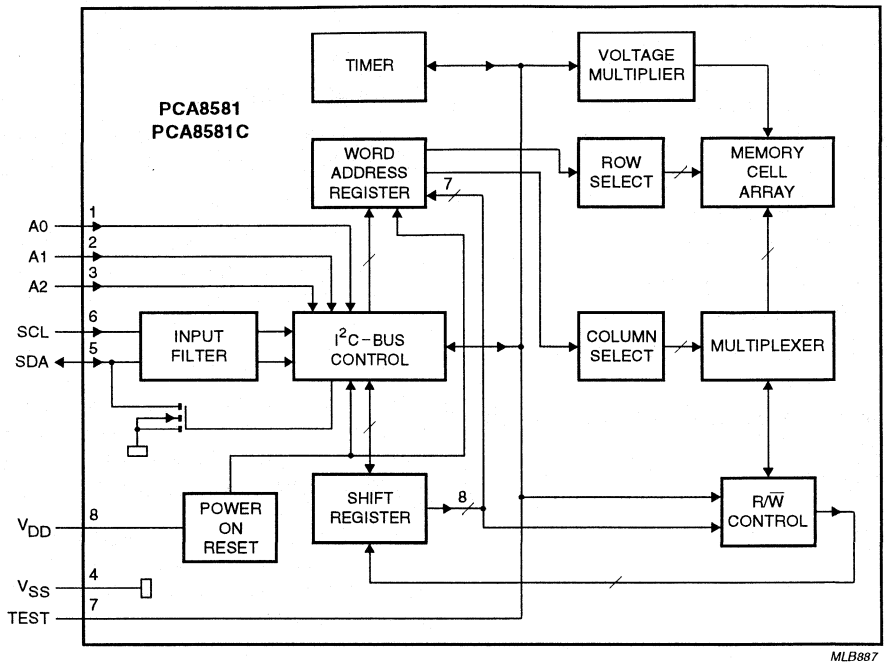


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	hardware address input 0
A1	2	hardware address input 1
A2	3	hardware address input 2
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
TEST	7	test output can be connected to V_{SS}, V_{DD} or left open-circuit
V_{DD}	8	positive supply

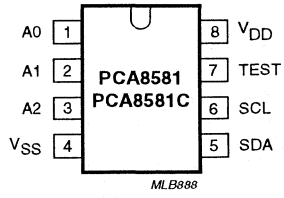


Fig.2 Pin configuration.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

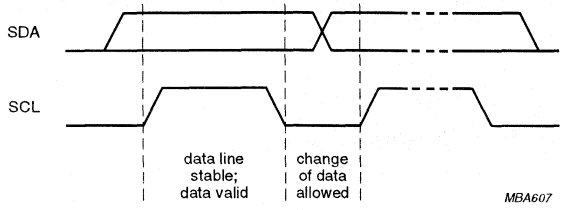


Fig.3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

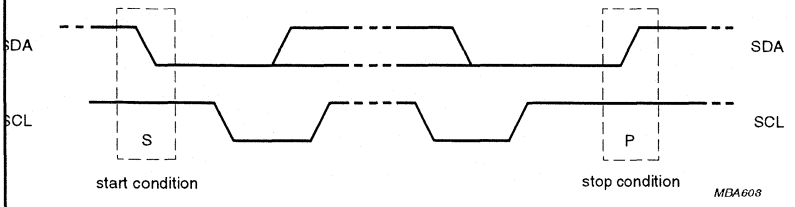


Fig.4 Definition of start and stop conditions.

System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

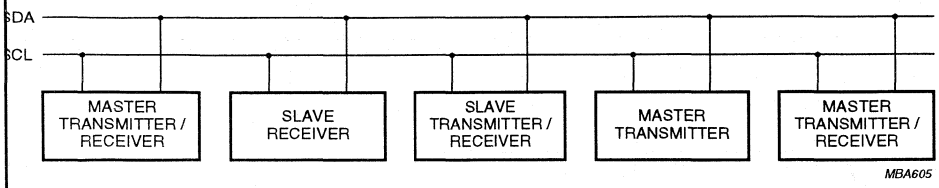


Fig.5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

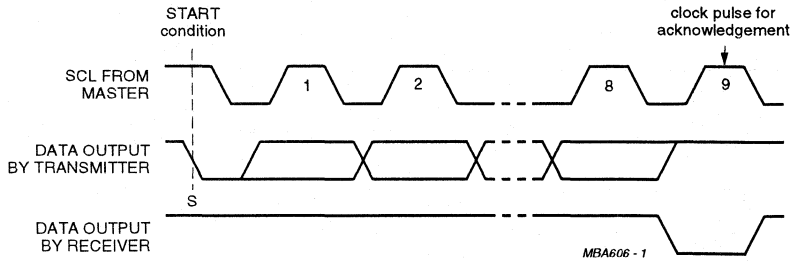


Fig.6 Acknowledgement on the I²C-bus.

I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCA8581 WRITE and READ cycles is shown in Figs 7, 9 and 10.

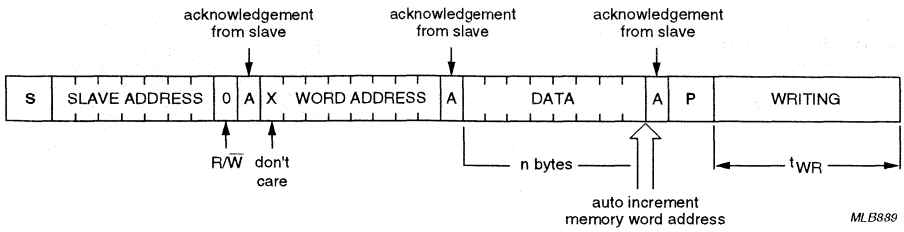
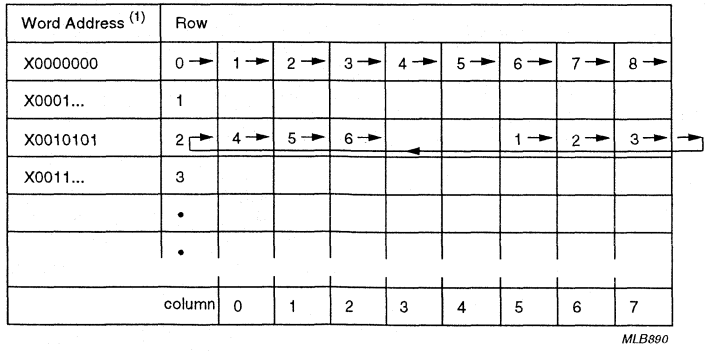


Fig.7 Master transmits to slave receiver (WRITE) mode.

After the word address, one-to-eight data bytes can be sent. The address is automatically incremented, but the four highest address bits (row) are internally latched. Therefore all bytes are written in the same row.

An example of writing eight bytes with word address X 0 0 0 0 0 0 0 and six bytes with word address X 0 0 1 0 1 0 1 is shown in Fig.8.



(1) X = don't care.

Fig.8 Writing eight and six bytes with different word addresses.

To transmit eight bytes in sequential order, begin with the lowest address bits 0 0 0. The data is written after a stop is detected. The data is only written if complete bytes have been received and acknowledged. Writing takes a time t_{WR} (6 to 10 ms) during which the device will not respond to its slave address. Note that to write the next row, a new write operation is required (start, slave address, row address, data and stop).

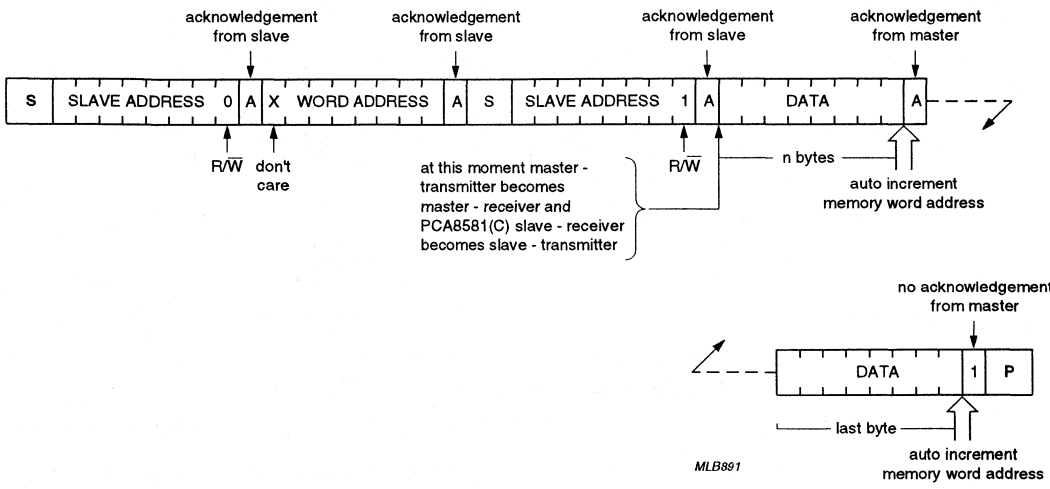


Fig.9 Master reads after setting word address (WRITE word address; READ data).

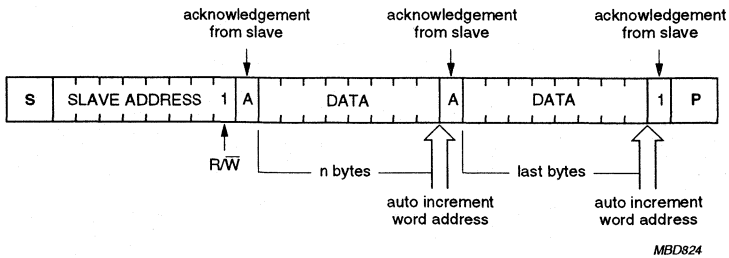


Fig.10 Master reads slave immediately after first byte (READ mode).

An unlimited number of data bytes can be read in one operation. The address is automatically incremented. If a read without setting the word address is performed after a write operation, the address pointer may point at a byte in the row after the previously written row. This occurs if, during writing, the three lowest address bits (column) rolled over.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pin 8)		−0.3	+7.0	V
V_I	input voltage (any input)	measured via a 500 Ω resistor	−0.8	V_{DD} + 0.8	V
I_I	DC input current		–	±10	mA
I_O	DC output current		–	±10	mA
P_{tot}	total power dissipation per package		–	150	mW
P_O	power dissipation per output		–	50	mW
T_{amb}	operating ambient temperature		−25	+85	°C
T_{stg}	storage temperature	without EEPROM retention	−65	+150	°C
		with EEPROM retention	−65	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

DC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V (PCA8581C); V_{DD} = 4.5 to 5.5 V (PCA8581); V_{SS} = 0 V; T_{amb} = −25 to +85 °C; note 1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage					
	PCA8581C		2.5	–	6.0	V
	PCA8581		4.5	–	5.5	V
I_{DD}	supply current					
	standby mode	f_{SCL} = 0 Hz; V_{IL} = 0 V; V_{IH} = V_{DD}	–	–	10	μA
	during read cycle	f_{SCL} = 100 Hz; V_{IL} = 0 V; V_{IH} = V_{DD}	–	–	400	μA
	during write cycle	V_{IL} = 0 V; V_{IH} = V_{DD}	–	–	1000	μA
Inputs A0, A1, A2, SDA and SCL						
V_{IL}	LOW level input voltage		–	–	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	–	V
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}	–	–	1	μA
C_I	input capacitance	V_I = V_{SS}	–	–	7	pF
Output SDA						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	–	–	mA
Erase/write data						
t_{WR}	write time		–	7	10	ms
t_{RET}	data retention time		10	–	–	years

Note

1. The PCA8581C is guaranteed to be programmed with all locations 'FF' (hexadecimal) provided the device has been stored within the temperature limits −65 to +85 °C.

AC CHARACTERISTICS

All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
I²C-bus timing (see Fig.11; note 1)					
f_{SCL}	SCL clock frequency	–	–	100	kHz
t_{SP}	tolerable spike width on bus	–	–	100	ns
t_{BUF}	bus free time	4.7	–	–	µs
$t_{SU;STA}$	start condition set-up time	4.7	–	–	µs
$t_{HD;STA}$	start condition hold time	4.0	–	–	µs
t_{LOW}	SCL LOW time	4.7	–	–	µs
t_{HIGH}	SCL HIGH time	4.0	–	–	µs
t_r	SCL and SDA rise time	–	–	1.0	µs
t_f	SCL and SDA fall time	–	–	0.3	µs
$t_{SU;DAT}$	data set-up time	250	–	–	ns
$t_{HD;DAT}$	data hold time	0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid	–	–	3.4	µs
$t_{SU;STO}$	stop condition set-up time	4.0	–	–	µs

Note

1. A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

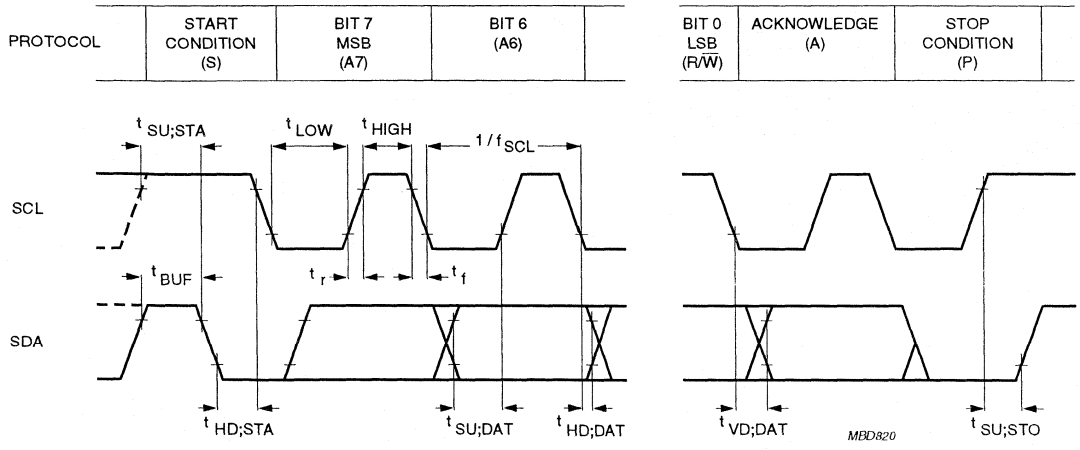


Fig.11 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

APPLICATION INFORMATION

Slave address

The PCA8581 has a fixed combination 1 0 1 0 as group 1, while group 2 is fully programmable (see Fig.12).

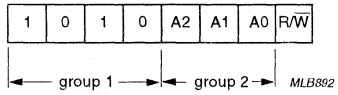
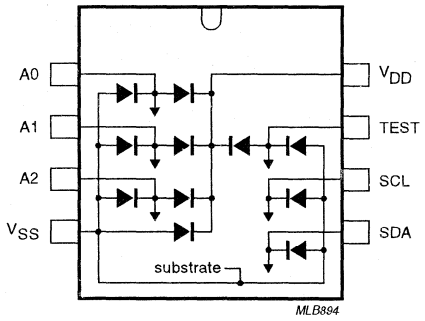


Fig.12 Slave address.

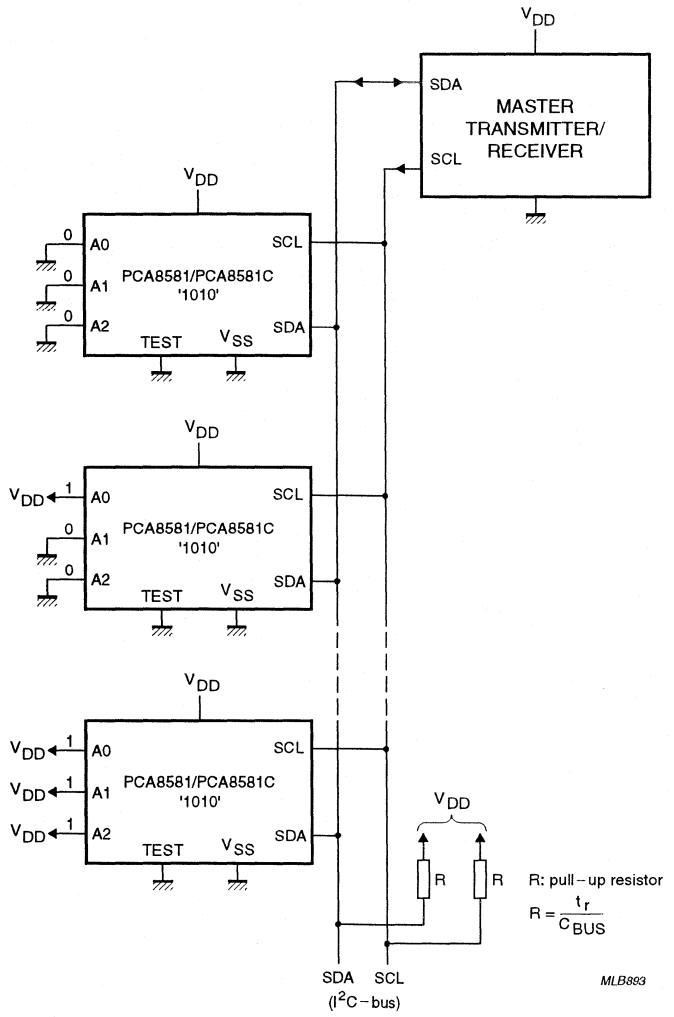
Diode protection



There is no connection between SCL and V_{DD}, and SDA and V_{DD}; this allows powering down the device without affecting I²C-bus operation.

Fig.13 Device diode protection.

Application example



Inputs A0, A1 and A2 must be connected to V_{DD} of V_{SS} but not left open-circuit.

Fig.14 Application diagram.

DTMF/MODEM/MUSICAL-TONE GENERATORS

GENERAL DESCRIPTION

The PCD3311C and PCD3312C are single-chip silicon gate CMOS integrated circuits. They are intended to provide dual-tone multi-frequency (DTMF) combinations required for tone dialling systems in telephone sets which contain a microcontroller for the control functions.

The various audio output frequencies are generated from an on-chip 3,58 MHz quartz crystal-controlled oscillator.

The devices can interface directly to all standard microcontrollers by accepting a binary-coded parallel input or serial data input (I^2C-bus).

With their on-chip voltage reference the PCD3311C and PCD3312C provide constant output amplitudes which are independent of the operating supply voltage and ambient temperature.

An on-chip filtering system assures a very low total harmonic distortion in accordance with the CEPT T/CS46-03 (= former CS203) recommendations.

In addition to the standard DTMF frequencies the devices provide 12 MODEM frequencies (300 to 1200 bits per second) used in simplex MODEM applications and two octaves of musical scale in steps of semitones.

Features

- Stabilized output voltage level
- Low output distortion with on-chip filtering (CEPT CS 203 compatible)
- Latched inputs for data bus applications
- I^2C-bus compatible
- Mode select input (selection of parallel or serial data input)
- MODEM and melody tone generators

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current	I_{DD}	–	–	0,9	mA
Static standby current	I_{DDO}	–	–	3	μA
DTMF output voltage level (RMS values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion	THD	–	−25	–	dB
Operating ambient temperature range	T_{amb}	−25	–	+70	°C

PACKAGE OUTLINES

PCD3311CP: 14-lead DIL; plastic (SOT27).
PCD3311CT: 16-lead mini-pack; plastic (SO16L; SOT162A).
PCD3312CP: 8-lead DIL; plastic (SOT97).
PCD3312CT: 8-lead mini-pack; plastic (SO8L; SOT176C).

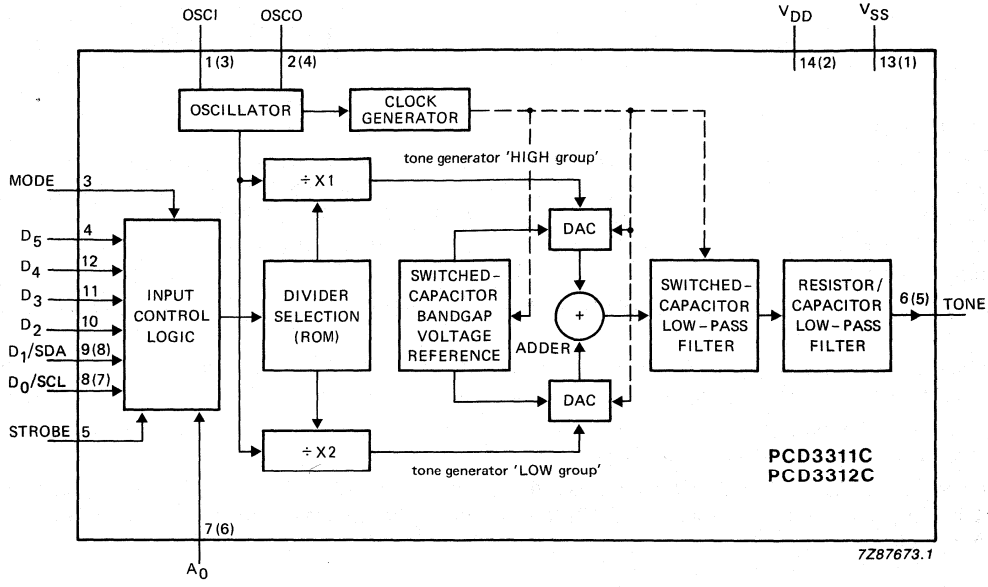


Fig. 1 Block diagram; the pin numbers in parenthesis refer to the PCD3312C.

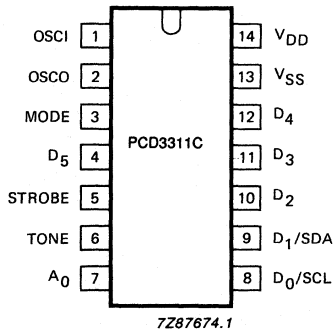


Fig. 2 Pinning diagram for the PCD3311CP.

PINNING

1	OSCI	oscillator input
2	OSCO	oscillator output
3	MODE	mode select input; used for the selection between serial mode (MODE = LOW) and parallel mode (MODE = HIGH)
4	D_5	parallel data input*
5	STROBE	strobe input; used for the loading of data in the parallel mode
6	TONE	frequency output for single or dual tones
7	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
8	D_0/SCL	parallel data input* or serial clock line (I^2C-bus)
9	D_1/SDA	parallel data input* or serial data line (I^2C-bus)
10	D_2	parallel data inputs*
11	D_3	
12	D_4	
13	V_{SS}	negative supply
14	V_{DD}	positive supply

* MODE = HIGH.

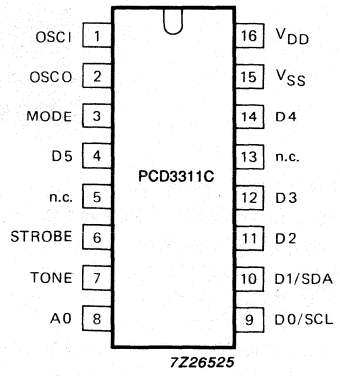


Fig. 3 Pinning diagram for the PCD3311CT.

PINNING

1	OSCI	oscillator input
2	OSCO	oscillator output
3	MODE	mode select input; used for the selection between serial mode (MODE = LOW) and parallel mode (MODE = HIGH)
4	D_5	parallel data input*
6	STROBE	strobe input; used for the loading of data in the parallel mode
7	TONE	frequency output for single or dual tones
8	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
9	D_0/SCL	parallel data input* or serial clock line (I^2C-bus)
10	D_1/SDA	parallel data input* or serial data line (I^2C-bus)
11	D_2	
12	D_3	parallel data inputs*
14	D_4	
15	V_{SS}	negative supply
16	V_{DD}	positive supply
5; 13	n.c.	not connected

* MODE = HIGH.

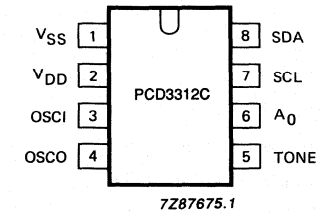


Fig. 4 Pinning diagram for the PCD3312C.

PINNING

1	V_{SS}	negative supply
2	V_{DD}	positive supply
3	OSCI	oscillator input
4	OSCO	oscillator output
5	TONE	frequency output for single or dual tones
6	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
7	SCL	serial clock line (I^2C bus)
8	SDA	serial data line (I^2C bus)

LCD controller/drivers

PCF2116 family (PCF2114X; PCF2116X)

FEATURES

- Single chip LCD controller / driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4 lines of up to 12 characters per line
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user defined symbols
- On-chip:
  - generation of LCD supply voltage (external supply also possible)
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I²C-bus interface
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1 : 32 and 1 : 16
- Uses common 11 code instruction set
- Logic supply voltage range, $V_{DD} - V_{SS}$: 2.5 to 6 V
- Display supply voltage range, $V_{DD} - V_{LCD}$: 3.5 to 9 V
- Low power consumption.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

GENERAL DESCRIPTION

The PCF2116 family of LCD controller/drivers consists of 2 similar members: PCF2116X and PCF2114X, later referred to as PCF2116. The specific differences are expressed in separate paragraphs for PCF2116X and PCF2114X respectively. The letter X in PCF2116X or PCF2114X specifies the character set in the character generator ROM (CGROM). The different character sets currently available are specified by the letters A, C, G and J (see Figs 7 to 10). Set 'A' in PCF2116A characterises the built-in standard character set. Other character sets are available on request.

The PCF2116 is a low-power CMOS LCD controller and driver, designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system power consumption. The chip contains a character generator and displays alphanumeric and kana characters. The PCF2116 interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I²C-bus.

Packages

- PCF2116XU/10; chip on FFC
- PCF2114XU/10; chip on FFC
- PCF2116XU/12; chip with bumps on FFC
- PCF2114XU/12; chip with bumps on FFC
- PCF2116XH; SQFP128 (14 × 20 mm)
- Pin grid array PGA144 (samples only).

For further details see Chapters "Bonding pad locations"and "Package outline".

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF2114XH	128	SQFP128	plastic	SOT387-1
PCF2116XH	128	SQFP128	plastic	SOT387-1
PCF2114XU	116	FFC116	–	–
PCF2116XU	116	FFC116	–	–

BLOCK DIAGRAM

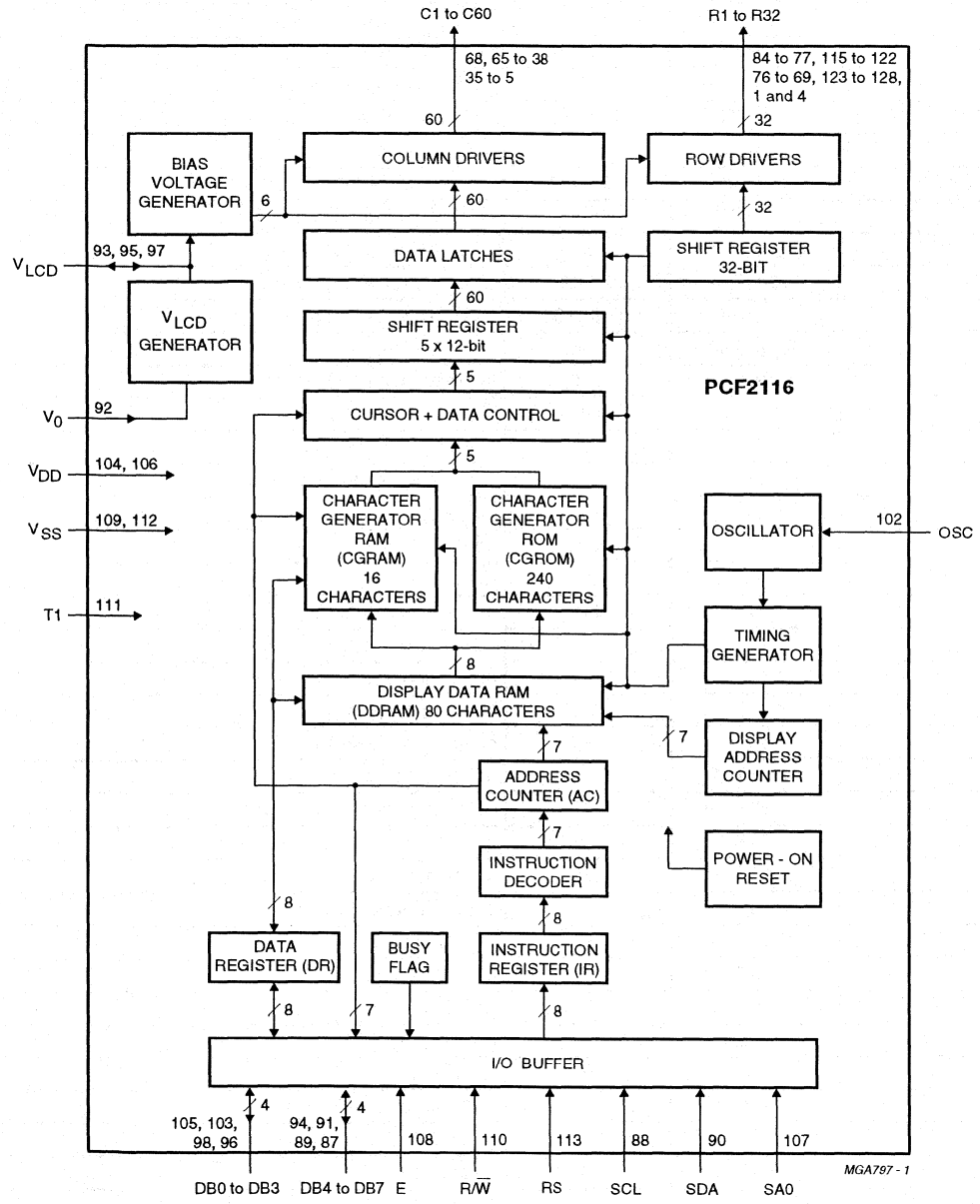


Fig.1 Block diagram (SQFP128).

PINNING

SYMBOL	SQFP128 PIN	FFC PAD	DESCRIPTION
R31	1	27	LCD row driver output
n.c.	2 and 3	–	not connected
R32	4	28	LCD row driver output
C60 to C30	5 to 35	29 to 59	LCD column driver outputs 60 to 30
n.c.	36 and 37	–	not connected
C29 to C2	38 to 65	60 to 87	LCD column driver outputs 29 to 2
n.c.	66 and 67	–	not connected
C1	68	88	LCD column driver output 1
R24 to R17	69 to 76	89 to 96	LCD row driver outputs
R8 to R1	77 to 84	97 to 104	LCD row driver outputs
n.c.	85 and 86	–	not connected
DB7	87	105	bidirectional data bus
SCL	88	106	I^2C serial clock input
DB6	89	107	bidirectional data bus
SDA	90	108	I^2C serial data input/output
DB5	91	109	bidirectional data bus
V_0	92	110	control input for V_{LCD}
V_{LCD1}	93	111	LCD supply voltage
DB4	94	112	bidirectional data bus
V_{LCD2}	95	113	LCD supply voltage
DB3	96	114	bidirectional data bus
V_{LCD3}	97	115	LCD supply voltage
DB2	98	116	bidirectional data bus
n.c.	99 to 101	–	not connected
OSC	102	1	oscillator/external clock input
DB1	103	2	bidirectional data bus
V_{DD2}	104	3	supply voltage
DB0	105	4	bidirectional data bus
V_{DD1}	106	5	supply voltage
SA0	107	6	I^2C address pin
E	108	7	data bus clock
V_{SS1}	109	8	ground (logic)
$R/\overline{W}$	110	9	read/write
T1	111	10	test pad (connect to V_{SS})
V_{SS2}	112	11	ground (logic)
RS	113	12	register select
n.c.	114	–	not connected
R9 to R16	115 to 122	13 to 20	LCD row driver outputs
R25 to R30	123 to 128	21 to 26	LCD row driver outputs

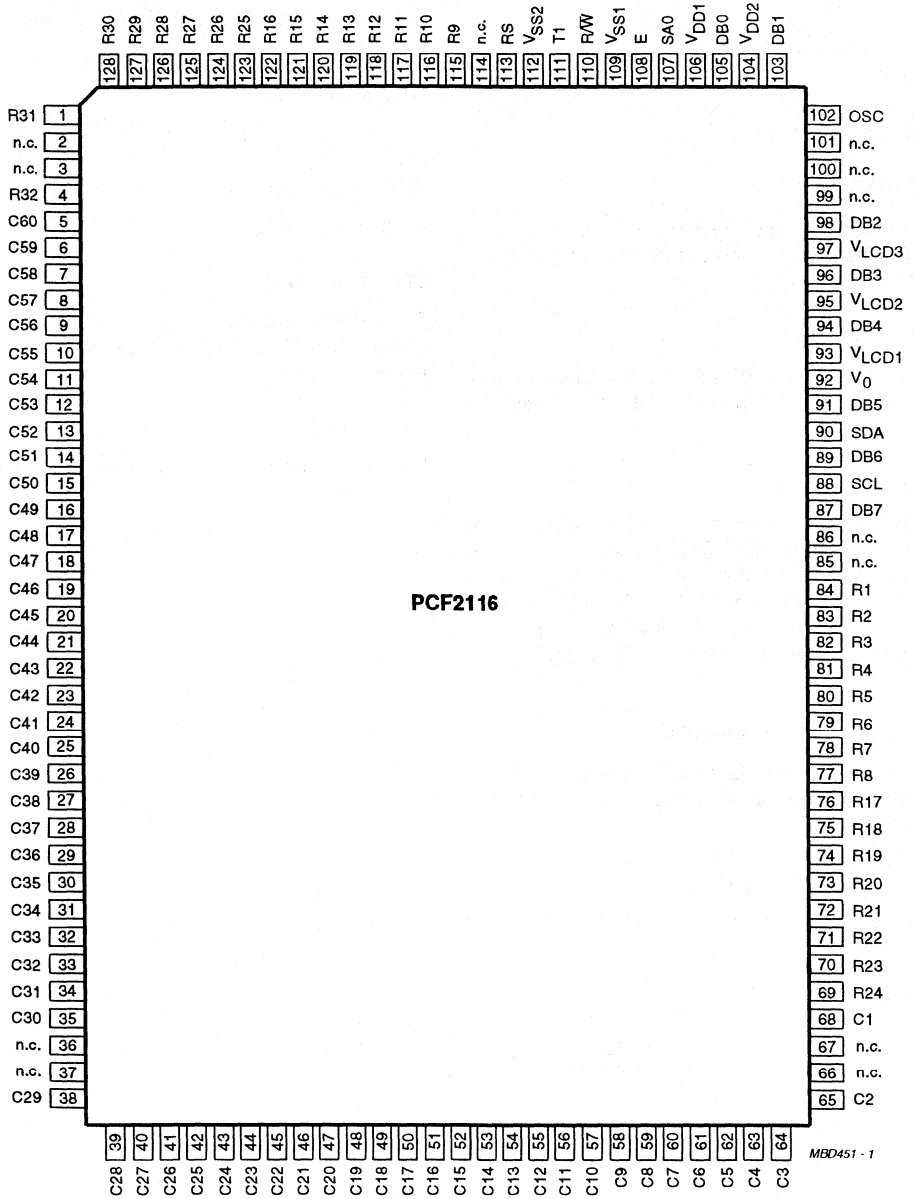


Fig.2 Pin configuration (SQFP128).

PIN FUNCTIONS

RS: register select(1)

RS selects the register to be accessed for read and write. RS = logic 0 selects the instruction register for write and the busy flag and address counter for read. RS = logic 1 selects the data register for both read and write. There is an internal pull-up on pin RS.

R/$\overline{W}$: read/write(1)

R/$\overline{W}$ selects either the read (R/$\overline{W}$ = logic 1) or write (R/$\overline{W}$ = logic 0) operation. There is an internal pull-up on this pin.

E: data bus clock(1)

The E pin is set HIGH to signal the start of a read or write operation. Data is clocked in or out of the chip on the negative edge of the clock.

DB0 to DB7: data bus(1)

The bidirectional, 3-state data bus transfers data between the system controller and the PCF2116. DB7 may be used as the busy flag, signalling that internal operations are not yet completed. In 4-bit operations the 4 higher order lines DB4 to DB7 are used; DB0 to DB3 must be left open circuit. There is an internal pull-up on each of the data lines.

C1 to C60: column driver outputs

These pins output the data for pairs of columns. This arrangement permits optimized COG layout for 4-line by 12 characters.

R1 to R32: row driver outputs

These pins output the row select waveforms to the left and right halves of the display.

V_{LCD}: LCD power supply

Negative power supply for the liquid crystal display. This may be generated on-chip or supplied externally.

V_0: V_{LCD} control input

The input level at this pin determines the generated V_{LCD} output voltage.

OSC: oscillator

When the on-chip oscillator is used this pin must be connected to V_{DD}. An external clock signal, if used, is input at this pin.

SCL: serial clock line

Input for the I^2C-bus clock signal.

SDA: serial data line

I/O for the I^2C-bus data line.

SAO: address pin

The hardware sub-address line is used to program the device sub-address for 2 different PCF2116s on the same I^2C-bus.

T1: test pad

Must be connected to V_{SS}. Not user accessible.

(1) When I^2C-bus is used, the parallel interface pin E must be defined: E = logic 0; in I^2C-bus read mode DB0 to DB7 must be left open circuit.

BLOCK DIAGRAM FUNCTIONS

LCD supply voltage generator

The on-chip voltage generator is controlled by bit G of the function set command and V_0.

V_0 is a high-impedance input and draws no current from the system power supply. Its range is between V_{SS} and $V_{DD} - 1$ V. When V_0 is connected to V_{DD} the generator is switched off and an external voltage must be supplied at pin V_{LCD}. This may be more negative than V_{SS}.

When G = logic 1 the generator produces a negative voltage at pin V_{LCD}, controlled by the input voltage at pin V_0. The LCD operating voltage is given by the relationship:

$$V_{OP} = 1.8V_{DD} - V_0$$

Where:

$$V_{OP} = V_{DD} - V_{LCD}$$

$$V_{LCD} = V_0 - (0.8V_{DD})$$

When G = logic 0, the generated output voltage V_{LCD} is equal to V_0 (between V_{SS} and V_{DD}). In this instance:

$$V_{OP} = V_{DD} - V_0$$

When V_{LCD} is generated on-chip the V_{LCD} pin should be decoupled to V_{DD} with a suitable capacitor. V_{DD} and V_0 must be selected to limit the maximum value of V_{OP} to 9 V.

Figure 3 shows the two control characteristics for the generator.

LCD bias voltage generator

The intermediate bias voltages for the LCD display are also generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system power consumption. The optimum levels depend on the multiplex rate and are selected automatically when the number of lines in the display is defined.

The optimum value of V_{OP} depends on the multiplex rate, the LCD threshold voltage (V_{th}) and the number of bias levels and is given by the relationships in Table 1.

Using a 5-level bias scheme for 1 : 16 mux rate allows $V_{OP} < 5$ V for most LCD liquids. The effect on the display contrast is negligible.

Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC pin must be connected to V_{DD}.

External clock

If an external clock is to be used this is input at the OSC pin. The resulting display frame frequency is given by $f_{frame} = f_{osc} / 2304$. A clock signal must always be present, otherwise the LCD may be frozen in a DC state.

Power-on reset

The power-on reset block initializes the chip after power-on or power failure.

Registers

The PCF2116 has two 8-bit registers, an instruction register (IR) and a data register (DR). The register select signal (RS) determines which register will be accessed.

The instruction register stores instruction codes such as display clear and cursor shift, and address information for the Display Data RAM (DDRAM) and Character Generator RAM (CGRAM). The instruction register can be written from but not read by the system controller.

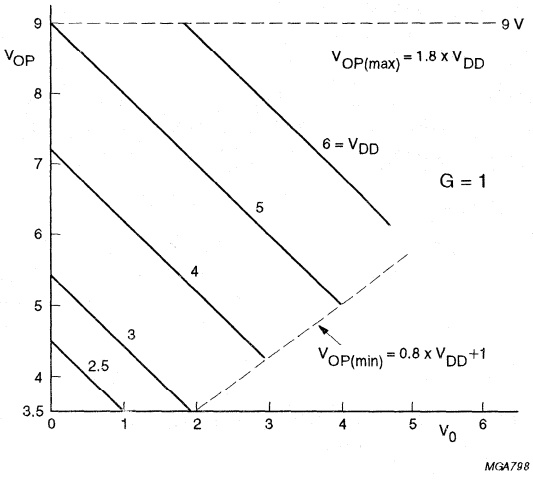
The data register temporarily stores data to be read from the DDRAM and CGRAM. When reading, data from the DDRAM or CGRAM corresponding to the address in the address counter is written to the data register prior to being read by the read data instruction.

Busy flag

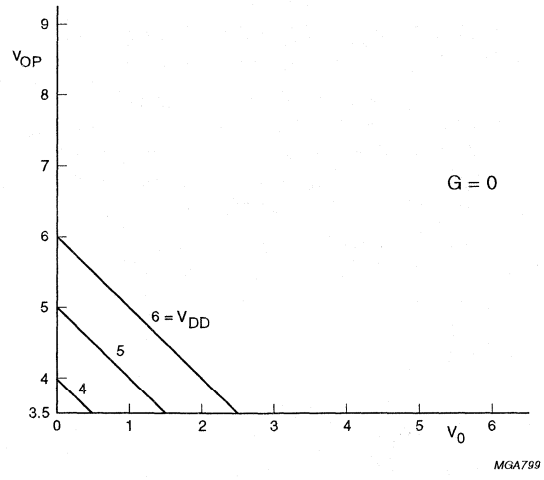
The busy flag indicates the internal status of the PCF2116, a logic 1 indicating that the chip is busy and further instructions will not be accepted. The busy flag is output to pin DB7 when RS = logic 0 and R/$\overline{W}$ = logic 1. Instructions should only be written after checking that the busy flag is logic 0 or waiting for the required number of clock cycles.

Table 1 Optimum values for V_{OP}.

MUX RATE	NUMBER OF BIAS LEVELS	V_{OP}/V_{th}	DISCRIMINATION V_{on}/V_{off}
1 : 16	5	3.67	1.277
1 : 32	6	5.19	1.196



a. High-voltage mode $V_{OP} = 1.8 \times V_{DD} - V_0$.



b. Buffer mode $V_{OP} = V_{DD} - V_0$.

Fig.3 V_{OP} as a function of V_0 control characteristics.

Address counter (AC)

The address counter assigns addresses to the DDRAM and CGRAM for reading and writing and is set by the commands 'Set CGRAM Address' and 'Set DDRAM Address'. After a read/write operation the address counter is automatically incremented or decremented by 1. The address counter contents are output to the bus (DB0 to DB6) when RS = logic 0 and R/$\overline{W}$ = logic 1.

Display data RAM (DDRAM)

The display data RAM stores up to 80 characters of display data represented by 8-bit character codes. RAM locations not used for storing display data can be used as general purpose RAM. The basic RAM to display addressing scheme is shown in Fig.4. With no display shift the characters represented by the codes in the first 12 or 24 RAM locations starting at address 00 in line 1 are displayed. Subsequent lines display data starting at addresses 20, 40, or 60 Hex. Figs 5 and 6 show the DDRAM to display mapping principle when the display is shifted.

The address range for a 1-line display is 00 to 4F; for a 2-line display from 00 to 27 (line 1) and 40 to 67 (line 2); for a 4-line display from 00 to 13, 20 to 33, 40 to 53 and 60 to 73 for lines 1, 2, 3 and 4 respectively. For 2 and 4-line displays the end address of one line and the start address of the next line are not consecutive. When the display is shifted each line wraps around independently of the others (Figs 5 and 6).

When data is written into the DDRAM wrap-around occurs from 4F to 00 in 1-line mode and from 27 to 40 and 67 to 00 in 2-line mode; from 13 to 20, 33 to 40, 53 to 60 and 73 to 00 in 4-line mode.

Character generator ROM (CGROM)

The character generator ROM generates 240 character patterns in 5 × 8 dot format from 8-bit character codes. Figures 7 to 10 show the character sets currently available.

Character generator RAM (CGRAM)

Up to 16 user-defined characters may be stored in the character generator RAM. The CGROM and CGRAM use a common address space, of which the first column is reserved for the CGRAM (see Fig.7). Figure 11 shows the addressing principle for the CGRAM.

Cursor control circuit

The cursor control circuit generates the cursor (underline and/or character blink as shown in Fig.12) at the DDRAM address contained in the address counter. When the address counter contains the CGRAM address the cursor will be inhibited.

Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

LCD row and column drivers

The PCF2116 contains 32 row and 60 column drivers, which connect the appropriate LCD bias voltages in sequence to the display, in accordance with the data to be displayed. The bias voltages and the timing are selected automatically when the number of lines in the display is selected. Figures 13 and 14 show typical waveforms.

In 1-line mode (1 : 16) the row outputs are driven in pairs: R1/R17, R2/R18 for example. This allows the output pairs to be connected in parallel, providing greater drive capability.

Unused outputs should be left unconnected.

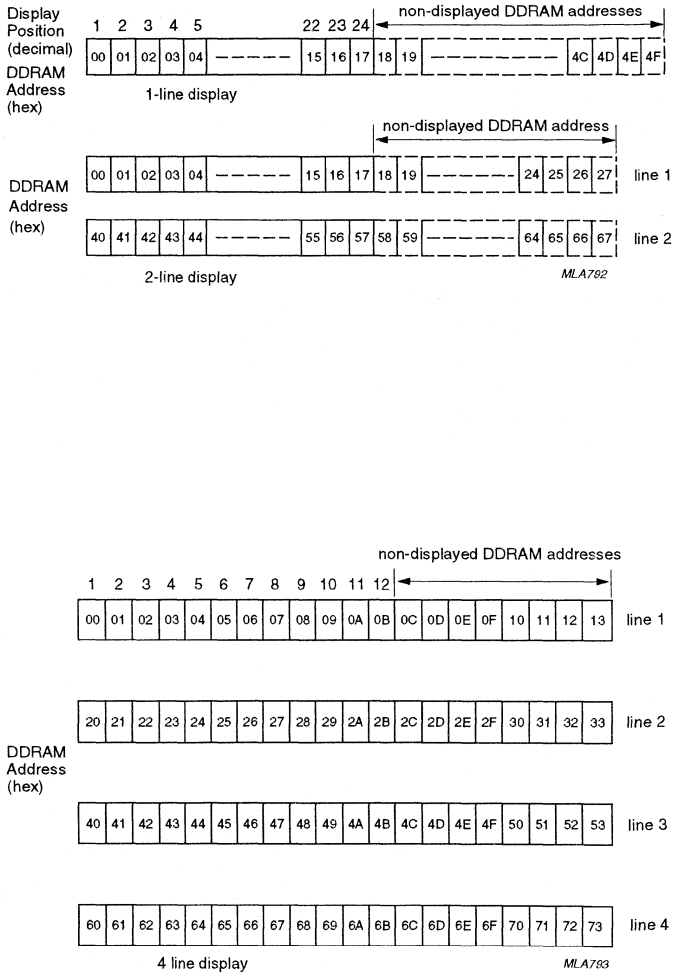


Fig.4 DDRAM to display mapping; no shift (PCF2116X).

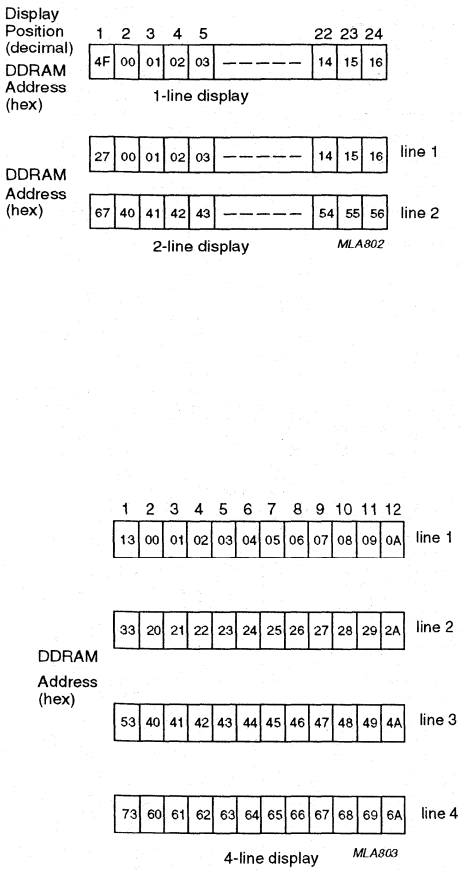


Fig.5 DDRAM to display mapping; right shift (PCF2116X).

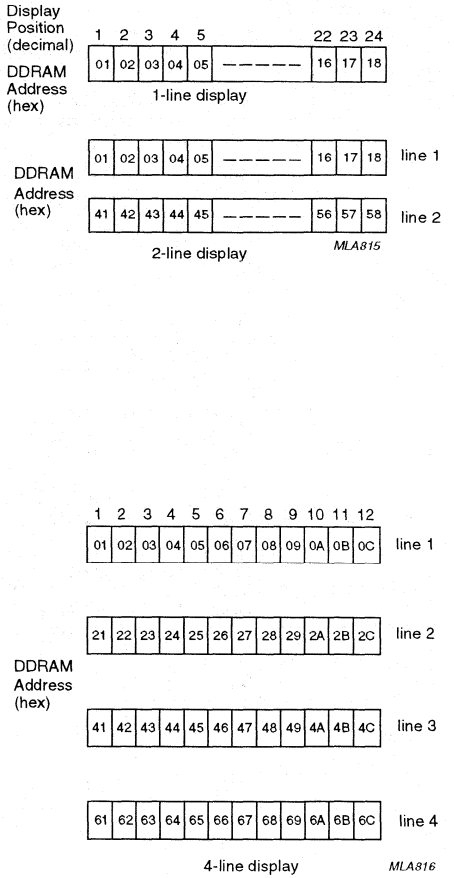


Fig.6 DDRAM to display mapping; left shift (PCF2116X).

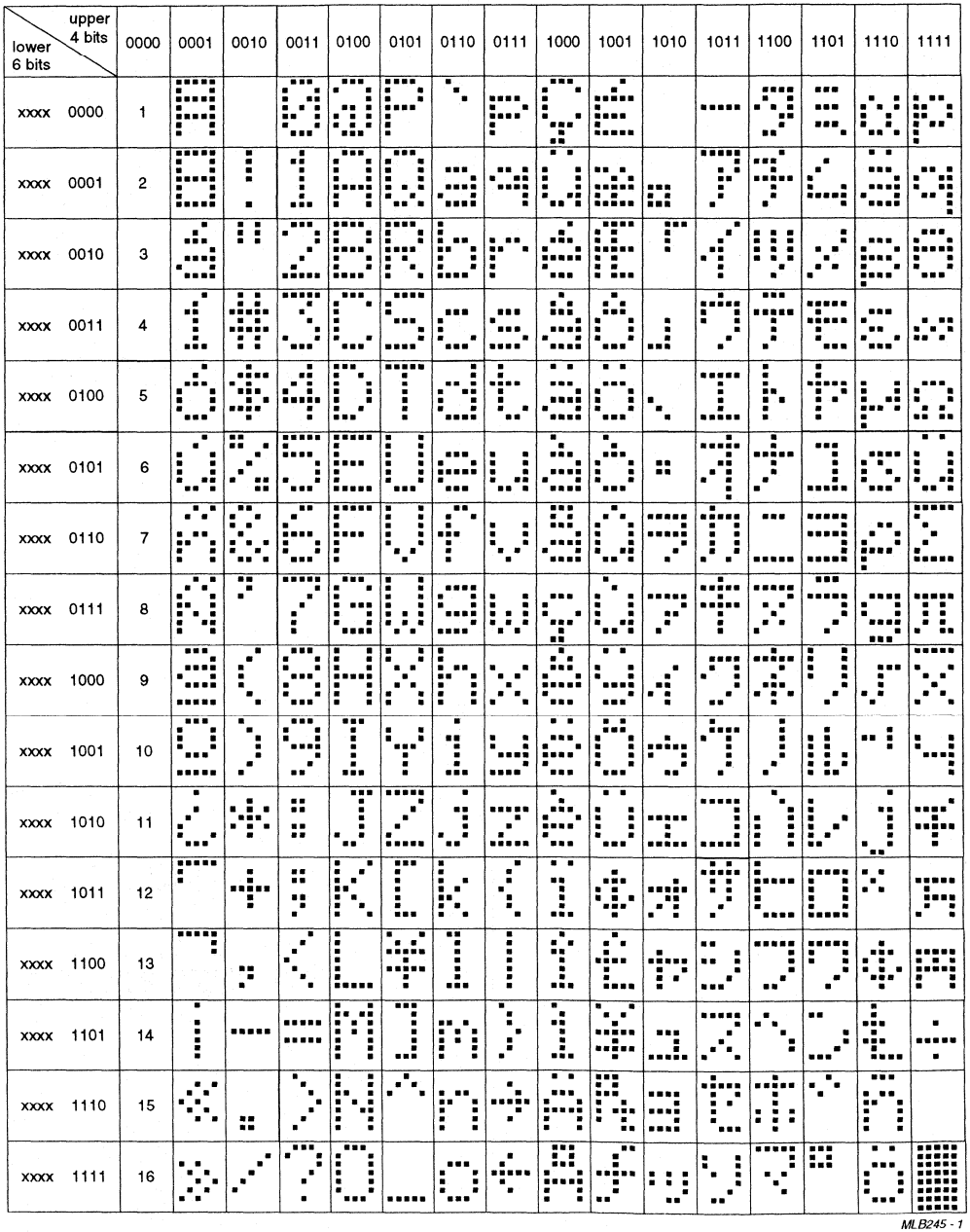


Fig.7 Character set 'A' in CGROM; PCF2116A; PCF2114A.

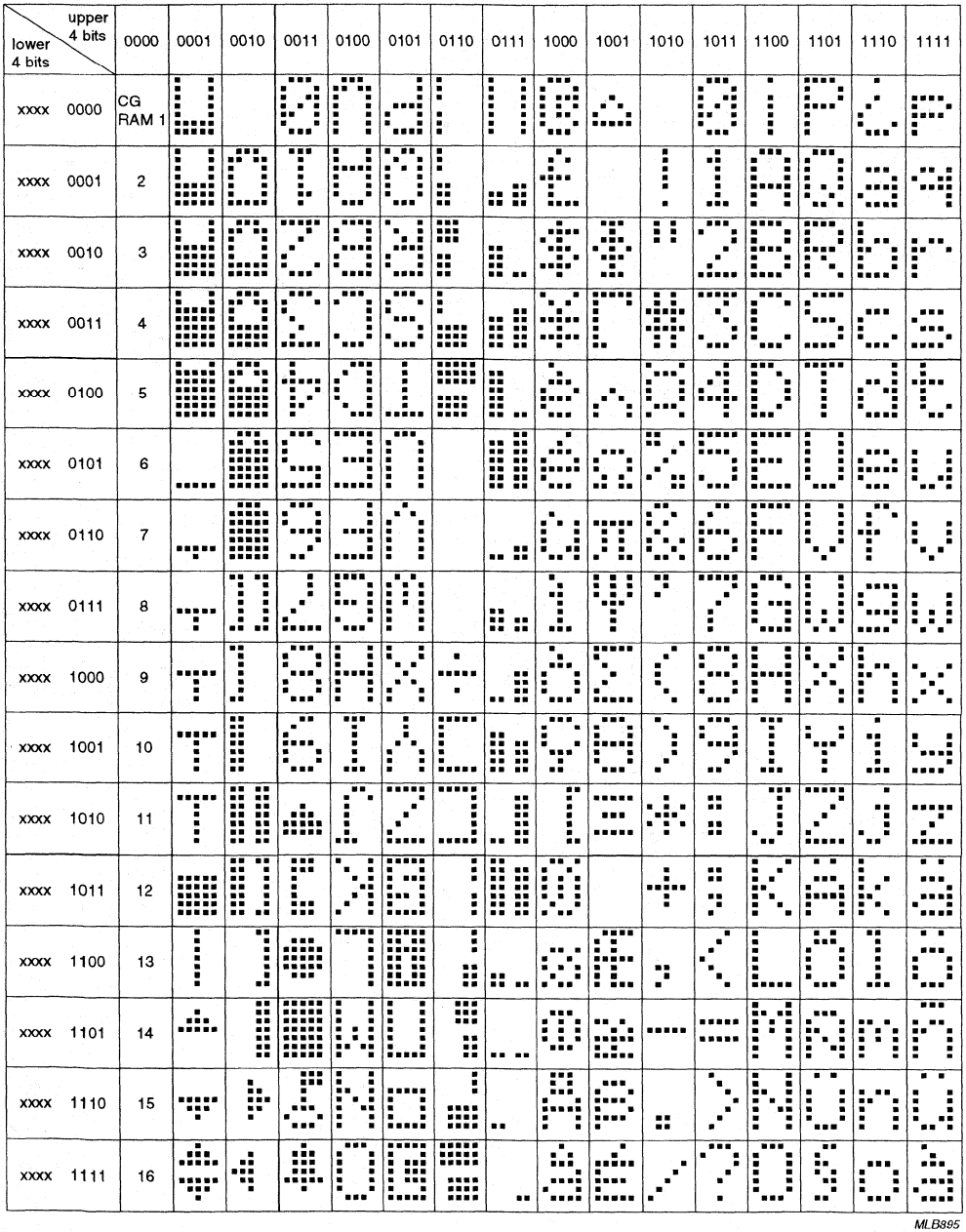


Fig.8 Character set 'C' in CGROM; PCF2116C; PCF2114C.

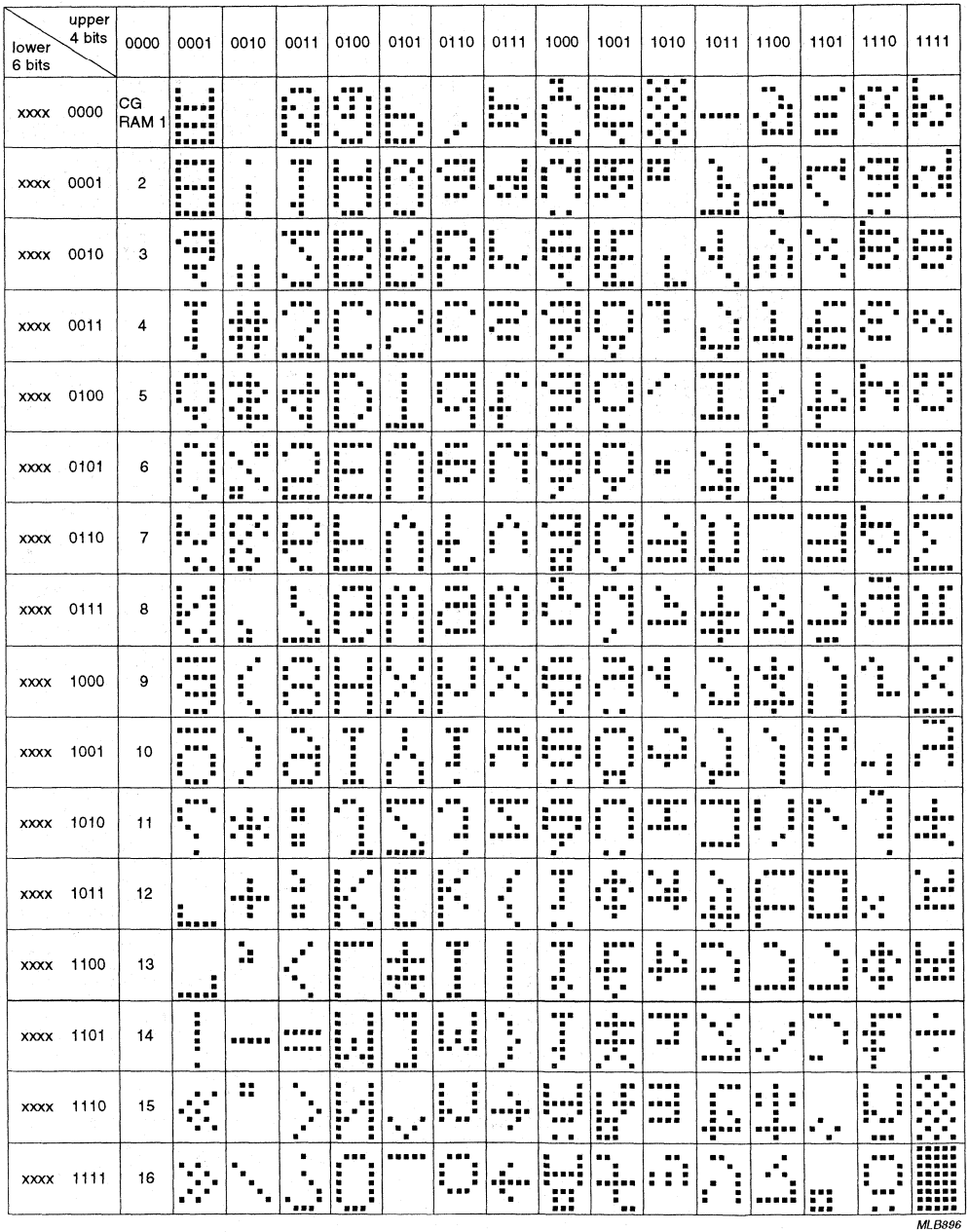


Fig.9 Character set 'G' in CGROM; PCF2116G; PCF2114G.

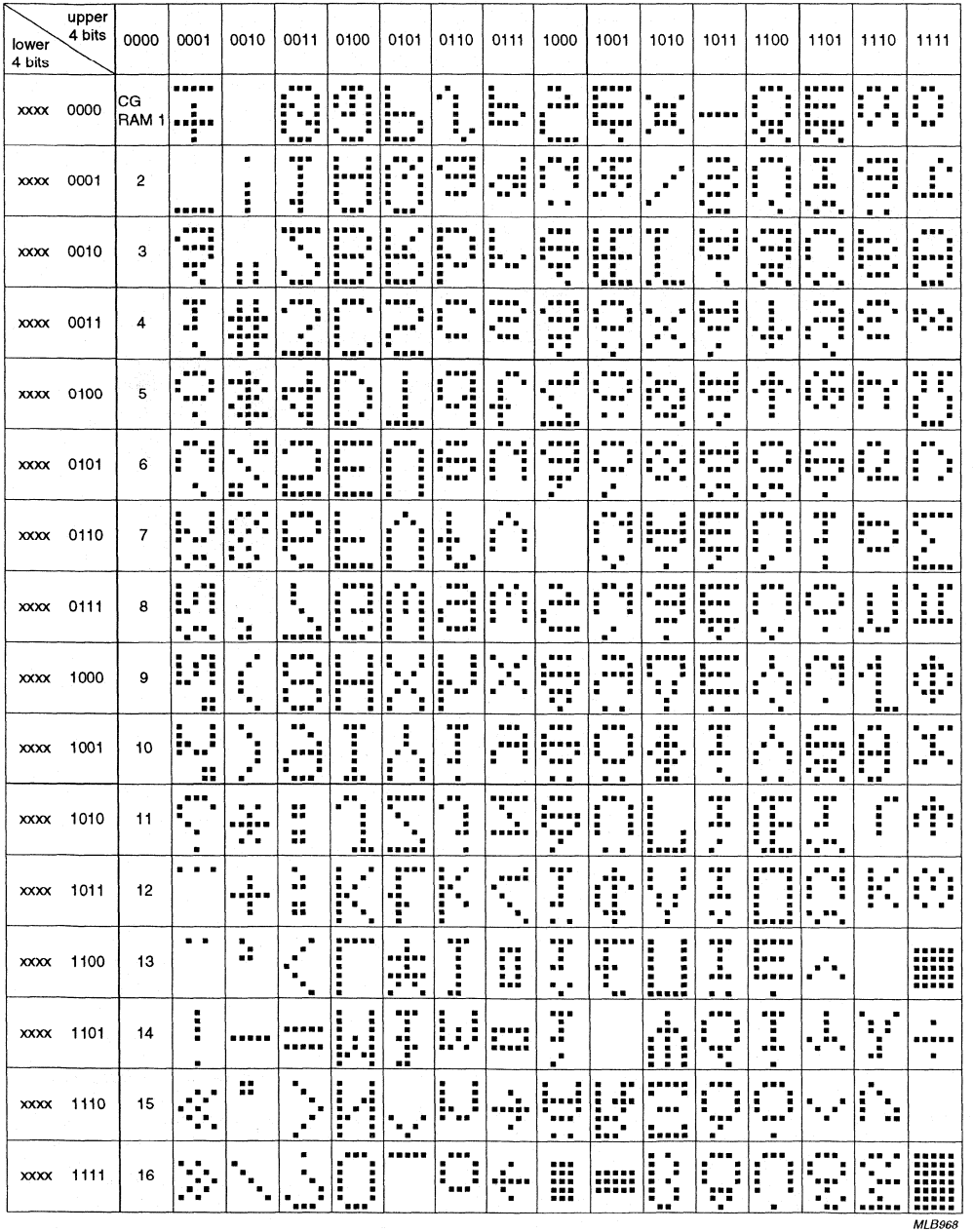
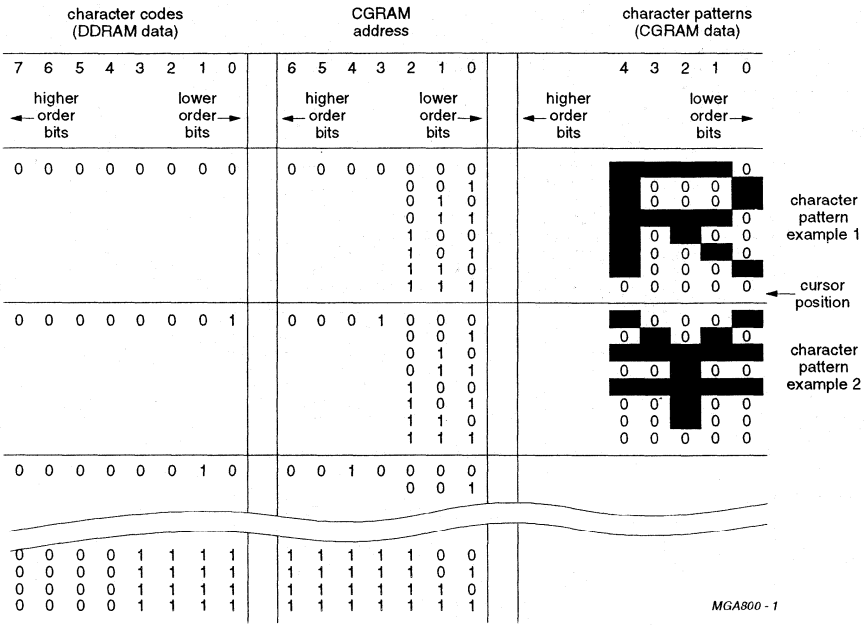


Fig.10 Character set 'J' in CGROM; PCF2116J; PCF2114J.



Character code bits 0 to 3 correspond to CGRAM address bits 3 to 6.

CGRAM address bits 0 to 2 designate character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor. Data in the 8th line will appear in the cursor position.

Character pattern column positions correspond to CGRAM data bits 0 to 4, as shown in Fig.11 (bit 4 being at the left end).

As shown in Figs 7 and 11, CGRAM character patterns are selected when character code bits 4 to 7 are all logic 0. CGRAM data = logic 1 corresponds to selection for display.

Only bits 0 to 5 of the CGRAM address are set by the 'Set CGRAM Address' command. Bit 6 can be set using the 'Set DDRAM Address' command or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the 'Read BF and Address' command.

Fig.11 Relationship between CGRAM addresses and data and display patterns.

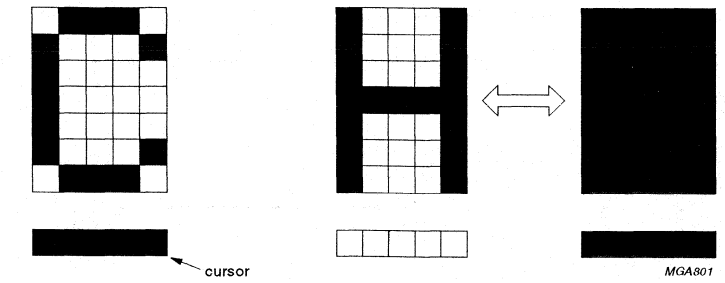


Fig.12 Cursor and blink display examples.

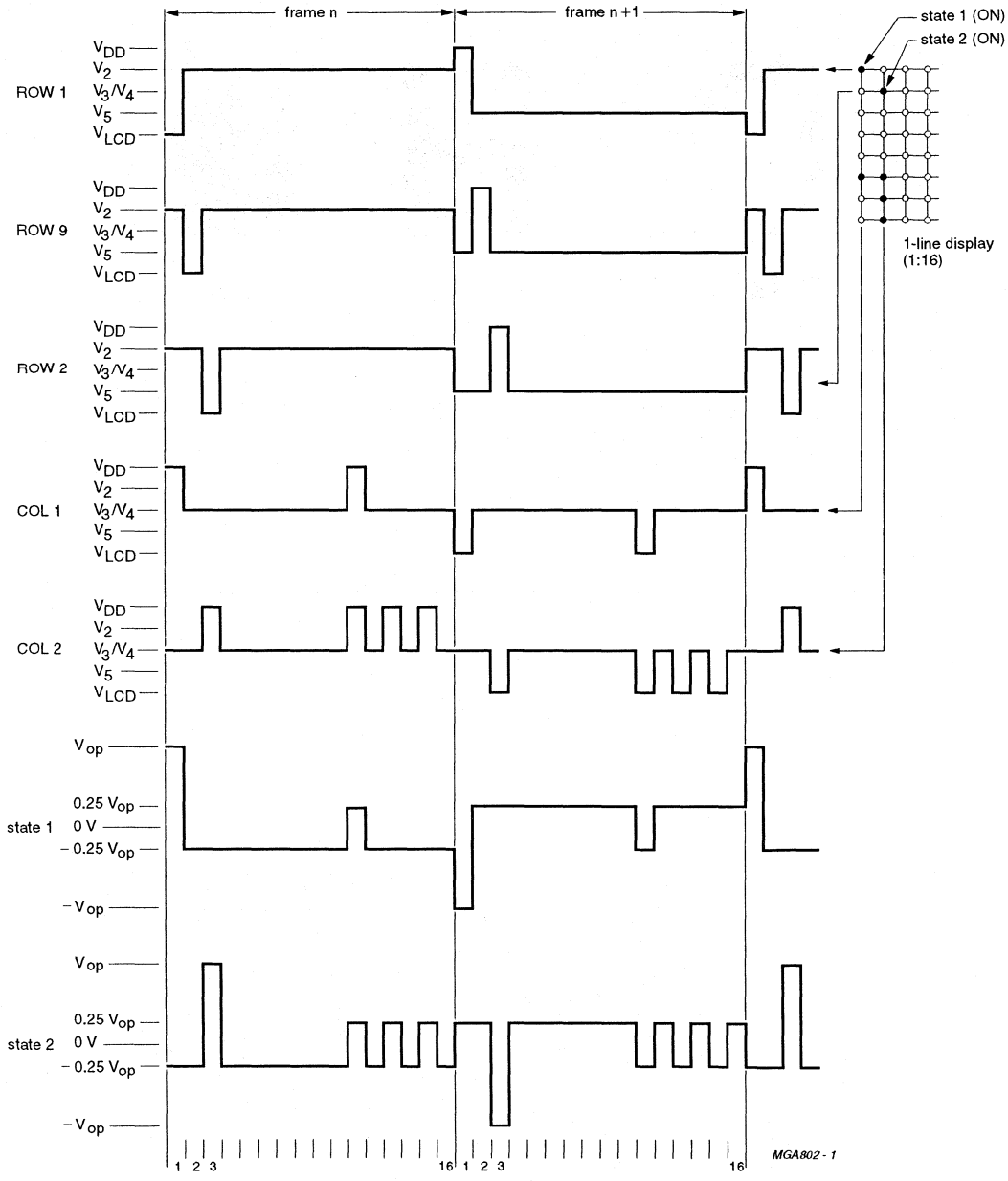


Fig.13 Typical LCD waveforms; 1-line mode.

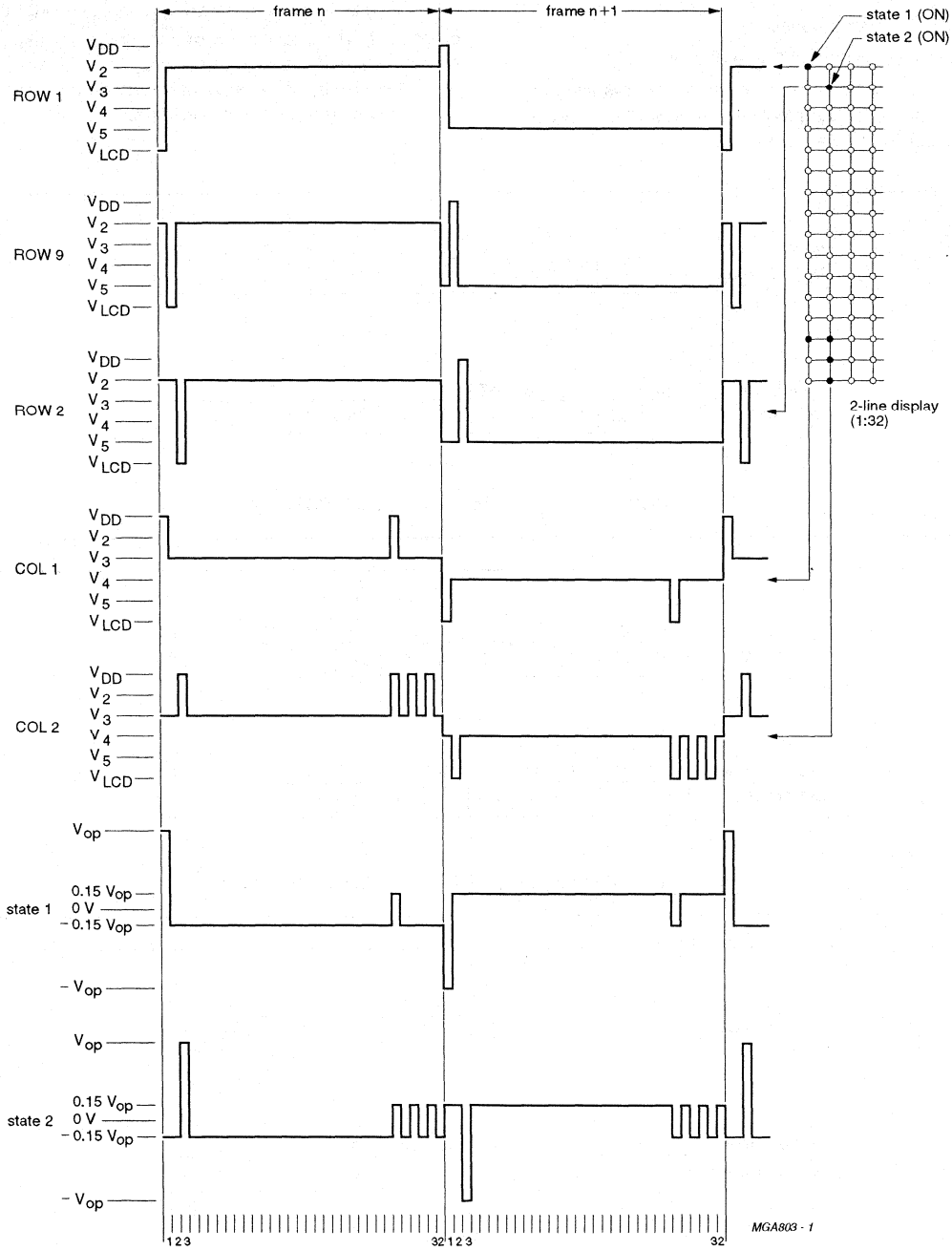


Fig.14 Typical LCD waveforms; 2-line mode.

Programming of mux 1 : 16 displays with PCF2114X

The PCF2114 can be used in:

- 1-line mode to drive a 2-line display
- 2 × 12 characters with mux rate 1 : 16, resulting in better contrast. The internal data flow of the chip is optimized for this purpose.

With the Function Set instruction M and N are set to 0, 0. Figures 15 to 17 show DDRAM addresses of the display characters. The second row of each table corresponds to either the right half of a 1-line display or to the second line of a 2-line display. Wrap around of data during display shift or when writing data is non-standard.

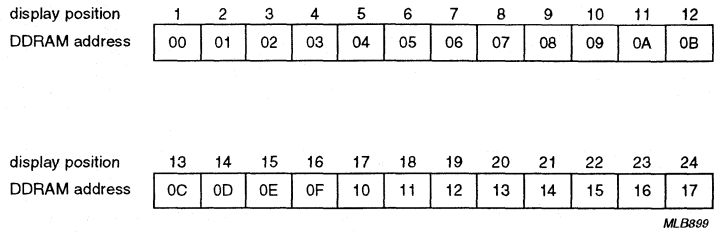


Fig.15 DDRAM to display mapping; no shift (PCF2114X).

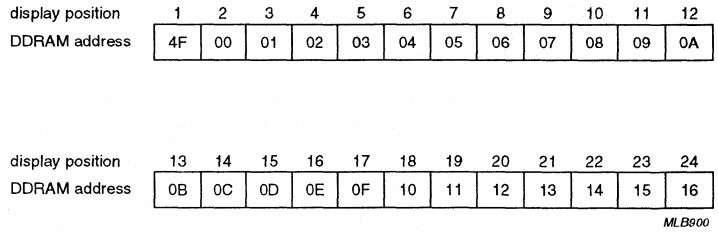


Fig.16 DDRAM to display mapping; right shift (PCF2114X).

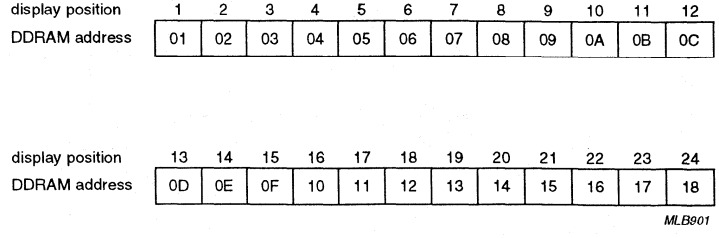


Fig.17 DDRAM to display mapping; left shift (PCF2114X).

Programming of mux 1 : 32 displays with PCF2114X

To drive a 2-line by 24 characters mux 1 : 32 display, use instruction Function Set M, N to 0, 1. Note that the right half of the display needs mirrored column connection compared to a display driven by a PCF2116X.

To drive a 4-line by 12 characters mux 1 : 32 display the PCF2116 operating instructions apply. There is no functional difference between the two chips in this mode. For such an application set M, N to 1,1 with the Function Set instruction.

Reset function

The PCF2116 automatically initializes (resets) when power is turned on. After reset the chip has the following state.

Table 2 State after reset.

STEP	DESCRIPTION		
1	Display clear.		
2	Function set.	DL = 1	8-bit interface
		M, N = 0	1-line display
		G = 0	voltage generator; $V_{LCD} = V_0$
3	Display on/off control.	D = 0	display off
		C = 0	cursor off
		B = 0	blink off
4	Entry mode set.	I/D = 1	+1 (increment)
		S = 0	no shift
5	Default address pointer to DDRAM. The busy flag (BF) indicates the busy state (BF = logic 1) until initialization ends. The busy state lasts 2 ms. The chip may also be initialized by software. See Figs 28 and 29.		
6	I^2C-bus interface reset.		

INSTRUCTIONS

Only two PCF2116 registers, the instruction register (IR) and the data register (DR) can be directly controlled by the MPU. Before internal operation, control information is stored temporarily in these registers to allow interface to various types of MPUs which operate at different speeds or to allow interface to peripheral control ICs. The PCF2116 operation is controlled by the instructions shown in Table 3 together with their execution time. Details are explained in subsequent sections.

Instructions are of 4 categories, those that:

1. Designate PCF2116 functions such as display format, data length, etc.
2. Set internal RAM addresses.
3. Perform data transfer with internal RAM.
4. Others.

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the MPU program load. The display shift in particular can be performed concurrently with display data write, enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation, no instruction other than the busy flag/address read instruction will be executed.

Because the busy flag is set to logic 1 while an instruction is being executed, check to make sure it is on logic 0 before sending the next instruction or wait for the maximum instruction execution time, as given in Table 3. An instruction sent while the busy flag is HIGH will not be executed.

Table 3 Instructions (note 1).

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES(2)
NOP	0	0	0	0	0	0	0	0	0	0	no operation	0
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DDRAM address 0 in address counter.	165
Return Home	0	0	0	0	0	0	0	0	1	0	Sets DDRAM address 0 in address counter. Also returns shifted display to original position. DDRAM contents remain unchanged.	3
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read.	3
Display control	0	0	0	0	0	0	1	D	C	B	Sets entire display on/off (D), cursor on/off (C) and blink of cursor position character (B).	3
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	0	0	Moves cursor and shifts display without changing DDRAM contents.	3
Function set	0	0	0	0	1	DL	N	M	G	0	Sets interface data length (DL), number of display lines (N, M) and voltage generator control (G).	3
Set CGRAM address	0	0	0	1	A_{CG}						Sets CGRAM address	3
Set DDRAM address	0	0	1	A_{DD}							Sets DDRAM address	3
Read Busy Flag and Address Counter	0	1	BF	A_C							Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0
Read data	1	1	read data								Reads data from CGRAM or DDRAM.	3
Write data	1	0	write data								Writes data to CGRAM or DDRAM.	3

Notes

1. In the I²C-bus mode the DL bit is don't care. 8-bit mode is assumed.
   In the I²C-bus mode a control byte is required when RS or R/$\overline{W}$ is changed; control byte: Co, RS, R/$\overline{W}$, 0, 0, 0, 0, 0; command byte: DB7 to DB0.
2. Example: f_{osc} = 150 kHz, $T_{cy} = \frac{1}{f_{osc}}$ = 6.67 µs; 3 cycles = 20 µs, 165 cycles = 1.1 ms.

Table 4 Command bit identities.

BIT	0	1
I/D	decrement	increment
S	display freeze	display shift
D	display off	display on
C	cursor off	cursor on
B	character at cursor position does not blink	character at cursor position blinks
S/C	cursor move	display shift
R/L	left shift	right shift
DL	4 bits	8 bits
G	voltage generator: $V_{LCD} = V_0$	voltage generator; $V_{LCD} = V_0 - 0.8V_{DD}$
N, (M = 0)		
PCF2116	1 line × 24 characters; mux 1 : 16	2 lines × 24 characters; mux 1 : 32
PCF2114	2 line × 12 characters; mux 1 : 16	2 lines × 24 characters; mux 1 : 32
N, (M = 1)	reserved	4 lines × 12 characters; mux 1 : 32
BF	end of internal operation	internal operation in progress
Co	last control byte, only data bytes to follow	next two bytes are a data byte and another control byte

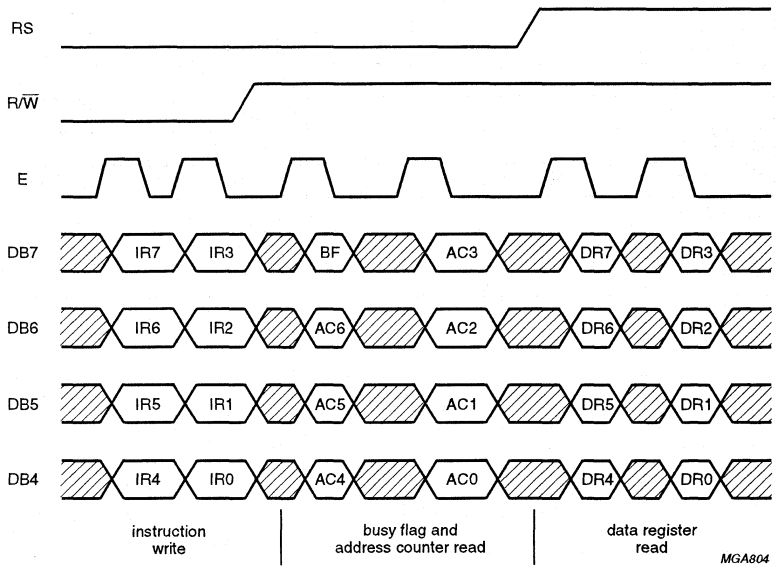
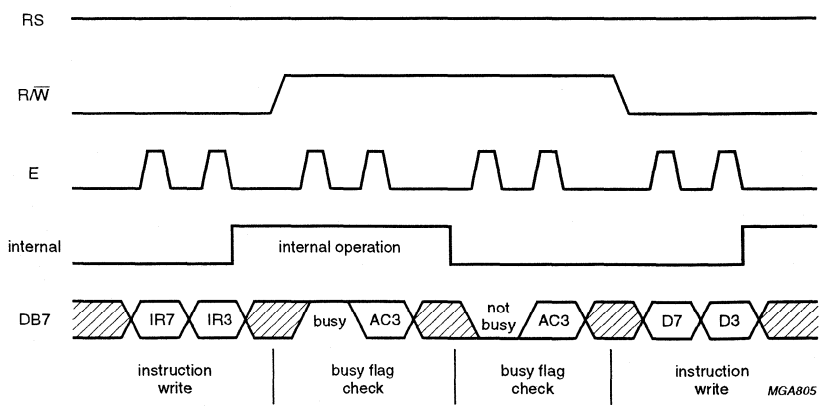


Fig.18 4-bit transfer example.



IR7, IR3: instruction 7th bit, 3rd bit.
AC3: address counter 3rd bit.

Fig.19 An example of 4-bit data transfer timing sequence.

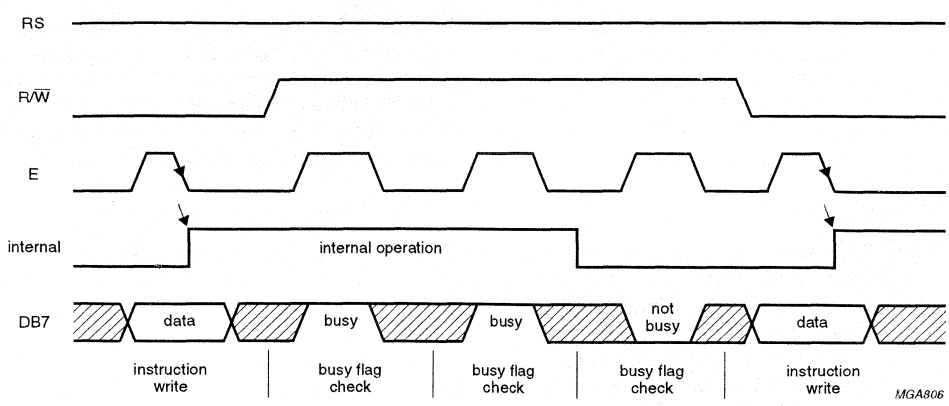


Fig.20 Example of busy flag check timing sequence.

Clear display

Clear Display writes space code 20 (hexadecimal) into all DDRAM addresses (The character pattern for character code 20 must be blank pattern). Sets the DDRAM address counter to logic 0. Returns display to its original position if it was shifted. Thus, the display disappears and the cursor or blink position goes to the left edge of the display (the first line if 2 or 4 lines are displayed). Sets entry mode I/D = logic 1 (increment mode). S of entry mode does not change.

The instruction Clear Display requires extra execution time. This may be allowed for by checking the busy-flag (BF) or by waiting until 2 ms has elapsed. The latter must be applied where no read-back options are foreseen, as in some chip-on-glass (COG) applications.

Return Home

Return Home sets the DDRAM address counter to logic 0. Returns display to its original position if it was shifted. DDRAM contents do not change. The cursor or blink position goes to the left of the display (the first line if 2 or 4 lines are displayed). I/D and S of entry mode do not change.

Entry mode set

ID

When I/D = logic 1 (0) the DDRAM or CGRAM address increments (decrements) by 1 when data is written into or read from the DDRAM or CGRAM. The cursor or blink position moves to the right when incremented and to the left when decremented. The cursor and blink are inhibited when the CGRAM is accessed.

S

When S = logic 1, the entire display shifts either to the right (I/D = logic 0) or to the left (I/D = logic 1) during a DDRAM write. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing into or reading out of the CGRAM. When S = logic 0 the display does not shift.

Display on/off control

D

The display is on when D = logic 1 and off when D = logic 0. Display data in the DDRAM are not affected and can be displayed immediately by setting D to logic 1.

C

The cursor is displayed when C = logic 1 and inhibited when C = logic 0. Even if the cursor disappears, the display functions I/D, etc. remain in operation during display data write. The cursor is displayed using 5 dots in the 8th line (see Fig.12).

B

The character indicated by the cursor blinks when B = logic 1. The blink is displayed by switching between display characters and all dots on with a period of 1 second when f_{osc} = 150 kHz (Fig.12). At other clock frequencies the blink period is equal to 150 kHz/f_{osc}. The cursor and the blink can be set to display simultaneously.

Cursor or display shift

Cursor or Display Shift moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display. In 2 or 4-line displays, the cursor moves to the next line when it passes the last position (40 or 20 decimal) of the line. When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line. The address counter (AC) content does not change if the only action performed is shift display, but increments or decrements with the cursor shift.

Function set

DL (PARALLEL MODE ONLY)

Sets interface data width. Data is sent or received in bytes (DB7 to DB0) when DL = logic 1 or in two nibbles (DB7 to DB4) when DL = logic 0. When 4-bit width is selected, data is transmitted in two cycles using the parallel bus(1).

Function set from I²C-interface: DL bit can not bet set to 0 from the I²C-interface. If bit DL has been set to 0 via the parallel bus, programming via the I²C-interface is complicated.

N, M

Sets number of display lines.

G

Controls the V_{LCD} voltage generator characteristic.

Set CGRAM address

Set CGRAM Address sets bit 0 to 5 of the CGRAM address ACG into the address counter (binary $A_5A_4A_3A_2A_1A_0$). Data can then be written to or read from the CGRAM.

Only bits 0 to 5 of the CGRAM address are set by the set CGRAM address command. Bit 6 can be set using the set DDRAM address command or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the read BF and address command.

Set DDRAM address

Set DDRAM Address sets the DDRAM address into the address counter (binary $A_6A_5A_4A_3A_2A_1A_0$). Data can then be written to or read from the DDRAM.

Hexadecimal address ranges.

ADDRESS	FUNCTION
00 to 4F	1-line by 24; 2116
00 to 0B and 0C to 4F	2-line by 12; 2114
00 to 27 and 40 to 67	2-line by 24; 2114/2116
00 to 13, 20 to 33, 40 to 53 and 60 to 73	4-line by 12; 2114/2116

Read busy flag and address

Read Busy Flag and Address reads the busy flag (BF). BF = logic 1 indicates that an internal operation is in progress. The next instruction will not be executed if BF = 1. Check the BF status before sending the next instruction.

At the same time, the value of the address counter expressed in binary A_6 to A_0 is read out. The address counter is used by both CGRAM and DDRAM, and its value is determined by the previous instruction.

Write data to CGRAM or DDRAM

Writes binary 8-bit data D_7 to D_0 to the CGRAM or the DDRAM.

Whether the CGRAM or DDRAM is to be written into is determined by the previous specification of CGRAM or DDRAM address setting. After writing, the address automatically increments or decrements by 1, in accordance with the entry mode. Only bits D0 to D4 of CGRAM data are valid, bits D5 to D7 are 'don't care'.

(1) In a 4-bit application DB3 to DB0 are left open (internal pull-ups). Hence in the first function set instruction after power-on G and H are set to 1. A second function set must then be sent (2 nibbles) to set G and H to their required values.

Read data from CGRAM or DDRAM

Reads binary 8-bit data D_7 to D_0 from the CGRAM or DDRAM.

The most recent Set Address command determines whether the CGRAM or DDRAM is to be read.

The Read Data instruction gates the content of the data register (DR) to the bus while E = HIGH. After E goes LOW again, internal operation increments (or decrements) the AC and stores RAM data corresponding to the new AC into the DR.

Remark: the only three instructions that update the data register (DR) are:

- Set CGRAM Address
- Set DDRAM Address
- Read Data from CGRAM or DDRAM.

Other instructions (e.g. Write Data, Cursor/Display shift, Clear Display, Return Home) will not modify the data register content.

INTERFACE TO MPU (PARALLEL INTERFACE)

The PCF2116 can send data in either two 4-bit operations or one 8-bit operation and can thus interface to 4-bit or 8-bit microcontrollers.

In 8-bit mode data is transferred as 8-bit bytes using the 8 data lines DB0 to DB7. Three further control lines E, RS, and R/$\overline{W}$ are required.

In 4-bit mode data is transferred in two cycles of 4-bits each. The higher order bits (corresponding to DB4 to DB7 in 8-bit mode) are sent in the first cycle and the lower order bits (DB0 to DB3 in 8-bit mode) in the second. Data transfer is complete after two 4-bit data transfers. Note that two cycles are also required for the busy flag check. 4-bit operation is selected by instruction. See Figs 18, 19 and 20 for examples of bus protocol.

In 4-bit mode pins DB3 to DB0 must be left open-circuit. They are pulled up to V_{DD} internally.

INTERFACE TO MPU: I²C-BUS INTERFACE

Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF2116 READ and WRITE cycles is shown in Figs 25 to 27.

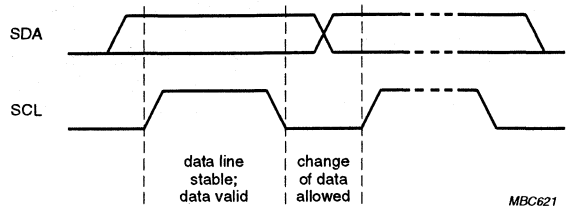


Fig.21 Bit transfer.

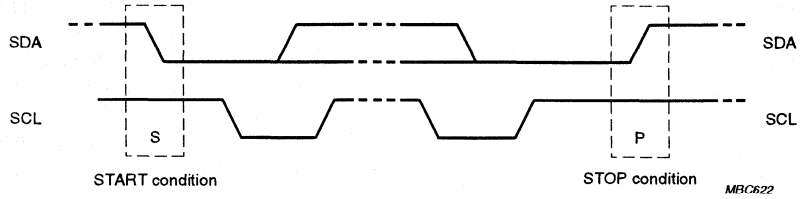


Fig.22 Definition of start and stop conditions.

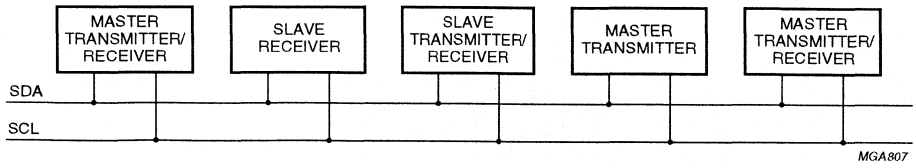


Fig.23 System configuration.

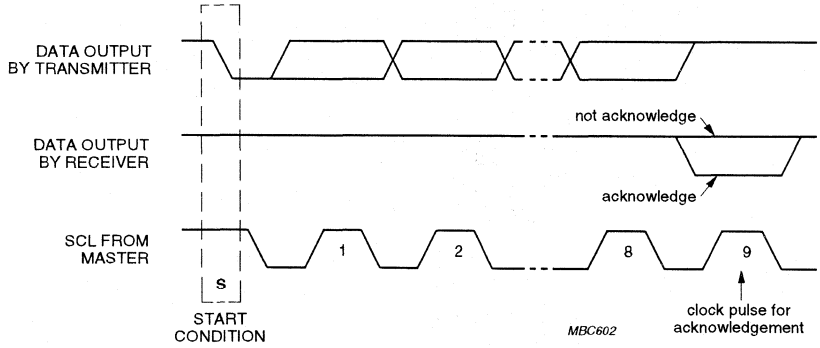


Fig.24 Acknowledgement on the I²C-bus.

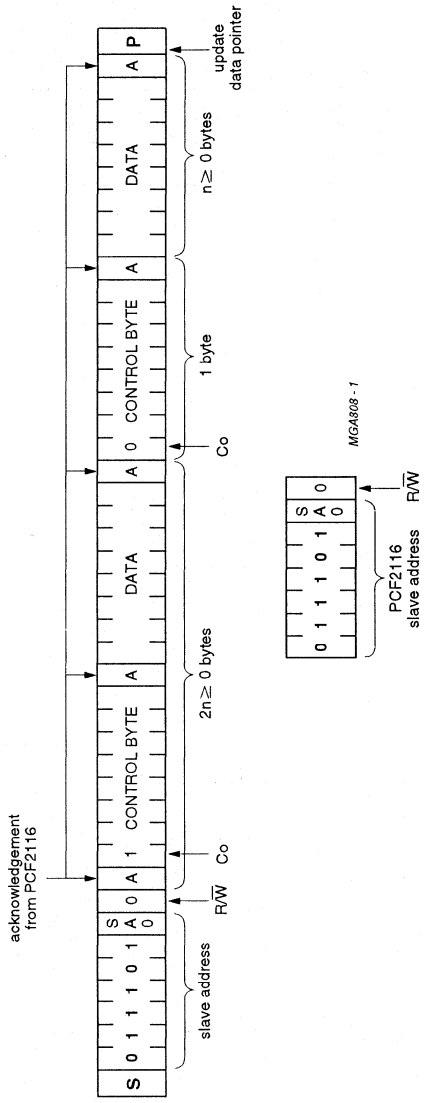


Fig.25 Master transmits to slave receiver; WRITE mode.

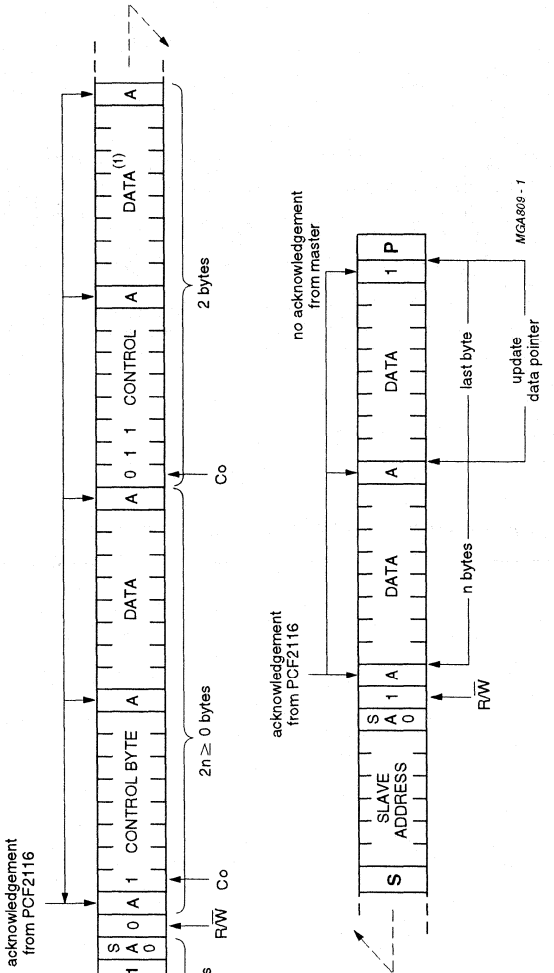


Fig.26 Master reads after setting word address; write word address, set RS/$\overline{RW}$; READ data.

(1) Last data byte is a dummy byte (may be omitted).

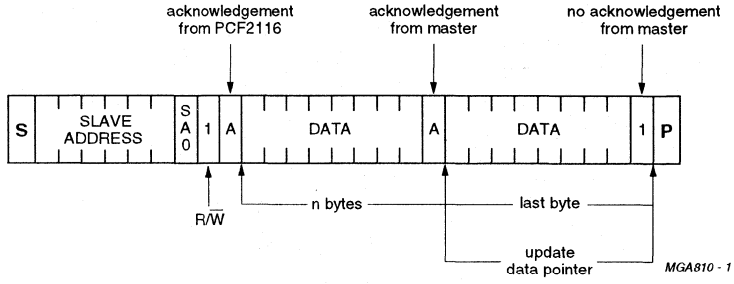


Fig.27 Master reads slave immediately after first byte; READ mode (RS previously defined).

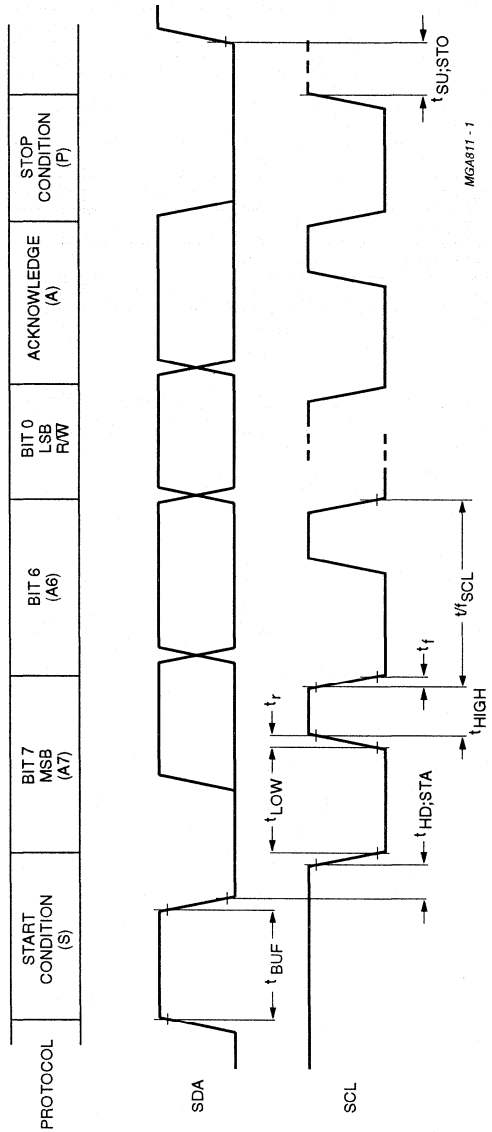


Fig.28 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+8	V
V_{LCD}	LCD supply voltage	V_{DD} − 11	V_{DD}	V
V_I	input voltage OSC, V_0, RS, R/$\overline{W}$, E and DB0 to DB7	V_{SS} − 0.5	V_{DD} + 0.5	V
V_O	output voltage R1 to R32, C1 to C60 and V_{LCD}	V_{LCD} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	−50	+50	mA
P_{tot}	total power dissipation	−	400	mW
P_O	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 to V_{DD} − 9 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2.5	–	6	V
V_{LCD}	LCD supply voltage		V_{DD} − 9	–	V_{DD} − 3.5	V
I_{DD}	supply current external V_{LCD}	note 1				
I_{DD1}	supply current 1		–	200	500	μA
I_{DD2}	supply current 2	V_{DD} = 5 V; V_{OP} = 9 V; f_{osc} = 150 kHz; T_{amb} = 25 °C	–	200	300	μA
I_{DD3}	supply current 3	V_{DD} = 3 V; V_{OP} = 5 V; f_{osc} = 150 kHz; T_{amb} = 25 °C	–	150	200	μA
I_{DD}	supply current internal V_{LCD}	notes 1, 2 and 8				
I_{DD4}	supply current 4		–	700	1100	μA
I_{DD5}	supply current 5	V_{DD} = 5 V; V_{OP} = 9 V; f_{osc} = 150 kHz; T_{amb} = 25 °C	–	600	900	μA
I_{DD6}	supply current 6	V_{DD} = 3 V; V_{OP} = 5 V; f_{osc} = 150 kHz; T_{amb} = 25 °C	–	500	800	μA
I_{LCD}	V_{LCD} input current	notes 1 and 7	–	50	100	μA
V_{POR}	power-on reset voltage level	note 3	–	1.3	1.8	V
Logic						
V_{IL1}	LOW level input voltage E, RS, R/$\overline{W}$, DB0 to DB7 and SA0		V_{SS}	–	0.3V_{DD}	V
V_{IH1}	HIGH level input voltage E, RS, R/$\overline{W}$, DB0 to DB7 and SA0		0.7V_{DD}	–	V_{DD}	V
V_{oscL}	LOW level input voltage OSC		V_{SS}	–	V_{DD} − 1.5	V
V_{oscH}	HIGH level input voltage OSC		V_{DD} − 0.1	–	V_{DD}	V
V_{V0L}	LOW level input voltage V_0		V_{SS}	–	V_{DD} − 0.5	V
V_{V0H}	HIGH level input voltage V_0		V_{DD} − 0.05	–	V_{DD}	V
I_{pu}	pull-up current at DB0 to DB7	V_I = V_{SS}	0.04	0.15	1.00	μA
I_{OL1}	LOW level output current DB0 to DB7	V_{OL} = 0.4 V; V_{DD} = 5 V	1.6	–	–	mA
I_{OH}	HIGH level output current DB0 to DB7	V_{OH} = 4 V; V_{DD} = 5 V	−1.0	–	–	mA
I_{L1}	leakage current OSC, V_0, E, RS, R/$\overline{W}$, DB0 to DB7 and SA0	V_I = V_{DD} or V_{SS}	−1	–	+1	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I^2C-bus						
SDA, SCL						
V_{IL2}	LOW level input voltage	note 4	V_{SS}	–	$0.3V_{DD}$	V
V_{IH2}	HIGH level input voltage	note 4	$0.7V_{DD}$	–	V_{DD}	V
I_{L2}	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	μA
C_I	input capacitance	note 5	–	–	7	pF
I_{OL2}	LOW level output current (SDA)	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
LCD outputs						
R_{ROW}	row output resistance R1 to R32	note 6	–	1.5	3	kΩ
R_{COL}	column output resistance C1 to C60	note 6	–	3	6	kΩ
V_{tol1}	bias tolerance R1 to R32 and C1 to C60	note 7	–	±20	±130	mV
V_{tol2}	V_{LCD} tolerance	note 2	–	±40	±300	mV

Notes

1. LCD outputs are open-circuit; inputs at V_{DD} or V_{SS}; $V_0 = V_{DD}$; bus inactive; internal or external clock with duty cycle 50% (I_{DD1} only).
2. LCD outputs are open-circuit; HV generator is on; load current at V_{LCD} = 20 μA.
3. Resets all logic when $V_{DD} < V_{POR}$.
4. When the voltages are above or below the supply voltages V_{DD} or V_{SS}, an input current may flow; this current must not exceed ±0.5 mA.
5. Tested on sample basis.
6. Resistance of output terminals (R1 to R32 and C1 to C60) with load current = 150 μA; $V_{OP} = V_{DD} - V_{LCD}$ = 9 V; outputs measured one at a time; (external V_{LCD}).
7. LCD outputs open-circuit; external V_{LCD}.
8. Maximum value occurs at 85 °C.

AC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9 V; T_{amb} = −40 °C to + 85 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
f_{FR}	LCD frame frequency (internal clock); note 1	40	65	100	Hz
f_{osc}	external clock frequency	90	150	225	kHz
Bus timing characteristics: Parallel Interface; notes 1 and 2					
WRITE OPERATION (WRITING DATA FROM MPU TO PCF2116)					
T_{cy}	enable cycle time	500	–	–	ns
PW_{EH}	enable pulse width	220	–	–	ns
t_{ASU}	address set-up time	50	–	–	ns
t_{AH}	address hold time	25	–	–	ns
t_{DSW}	data set-up time	60	–	–	ns
t_{HD}	data hold time	25	–	–	ns
READ OPERATION (READING DATA FROM PCF2116 TO MPU)					
T_{cy}	enable cycle time	500	–	–	ns
PW_{EH}	enable pulse width	220	–	–	ns
t_{ASU}	address set-up time	50	–	–	ns
t_{AH}	address hold time	25	–	–	ns
t_{DHD}	data delay time	–	–	150	ns
t_{HD}	data hold time	20	–	100	ns
Timing characteristics: I^2C-bus interface; note 2					
f_{SCL}	SCL clock frequency	–	–	100	kHz
t_{SW}	tolerable spike width on bus	–	–	100	ns
t_{BUF}	bus free time	4.7	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition	4.7	–	–	µs
$t_{HD;STA}$	start condition hold time	4	–	–	µs
t_{LOW}	SCL LOW time	4.7	–	–	µs
t_{HIGH}	SCL HIGH time	4	–	–	µs
t_r	SCL and SDA rise time	–	–	1	µs
t_f	SCL and SDA fall time	–	–	0.3	µs
$t_{SU;DAT}$	data set-up time	250	–	–	ns
$t_{HD;DAT}$	data hold time	0	–	–	ns
$t_{SU;STO}$	set-up time for STOP condition	4	–	–	µs

Notes

1. V_{DD} = 5.0 V.
2. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

TIMING CHARACTERISTICS

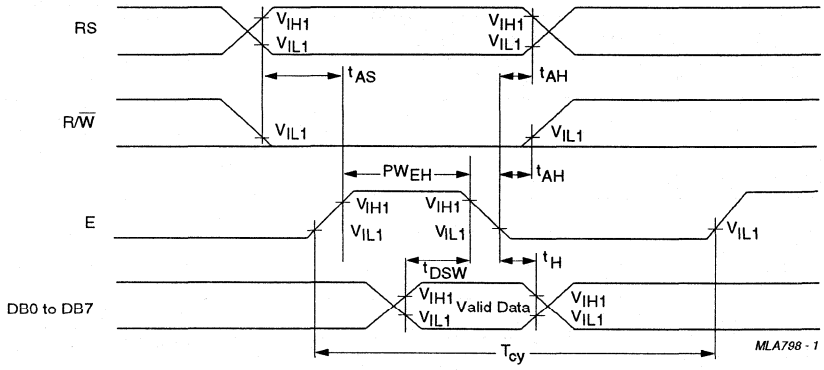


Fig.29 Parallel bus write operation sequence; writing data from MPU to PCF2116.

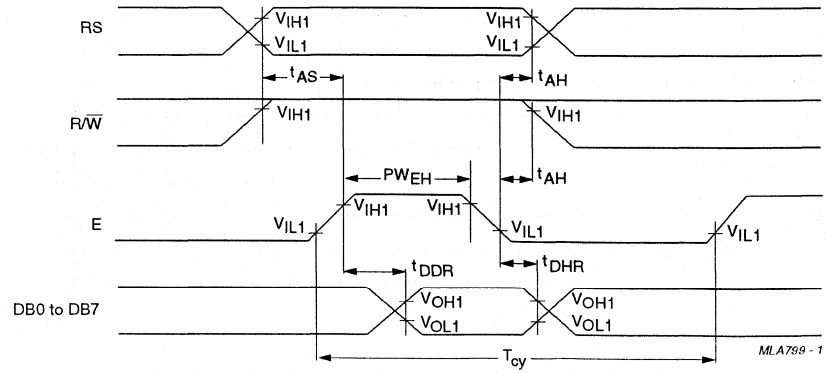


Fig.30 Parallel bus read operation sequence; reading data from PCF2116 to MPU.

APPLICATION INFORMATION

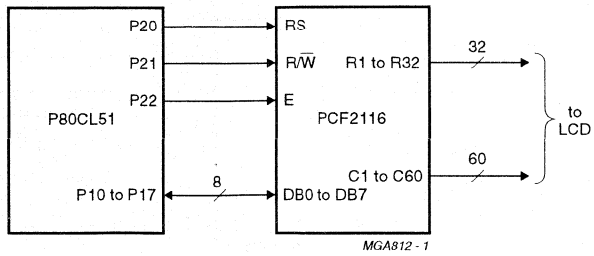


Fig.31 Direct connection to 8-bit MPU; 8-bit bus.

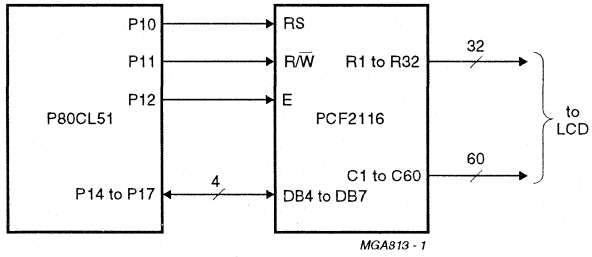


Fig.32 Direct connection to 8-bit MPU; 4-bit bus.

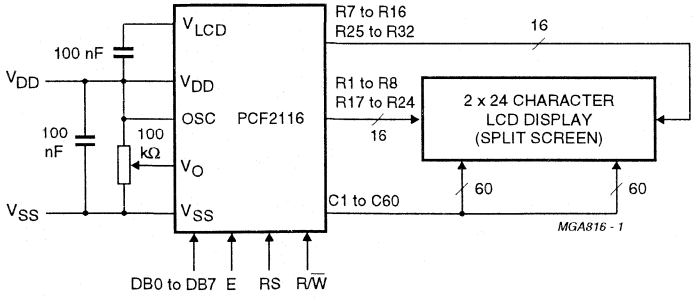


Fig.33 Typical application using parallel interface.

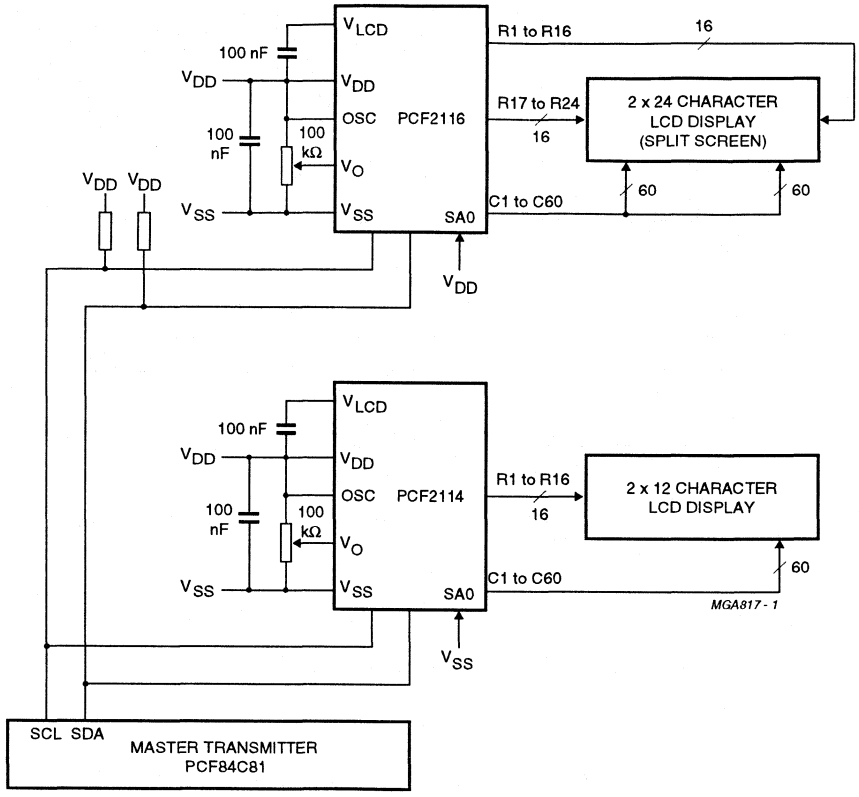


Fig.34 Application using I²C-bus interface.

8-bit operation, 1-line display using internal reset

Table 6 shows an example of a 1-line display in 8-bit operation. The PCF2116 functions must be set by the function set instruction prior to display. Since the display data RAM can store data for 80 characters, the RAM can be used for advertising displays when combined with display shift operation. Since the display shift operation changes display position only and DDRAM contents remain unchanged, display data entered first can be displayed when the Return Home operation is performed.

4-bit operation, 1-line display using internal reset

The program must set functions prior to 4-bit operation. Table 5 shows an example. When power is turned on, 8-bit operation is automatically selected and the PCF2116 attempts to perform the first write as an 8-bit operation. Since nothing is connected to DB0 to DB3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is required to set the functions (see Table 5 step 3).

Thus, DB4 to DB7 of the function set are written twice.

8-bit operation, 2-line display

For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be set after the eighth character is completed (see Table 7). Note that both lines of the display are always shifted together; data does not shift from one line to the other.

I²C operation, 1-line display

A control byte is required with most commands (see Table 8).

Initializing by instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, the PCF2116 must be initialized by instruction. Tables 9 and 10 show how this may be performed for 8-bit and 4-bit operation.

Table 5 4-bit operation, 1-line display example; using internal reset.

STEP	INSTRUCTION						DISPLAY	OPERATION
1	Power supply on (PCF2116 is initialized by the internal reset circuit).							Initialized. No display appears.
2	Function set							
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4		Sets to 4-bit operation. In this instance operation is handled as 8-bits by initialization and only this instruction completes with one write.
	0	0	0	0	1	0		
3	Function set							
	0	0	0	0	1	0		Sets to 4-bit operation, selects 1-line display and $V_{LCD} = V_0$. 4-bit operation starts from this point and resetting is needed.
	0	0	0	0	0	0		
4	Display on/off control							
	0	0	0	0	0	0	_	Turns on display and cursor. Entire display is blank after initialization.
	0	0	1	1	1	0		
5	Entry mode set							
	0	0	0	0	0	0	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted.
	0	0	0	1	1	0		
6	Write data to CGRAM/DDRAM							
	1	0	0	1	0	1	P_	Writes 'P'. The DDRAM has already been selected by initialization at power-on. The cursor is incremented by 1 and shifted to the right.
	1	0	0	0	0	0		

Table 6 8-bit operation, 1-line display example; using internal reset (character set 'A').

STEP	INSTRUCTION	DISPLAY	OPERATION
1	Power supply on (PCF2116 is initialized by the internal reset function).		Initialized. No display appears.
2	Function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		Sets to 8-bit operation, selects 1-line display and $V_{LCD} = V_0$.
3	Display mode on/off control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is blank after initialization.
4	Entry mode set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM. Display is not shifted.
5	Write data to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	Writes 'P'. The DDRAM has already been selected by initialization at power-on. The cursor is incremented by 1 and shifted to the right.
6	Write data to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0	**PH**_	Writes 'H'.
7			
8	Write data to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS**_	Writes 'S'.
9	Entry mode set 0 0 0 0 0 0 0 1 1 1	**PHILIPS**_	Sets mode for display shift at the time of write.
10	Write data to CGRAM/DDRAM 1 0 0 0 1 0 0 0 0 0	**HILIPS** _	Writes space.
11	Write data to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**ILIPS M**_	Writes 'M'.

STEP	INSTRUCTION	DISPLAY	OPERATION
12			
13	Write data to CGRAM/DDRAM 1 0 0 1 0 0 1 1 1 1	**MICROKO_**	Writes 'O'.
14	Cursor or display shift 0 0 0 0 0 1 0 0 0 0	**MICROKO**	Shifts only the cursor position to the left.
15	Cursor or display shift 0 0 0 0 0 1 0 0 0 0	**MICROKO**	Shifts only the cursor position to the left.
16	Write data to CGRAM/DDRAM 1 0 0 1 0 0 0 0 1 1	**ICROCO**	Writes 'C' correction. The display moves to the left.
17	Cursor or display shift 0 0 0 0 0 1 1 1 0 0	**MICROCO**	Shifts the display and cursor to the right.
18	Cursor or display shift 0 0 0 0 0 1 0 1 0 0	**MICROCO_**	Shifts only the cursor to the right.
19	Write data to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**ICROCOM_**	Writes 'M'.
20			
21	Return Home 0 0 0 0 0 0 0 0 1 0	**PHILIPS M**	Returns both display and cursor to the original position (address 0).

Table 7 8-bit operation, 2-line display example; using internal reset.

STEP	INSTRUCTION	DISPLAY	OPERATION
1	Power supply on (PCF2116 is initialized by the internal reset function).		Initialized. No display appears.
2	Function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 1 0 0 0		Sets to 8-bit operation, selects 2-line display and voltage generator off.
3	Display on/off control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is blank after initialization.
4	Entry mode set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the CG/DDRAM. Display is not shifted.
5	Write data to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	Writes 'P'. The DDRAM has already been selected by initialization at power-on. The cursor is incremented by 1 and shifted to the right.
6			
7	Write data to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS**_	Writes 'S'.
8	Set DDRAM address 0 0 1 1 0 0 0 0 0 0	**PHILIPS** _	Sets DDRAM address to position the cursor at the head of the 2nd line.
9	Write data to CGRAM/ DDRAM 1 0 0 1 0 0 1 1 0 1	**PHILIPS** **M**_	Writes 'M'.
10			

STEP	INSTRUCTION	DISPLAY	OPERATION
11	Write data to CGRAM/ DDRAM 1 0 0 1 0 0 1 1 1 1	PHILIPS MICROCO_	Writes 'O'.
12	Write data to CGRAM/ DDRAM 0 0 0 0 0 0 0 1 1 1	PHILIPS MICROCO_	Sets mode for display shift at the time of write.
13	Write data to CGRAM/ DDRAM 1 0 0 1 0 0 1 1 0 1	HILIPS ICROCOM_	Writes 'M'. Display is shifted to the left. The first and second lines shift together.
14			
15	Return Home 0 0 0 0 0 0 0 0 1 0	PHILIPS MICROCOM	Returns both display and cursor to the original position (address 0).

Table 8 Example of I²C operation; 1-line display (using internal reset, assuming SA0 = V_{SS}; note 1).

STEP	I²C BYTE	DISPLAY	OPERATION
1	I²C start		Initialized. No display appears.
2	Slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1		During the acknowledge cycle SDA will be pulled-down by the PCF2116.
3	Send a control byte for function set Co RS R/$\overline{W}$ Ack 0 0 0 X X X X X 1		Control byte sets RS and R/$\overline{W}$ for following data bytes.
4	Function set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 1 X 0 0 0 0 1		Selects 1-line display and $V_{LCD} = V_0$; SCL pulse during acknowledge cycle starts execution of instruction.
5	Display on/off control DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 1 1 1 0 1	_	Turns on display and cursor. Entire display shows character hex 20 (blank in ASCII-like character sets).
6	Entry mode set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 1 1 0 1	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DDRAM or CGRAM. Display is not shifted.
7	I²C start	_	For writing data to DDRAM, RS must be set to 1. Therefore a control byte is needed.
8	Slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1	_	
9	Send a control byte for write data Co RS R/$\overline{W}$ Ack 0 1 0 X X X X X 1	_	
10	Write data to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 0 0 1	P_	Writes 'P'. The DDRAM has been selected at power-up. The cursor is incremented by 1 and shifted to the right.

STEP	I²C BYTE	DISPLAY	OPERATION
11	Write data to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 1	PH_	Writes 'H'.
12 to 15			
16	Write data to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 1 1 1	PHILIPS_	Writes 'S'.
17	(optional I²C stop) I²C start + slave address for write (as step 8)	PHILIPS_	
18	Control byte Co RS R/$\overline{W}$ Ack 1 0 0 X X X X X 1	PHILIPS_	
19	Return Home DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 0 1 0 1	PHILIPS	Sets DDRAM address 0 in address counter. (also returns shifted display to original position. DDRAM contents unchanged). This instruction does not update the Data Register (DR).
20	Control byte for read Co RS R/$\overline{W}$ Ack 0 1 1 X X X X X 1	PHILIPS	DDRAM content will be read from following instructions. The R/$\overline{W}$ has to be set to 1 while still in I²C-write mode.
21	I²C start	PHILIPS	
22	Slave address for read SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 1 1	PHILIPS	During the acknowledge cycle the content of the DR is loaded into the internal I²C interface to be shifted out. In the previous instruction neither a Set Address nor a Read Data has been performed. Therefore the content of the DR was unknown.
23	Read data: 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack X X X X X X X X 0	PHILIPS	8 × SCL; content loaded into interface during previous acknowledge cycle is shifted out over SDA. MSB is DB7. During master acknowledge content of DDRAM address 01 is loaded into the I²C interface.

STEP	I²C BYTE	DISPLAY	OPERATION
24	Read data: 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 0	PHILIPS	8 × SCL; code of letter 'H' is read first. During master acknowledge code of 'I' is loaded into the I²C interface.
25	Read data: 8 × SCL + no master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 1 1	PHILIPS	No master acknowledge; After the content of the I²C interface register is shifted out no internal action is performed. No new data is loaded to the interface register, Data Register (DR) is not updated, Address Counter (AC) is not incremented and cursor is not shifted.
26	I²C stop	PHILIPS	

Notes

1. X = don't care.
2. SDA is left at high-impedance by the microcontroller during the READ acknowledge.

Table 9 Initialization by instruction, 8-bit interface (note 1).

STEP										DESCRIPTION
power-on or unknown state										
|										
wait 2 ms after V_{DD} rises above V_{POR}										
|										
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction.
0	0	0	0	1	1	X	X	X	X	Function set (interface is 8-bits long).
|										
wait 2 ms										
|										
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction.
0	0	0	0	1	1	X	X	X	X	Function set (interface is 8-bits long).
|										
wait more than 40 µs										
|										
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction.
0	0	0	0	1	1	X	X	X	X	Function set (interface is 8-bits long).
|										BF can be checked after the following instructions. When BF is not checked, the waiting time between instructions is the specified instruction time (see Table 3).
|										
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function set (interface is 8-bits long). Specify the number of display lines and voltage generator characteristic.
0	0	0	0	1	1	N	M	G	0	
0	0	0	0	0	0	1	0	0	0	Display off.
0	0	0	0	0	0	0	0	0	1	Clear display.
0	0	0	0	0	0	0	1	I/D	S	Entry mode set.
|										
Initialization ends										

Note

1. X = don't care.

Table 10 Initialization by instruction, 4-bit interface. Not applicable for I²C-bus operation.

STEP						DESCRIPTION
power-on or unknown state						
wait 2 ms after V_{DD} rises above V_{POR}						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction.
0	0	0	0	1	1	Function set (interface is 8-bits long).
wait 2 ms						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction.
0	0	0	0	1	1	Function set (interface is 8-bits long).
wait 40 μs						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction.
0	0	0	0	1	1	Function set (interface is 8-bits long).
						BF can be checked after the following instructions. When BF is not checked, the waiting time between instructions is the specified instruction time. (See Table 3).
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	Function set (set interface to 4-bits long).
0	0	0	0	1	0	Interface is 8-bits long.
0	0	0	0	1	0	Function set (interface is 4-bits long).
0	0	N	M	G	0	Specify number of display lines and voltage generator characteristic.
0	0	0	0	0	0	
0	0	1	0	0	0	Display off.
0	0	0	0	0	0	Clear display.
0	0	0	0	0	1	
0	0	0	0	0	0	Entry mode set.
0	0	0	1	I/D	S	
Initialization ends						

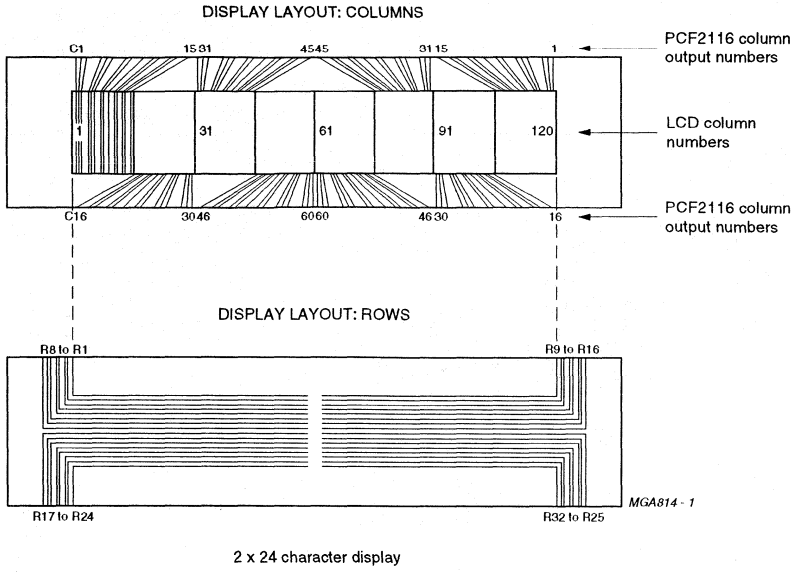


Fig.35 Example of 2 x 24 display layout (PCF2116).

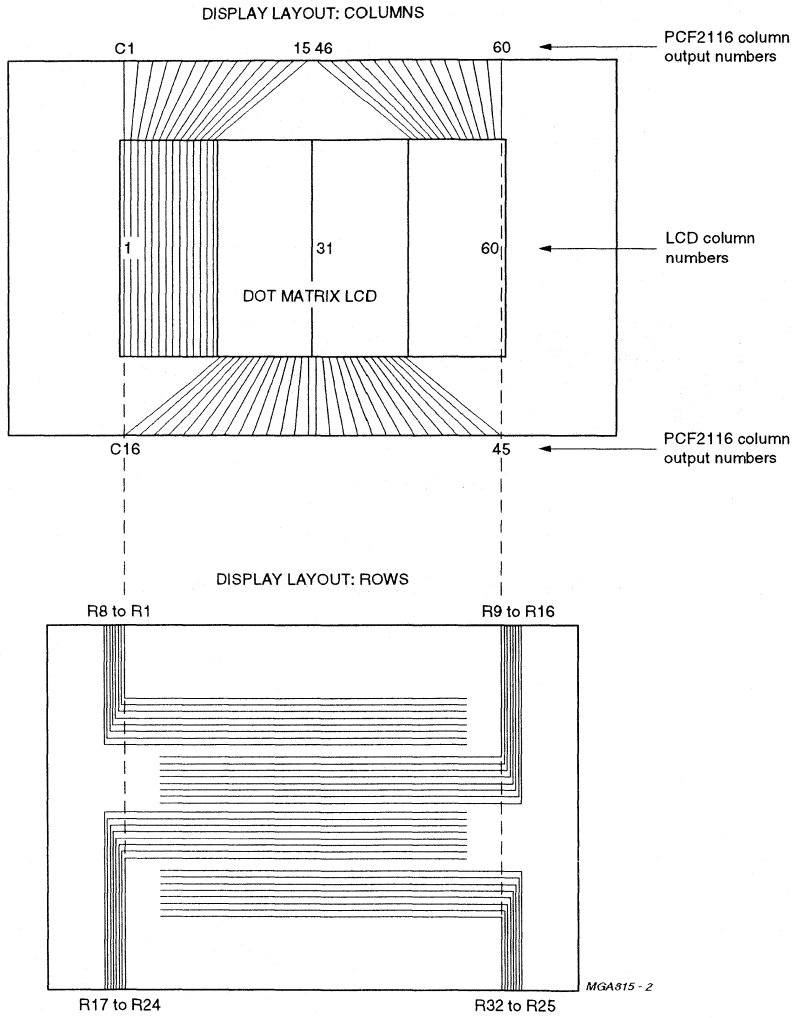


Fig.36 Example of 4 × 12 display layout (PCF2114/PCF2116).

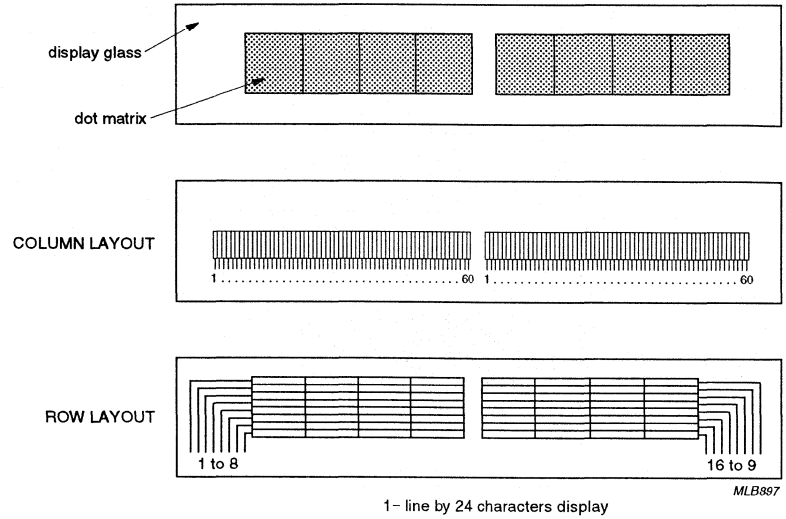


Fig.37 Display example (PCF2114); 1-line by 24 characters.

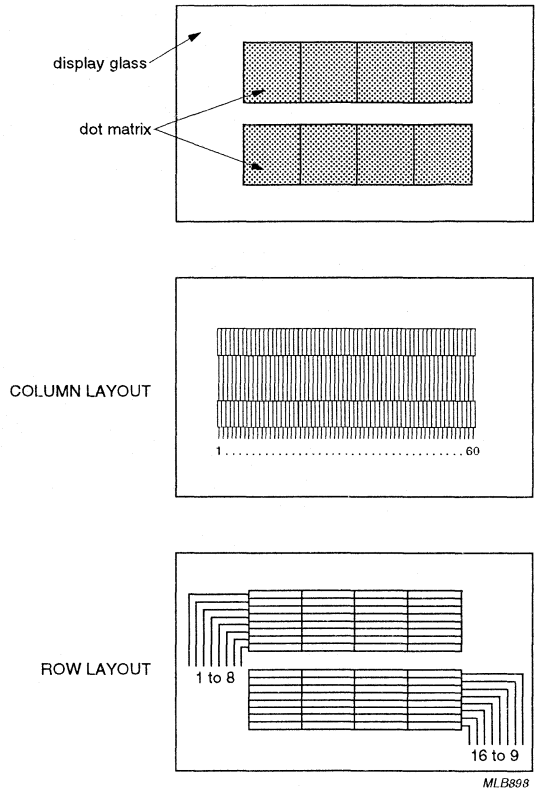


Fig.38 Display example (PCF2114); 2-lines by 12 characters.

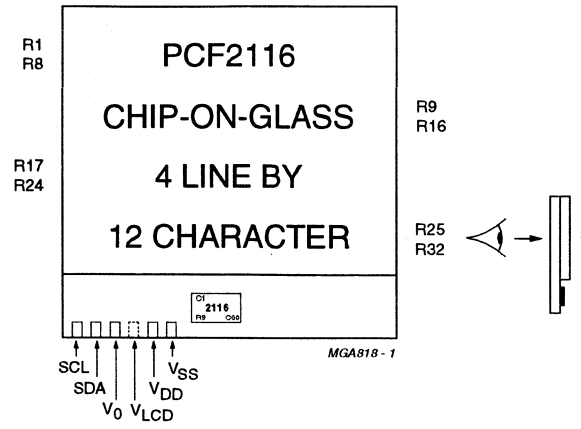
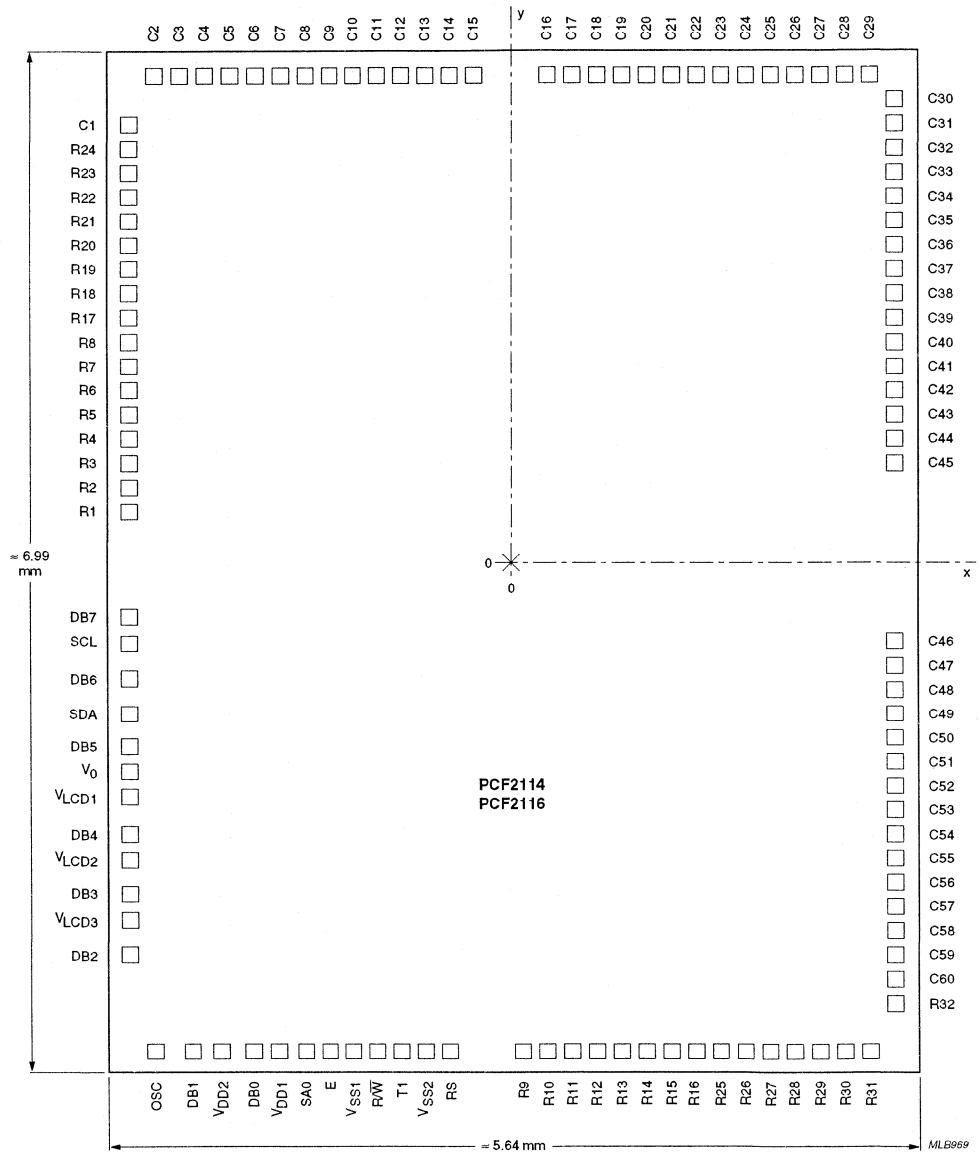


Fig.39 Chip on glass application.

BONDING PAD LOCATIONS



Chip dimensions: approximately 5.64 × 6.99 mm.
Pad area: 0.0121 mm^2.
Bonding pad dimensions: 110 × 110 µm.

Fig.40 Bonding pad locations.

Table 11 Bonding pad locations (dimensions in μm). All x/y coordinates are referenced to centre of chip, see Fig.40.

SYMBOL	PAD	x	y
OSC	1	−2445	−3300
DB1	2	−2211	−3300
V_{DD2}	3	−2034	−3300
DB0	4	−1806	−3300
V_{DD1}	5	−1627	−3300
SA0	6	−1437	−3300
E	7	−1245	−3300
V_{SS1}	8	−1056	−3300
$R/\overline{W}$	9	−867	−3300
T1	10	−672	−3300
V_{SS2}	11	−486	−3300
RS	12	−297	−3300
R9	13	77	−3300
R10	14	247	−3300
R11	15	417	−3300
R12	16	587	−3300
R13	17	757	−3300
R14	18	927	−3300
R15	19	1097	−3300
R16	20	1267	−3300
R25	21	1436	−3300
R26	22	1606	−3300
R27	23	1776	−3300
R28	24	1946	−3300
R29	25	2116	−3300
R30	26	2286	−3300
R31	27	2456	−3300
R32	28	2626	−3013
C60	29	2626	−2760
C59	30	2626	−2590
C58	31	2626	−2420
C57	32	2626	−2250
C56	33	2626	−2080
C55	34	2626	−1910
C54	35	2626	−1740
C53	36	2626	−1570
C52	37	2626	−1400
C51	38	2626	−1230

SYMBOL	PAD	x	y
C50	39	2626	−1060
C49	40	2626	−890
C48	41	2626	−720
C47	42	2626	−550
C46	43	2626	−380
C45	44	2626	582
C44	45	2626	752
C43	46	2626	922
C42	47	2626	1092
C41	48	2626	1262
C40	49	2626	1432
C39	50	2626	1602
C38	51	2626	1772
C37	52	2626	1942
C36	53	2626	2112
C35	54	2626	2282
C34	55	2626	2452
C33	56	2626	2622
C32	57	2626	2792
C31	58	2626	2962
C30	59	2626	3132
C29	60	2339	3302
C28	61	2169	3302
C27	62	1999	3302
C26	63	1829	3302
C25	64	1659	3302
C24	65	1489	3302
C23	66	1319	3302
C22	67	1149	3302
C21	68	979	3302
C20	69	809	3302
C19	70	639	3302
C18	71	469	3302
C17	72	299	3302
C16	73	129	3302
C15	74	−245	3302
C14	75	−415	3302
C13	76	−585	3302

SYMBOL	PAD	x	y
C12	77	–755	3302
C11	78	–925	3302
C10	79	–1095	3302
C9	80	–1265	3302
C8	81	–1435	3302
C7	82	–1605	3302
C6	83	–1775	3302
C5	84	–1945	3302
C4	85	–2115	3302
C3	86	–2285	3302
C2	87	–2455	3302
C1	88	–2625	3015
R24	89	–2625	2846
R23	90	–2625	2676
R22	91	–2625	2506
R21	92	–2625	2336
R20	93	–2625	2166
R19	94	–2625	1996
R18	95	–2625	1826
R17	96	–2625	1656
R8	97	–2625	1487
R7	98	–2625	1317
R6	99	–2625	1147
R5	100	–2625	977
R4	101	–2625	807
R3	102	–2625	637
R2	103	–2625	467
R1	104	–2625	297
DB7	105	–2625	–290
SCL	106	–2625	–479
DB6	107	–2625	–716
SDA	108	–2625	–976
DB5	109	–2625	–1202
V_0	110	–2625	–1388
V_{LCD1}	111	–2625	–1580
DB4	112	–2625	–1808
V_{LCD2}	113	–2625	–1985
DB3	114	–2625	–2213
V_{LCD3}	115	–2625	–2390
DB2	116	–2625	–2621

LCD drivers PCF21XXC family

FEATURES

- Supply voltage 2.25 to 6.0 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Stand-alone or expanded system
- Power-on reset clear
- LCD segments
  - 40 (PCF2100C)
  - 64 (PCF2111C)
  - 32 (PCF2112C)
- Multiplex rate
  - 1 : 2 (PCF2100C)
  - 1 : 2 (PCF2111C)
  - 1 : 1 (PCF2112C)
- Word length
  - 22 bits (PCF2100C)
  - 34 bits (PCF2111C)
  - 34 bits (PCF2112C).

GENERAL DESCRIPTION

The members of the PCF21XXC family are single-chip, silicon gate CMOS circuits. A 3-line bus (CBUS) structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

The PCF21XXC family chips have the same function and performance as those of the PCF21XX family. The voltage is reduced from 6.5 to 6.0 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.25	–	6.0	V
I_{DD1}	supply current 1	outputs open; CBUS inactive	–	20	50	µA
I_{DD2}	supply current 2	outputs open; CBUS inactive; T_{amb} = 25 °C	–	20	30	µA
P_O	power dissipation per output		–	–	100	mW
T_{amb}	operating ambient temperature		–40	–	+85	°C
T_{stg}	storage temperature		–65	–	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2100CP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCF2100CT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCF2111CP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF2111CT	VSO40	plastic very small outline package; 40 leads	SOT158-1
PCF2112CP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF2112CT	VSO40	plastic very small outline package; 40 leads	SOT158-1

BLOCK DIAGRAMS

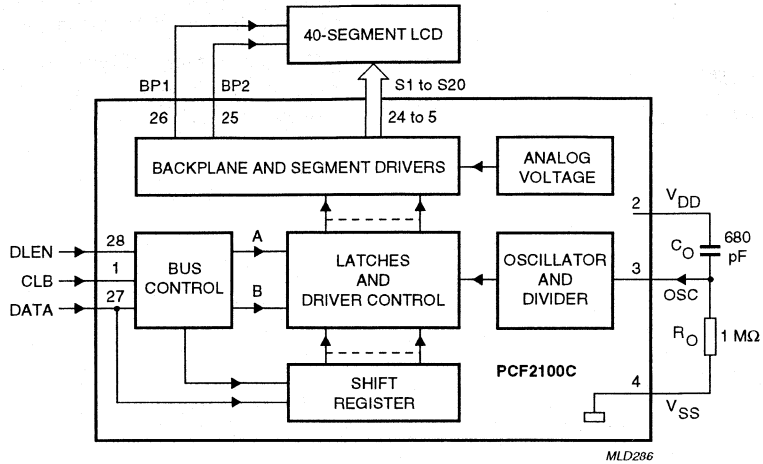


Fig.1 Block diagram; PCF2100C.

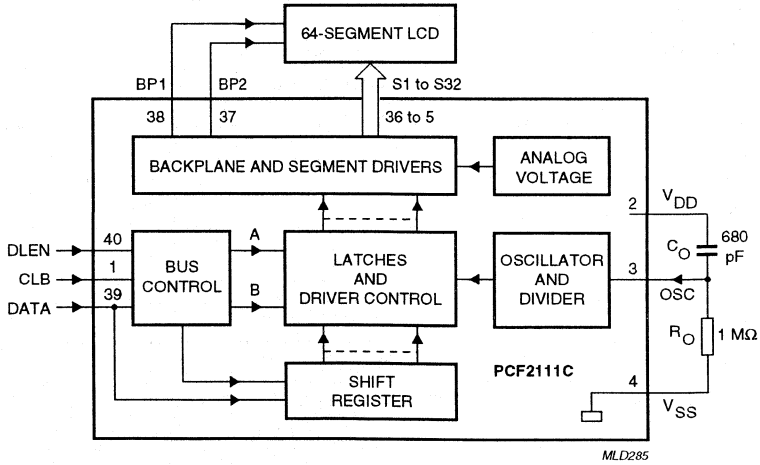


Fig.2 Block diagram; PCF2111C.

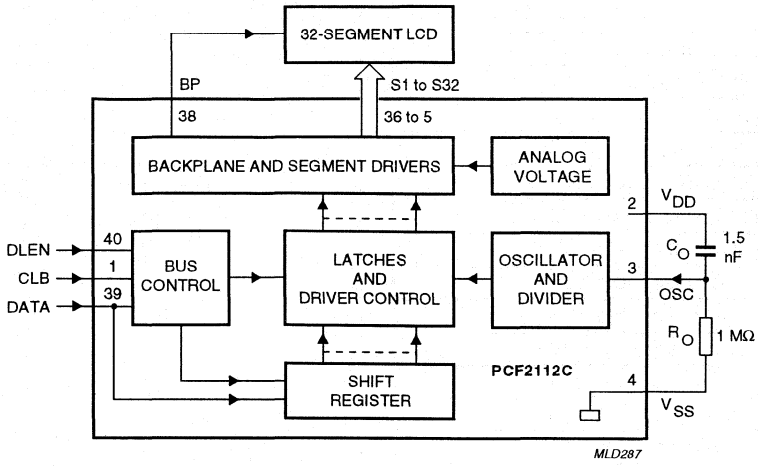


Fig.3 Block diagram; PCF2112C.

PINNING

PCF2100C

SYMBOL	PIN	DESCRIPTION
CLB	1	clock burst input (CBUS)
V_{DD}	2	supply voltage
OSC	3	oscillator input
V_{SS}	4	supply voltage ground
S20	5	LCD driver output 20
S19	6	LCD driver output 19
S18	7	LCD driver output 18
S17	8	LCD driver output 17
S16	9	LCD driver output 16
S15	10	LCD driver output 15
S14	11	LCD driver output 14
S13	12	LCD driver output 13
S12	13	LCD driver output 12
S11	14	LCD driver output 11
S10	15	LCD driver output 10
S9	16	LCD driver output 9
S8	17	LCD driver output 8
S7	18	LCD driver output 7
S6	19	LCD driver output 6
S5	20	LCD driver output 5
S4	21	LCD driver output 4
S3	22	LCD driver output 3
S2	23	LCD driver output 2
S1	24	LCD driver output 1
BP2	25	backplane driver output 2
BP1	26	backplane driver output 1
DATA	27	date input line (CBUS)
DLEN	28	data input line enable (CBUS)

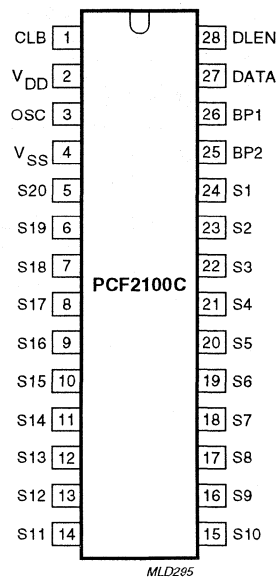


Fig.4 Pin configuration; SOT117-1 and SOT136-1.

PCF2111C

SYMBOL	PIN	DESCRIPTION
CLB	1	clock burst input (CBUS)
V_{DD}	2	supply voltage
OSC	3	oscillator input
V_{SS}	4	supply voltage ground
S32	5	LCD driver output 32
S31	6	LCD driver output 31
S30	7	LCD driver output 30
S29	8	LCD driver output 29
S28	9	LCD driver output 28
S27	10	LCD driver output 27
S26	11	LCD driver output 26
S25	12	LCD driver output 25
S24	13	LCD driver output 24
S23	14	LCD driver output 23
S22	15	LCD driver output 22
S21	16	LCD driver output 21
S20	17	LCD driver output 20
S19	18	LCD driver output 19
S18	19	LCD driver output 18
S17	20	LCD driver output 17
S16	21	LCD driver output 16
S15	22	LCD driver output 15
S14	23	LCD driver output 14
S13	24	LCD driver output 13
S12	25	LCD driver output 12
S11	26	LCD driver output 11
S10	27	LCD driver output 10
S9	28	LCD driver output 9
S8	29	LCD driver output 8
S7	30	LCD driver output 7
S6	31	LCD driver output 6
S5	32	LCD driver output 5
S4	33	LCD driver output 4
S3	34	LCD driver output 3
S2	35	LCD driver output 2
S1	36	LCD driver output 1
BP2	37	backplane driver output 2
BP1	38	backplane driver output 1
DATA	39	date input line (CBUS)
DLEN	40	data input line enable (CBUS)

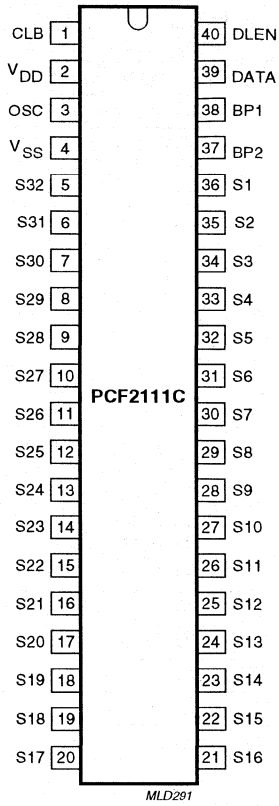


Fig.5 Pin configuration; SOT129-1 and SOT158-1.

PCF2112C

SYMBOL	PIN	DESCRIPTION
CLB	1	clock burst input (CBUS)
V_{DD}	2	supply voltage
OSC	3	oscillator input
V_{SS}	4	supply voltage ground
S32	5	LCD driver output 32
S31	6	LCD driver output 31
S30	7	LCD driver output 30
S29	8	LCD driver output 29
S28	9	LCD driver output 28
S27	10	LCD driver output 27
S26	11	LCD driver output 26
S25	12	LCD driver output 25
S24	13	LCD driver output 24
S23	14	LCD driver output 23
S22	15	LCD driver output 22
S21	16	LCD driver output 21
S20	17	LCD driver output 20
S19	18	LCD driver output 19
S18	19	LCD driver output 18
S17	20	LCD driver output 17
S16	21	LCD driver output 16
S15	22	LCD driver output 15
S14	23	LCD driver output 14
S13	24	LCD driver output 13
S12	25	LCD driver output 12
S11	26	LCD driver output 11
S10	27	LCD driver output 10
S9	28	LCD driver output 9
S8	29	LCD driver output 8
S7	30	LCD driver output 7
S6	31	LCD driver output 6
S5	32	LCD driver output 5
S4	33	LCD driver output 4
S3	34	LCD driver output 3
S2	35	LCD driver output 2
S1	36	LCD driver output 1
n.c.	37	not connected
BP	38	backplane driver output
DATA	39	date input line (CBUS)
DLEN	40	data input line enable (CBUS)

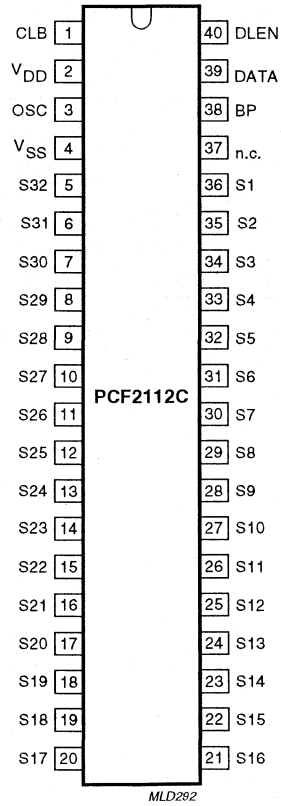


Fig.6 Pin configuration; SOT129-1 and SOT158-1.

FUNCTIONAL DESCRIPTION

An LCD segment or LED output is activated when the corresponding DATA bit is HIGH.

PCF2100C

When DATA bit 21 is HIGH, the A-latches (BP1) are loaded. With DATA bit 21 LOW, the B-latches (BP2) are loaded. CLB pulse 23 transfers data from the shift register to the selected latches.

PCF2111C

When DATA bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA bit 33 LOW, the B-latches (BP2) are loaded. CLB pulse 35 transfers data from the shift register to the selected latches.

PCF2112C

When DATA bit 33 is HIGH, the latches are loaded. CLB pulse 35 transfers data from the shift register to the selected latches.

Bus control logic

The following tests are carried out by the bus control logic:

1. Test on leading zero
2. Test on number of DATA bits
3. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN LOW) and the driver is ready to receive new data.

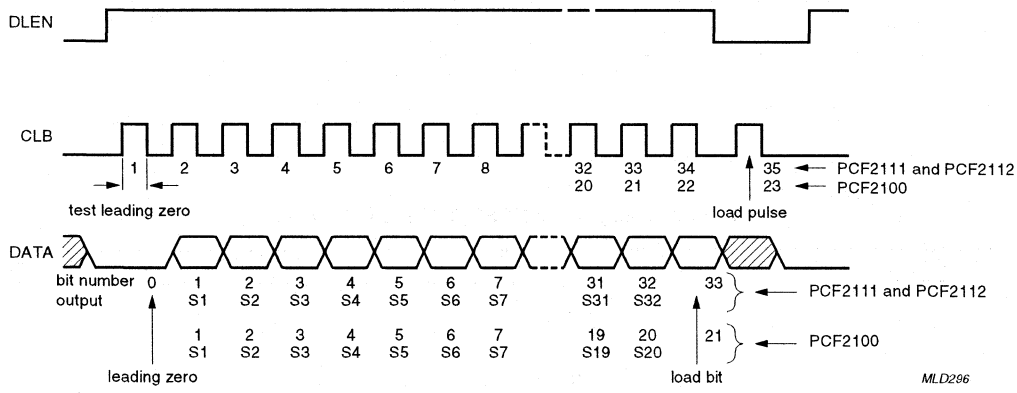


Fig.7 CBUS data format.

Timing

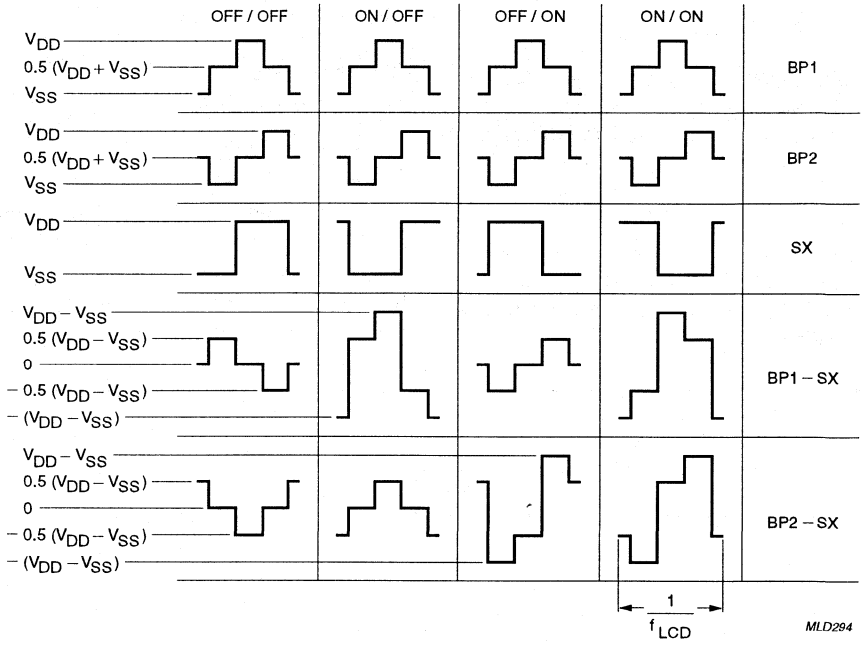


Fig.8 Timing diagram for PCF2100C and PCF2111C.

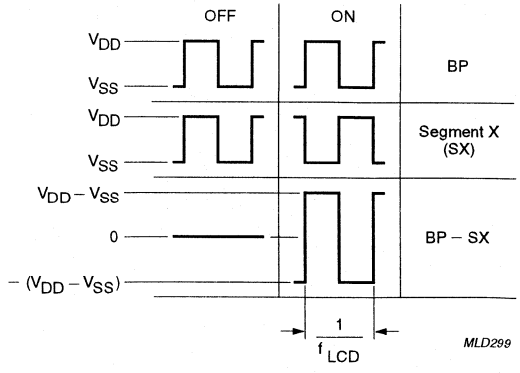
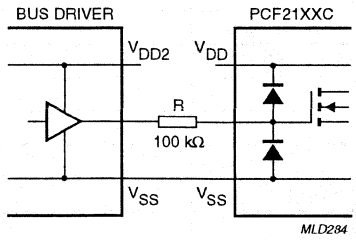


Fig.9 Timing diagram for PCF2112C.

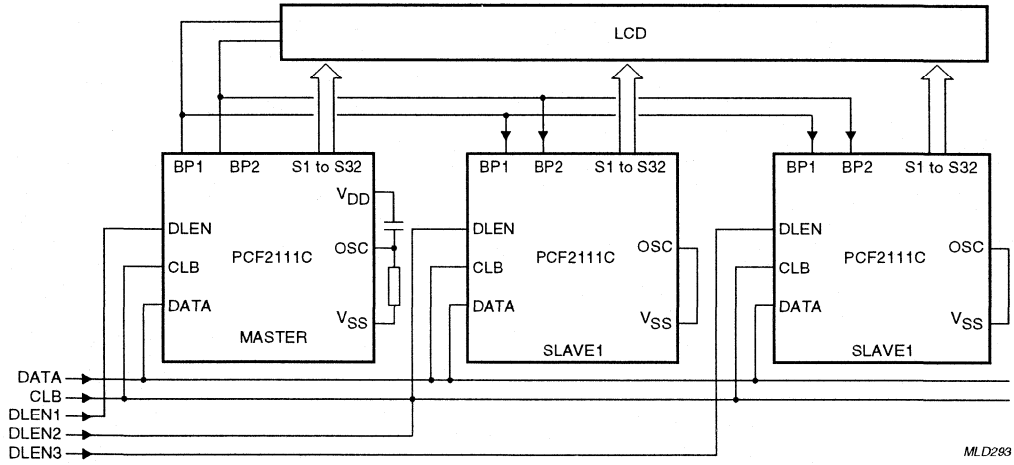
Input circuitry



V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0.5$ V, a resistor should be inserted to reduce the current flowing through the input protection. Maximum input current ≤40 μA.

Fig.10 Input circuitry.

Expansion



By connecting OSC to V_{SS} the BP pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several members of the PCF21XXC family up to the BP drive capability of the master. The PCF2112C can only function as a master for other PCF2112Cs.

Fig.11 Expansion possibility (using PCF2111C).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+8.0	V
V_I	input voltage DLEN, CLB, DATA and OSC		V_{SS} − 0.5	V_{DD} + 0.5	V
V_O	output voltage BP1, BP2 and S1 to S32		V_{SS} − 0.5	V_{DD} + 0.5	V
I_{DD}, I_{SS}	supply current		−50	+50	mA
I_I	DC input current		−20	+20	mA
I_O	DC output current		−25	+25	mA
P_{tot}	total power dissipation per package	note 1	−	500	mW
P_O	power dissipation per output		−	100	mW
T_{stg}	storage temperature		−65	+150	°C

Note

1. Derate by 7.7 mW/K when T_{amb} > 60 °C.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

ESD in accordance with *"MIL STD 883C, Method 3015"*.

DC CHARACTERISTICS

V_{DD} = 2.25 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +80 °C; R_O = 1 MΩ; C_O = 680 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.25	–	6.0	V
I_{DD}	supply current	note 1	–	20	50	µA
		note 1; T_{amb} = 25 °C	–	20	30	µA
V_{POR}	power-on reset voltage level	note 2	–	1.0	1.6	V
Inputs CLB, DATA and DLEN						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
I_{LI}	input leakage current	$V_I = V_{SS}$ or V_{DD}	–	–	±1	µA
C_I	input capacitance	note 3	–	–	10	pF
Input OSC						
I_{osc}	oscillator start-up current	$V_I = V_{SS}$	0.5	1.2	5.0	µA
LCD outputs						
V_{BP}	DC voltage of backplane drivers		–	±20	–	mV
$Z_{O(BP)}$	backplane driver output impedance	note 4; V_{DD} = 5 V	–	0.5	5.0	kΩ
$Z_{O(S)}$	segment driver output impedance	note 4; V_{DD} = 5 V	–	1	7	kΩ

Notes

1. Outputs open; CBUS inactive.
2. Resets all logic, when $V_{DD} < V_{POR}$.
3. Periodically sampled (not 100% tested).
4. Outputs measured one at a time.

AC CHARACTERISTICS

V_{DD} = 2.25 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +80 °C; R_O = 1 MΩ; C_O = 680 pF; all timing values are referenced to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs CLB, DATA and DLEN						
t_{SUDA}	data set-up time		3	–	–	µs
t_{HDDA}	data hold time		3	–	–	µs
t_{SUEN}	enable set-up time		1	–	–	µs
t_{SUDI}	disable set-up time		2	–	–	µs
t_{SULD}	load pulse set-up time		2.5	–	–	µs
t_{BUSY}	busy time		3	–	–	µs
t_{WH}	CLB HIGH time		1	–	–	µs
t_{WL}	CLB LOW time		5	–	–	µs
t_{CLB}	CLB cycle time		10	–	–	µs
t_r	rise time		–	–	10	µs
t_f	fall time		–	–	10	µs
LCD timing						
f_{LCD}	LCD frame frequency					
	PCF2100C, PCF2111C		60	75	100	Hz
	PCF2112C	C_O = 1.5 nF	30	35	50	Hz
t_{BS}	transfer time with test loads	V_{DD} = 5 V	–	20	100	µs
t_{PLCD}	driver delay time with test loads	V_{DD} = 5 V	–	20	100	µs

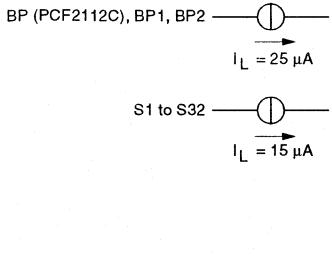


Fig.12 Test loads.

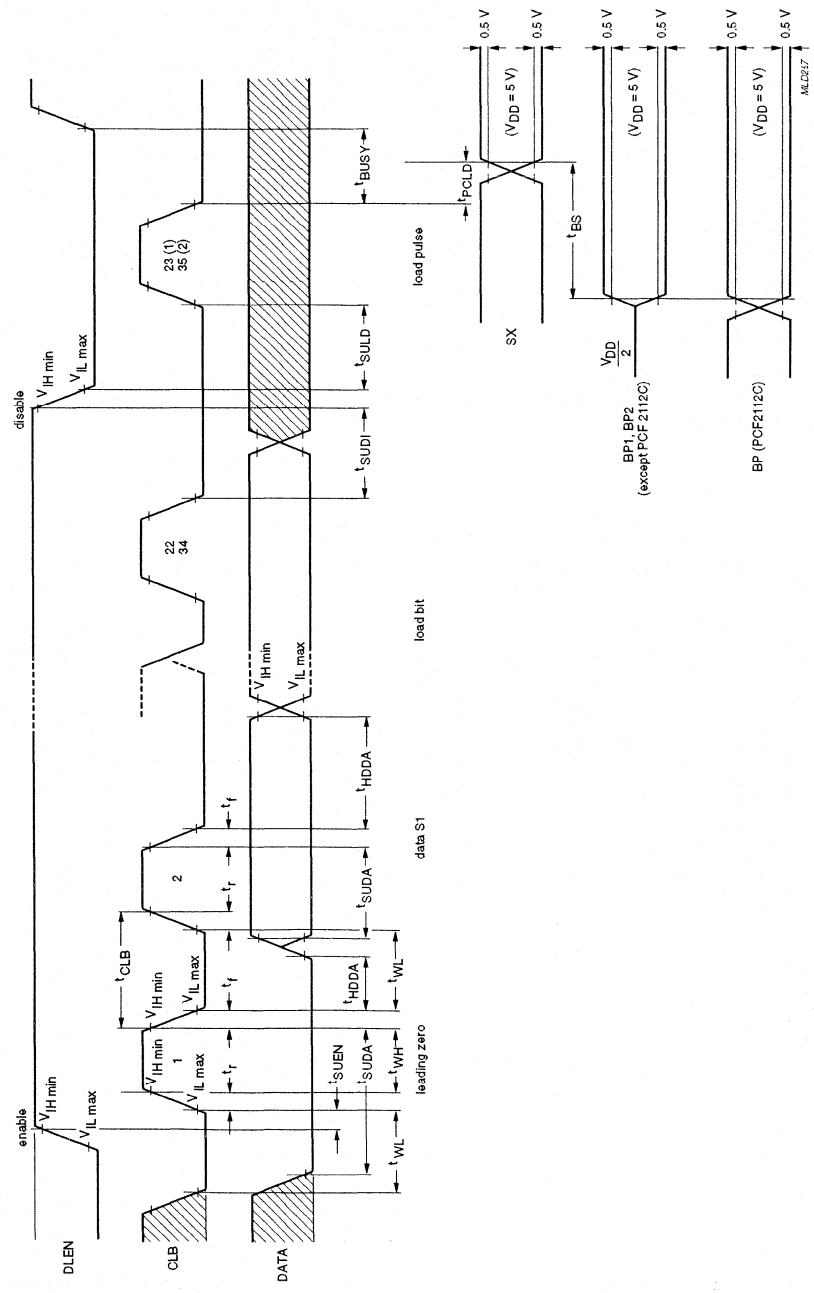
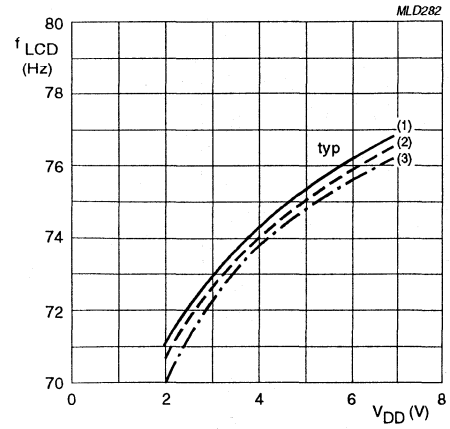


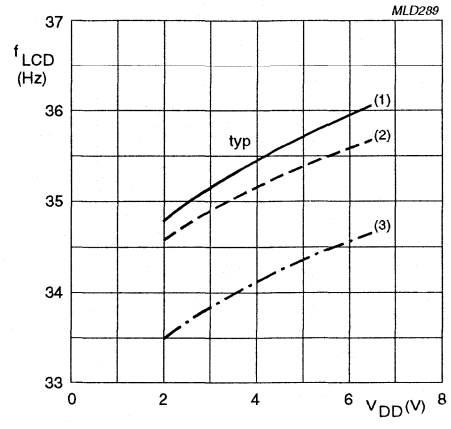
Fig.13 CBUS timing.

(1) Load pulse 23 for PCF2100C.
(2) Load pulse 35 for PCF2111C and PCF2112C (see Fig.7).



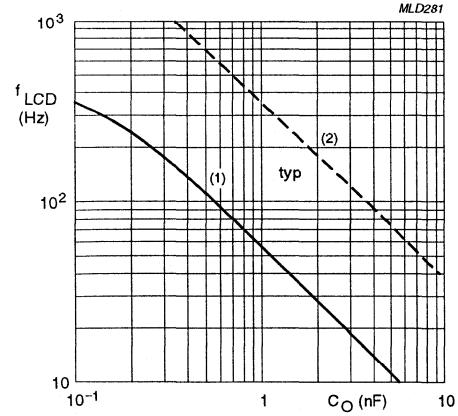
(1) $T_{amb} = -40$ °C.
(2) $T_{amb} = +25$ °C.
(3) $T_{amb} = +85$ °C.

Fig.14 Display frequency as a function of supply voltage; C_O = 680 pF (except PCF2112C).



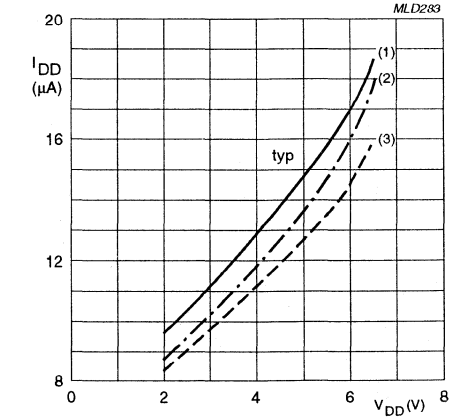
(1) $T_{amb} = -40$ °C.
(2) $T_{amb} = +25$ °C.
(3) $T_{amb} = +85$ °C.

Fig.15 Display frequency as a function of supply voltage; C_O = 1.5 nF (only PCF2112C).



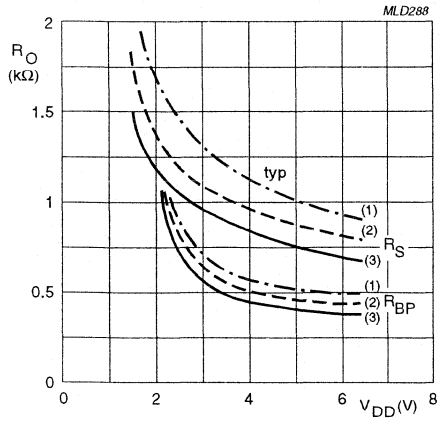
(1) $R_O = 1$ MΩ.
(2) $R_O = 100$ kΩ.

Fig.16 Display frequency as a function of R_O and C_O; T_{amb} = 25 °C; V_{DD} = 5 V.



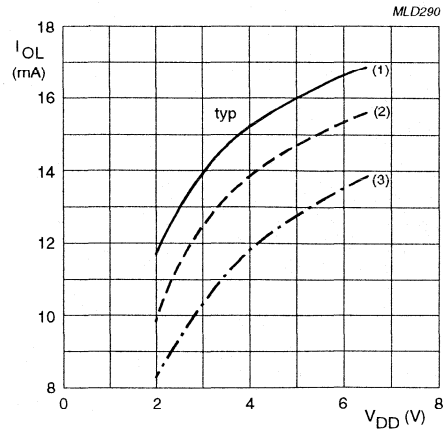
(1) $T_{amb} = -40$ °C.
(2) $T_{amb} = +85$ °C.
(3) $T_{amb} = +25$ °C.

Fig.17 Supply current as a function of supply voltage.



(1) T_{amb} = +85 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = −40 °C.

Fig.18 Output resistance of backplane and segments.



(1) T_{amb} = −40 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = +85 °C.

Fig.19 LOW level output current as a function of supply voltage (only PCF2112C).

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2,5 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40-lead plastic mini-pack (VSO-40; SOT-158A)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8566P: 40-lead DIL; plastic (SOT129).
PCF8566T: 40-lead mini-pack (VSO40; SOT158A).

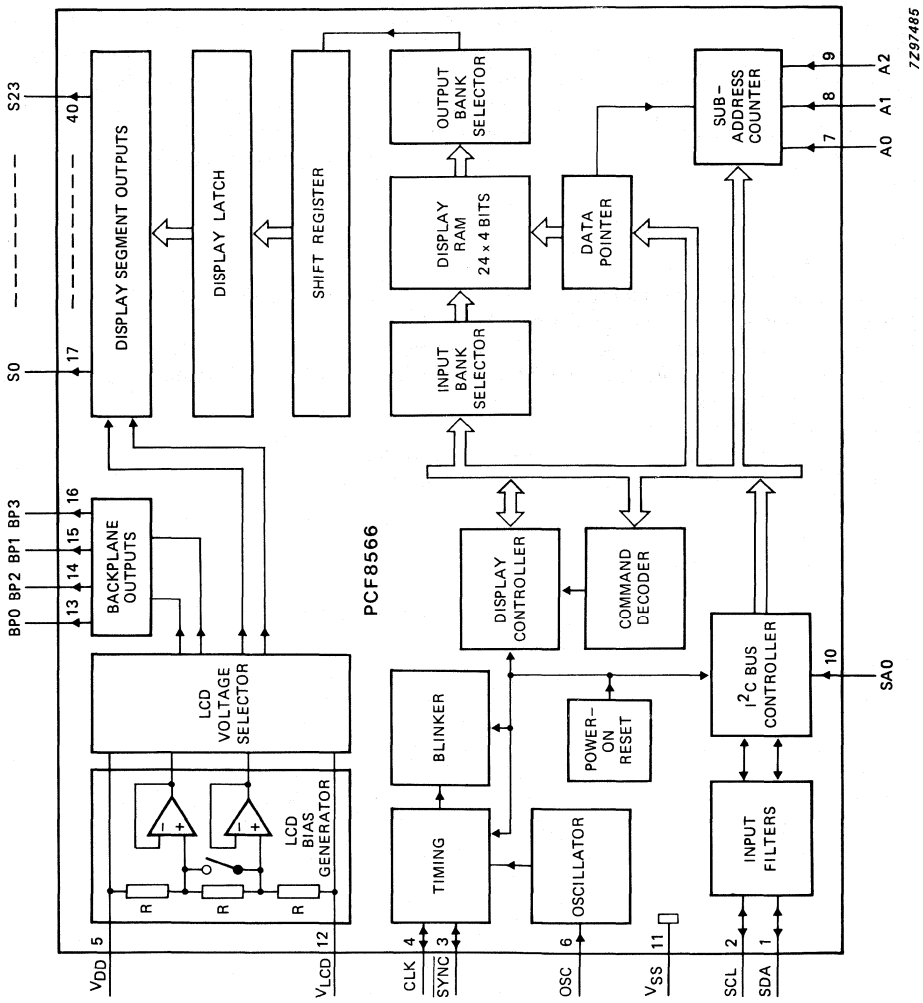


Fig. 1 Block diagram.

DEVELOPMENT DATA

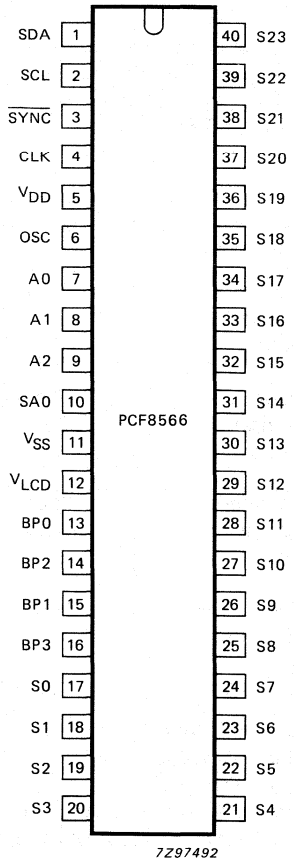


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{SYNC}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	
9	A2	
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17	S0	LCD segment outputs
to	to	
40	S23	

FUNCTIONAL DESCRIPTION

The PCF8566 is a versatile peripheral device designed to interface any microprocessor to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 24 segments. The display configurations possible with the PCF8566 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active back-plane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	96	12 digits + 12 indicator symbols	6 characters + 12 indicator symbols	96 dots (4 x 24)
3	72	9 digits + 9 indicator symbols	4 characters + 16 indicator symbols	72 dots (3 x 24)
2	48	6 digits + 6 indicator symbols	3 characters + 6 indicator symbols	48 dots (2 x 24)
1	24	3 digits + 3 indicator symbols	1 characters + 10 indicator symbols	24 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig. 3. The host microprocessor/microcontroller maintains the two-line I^2C bus communication channel with the PCF8566. The internal oscillator is selected by tying OSC (pin 6) to V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

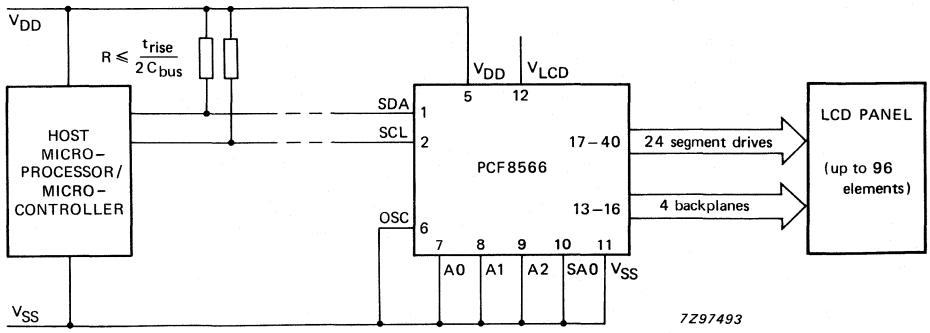


Fig. 3 Typical system configuration.

Power-on reset

At power-on the PCF8566 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0{,}354$	$\sqrt{10}/4 = 0{,}791$	$\sqrt{5} = 2{,}236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{5}/3 = 0{,}745$	$\sqrt{5} = 2{,}236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{33}/9 = 0{,}638$	$\sqrt{33}/3 = 1{,}915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{3}/3 = 0{,}577$	$\sqrt{3} = 1{,}732$

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\ V_{th}$.
Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1{,}732$ for 1 : 3 multiplex or $\sqrt{21}/3 = 1{,}528$ for 1 : 4 multiplex).
The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\ V_{off(rms)} = 2{,}449\ V_{off(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\ V_{off(rms)} = 2{,}309\ V_{off(rms)}$

These compare with $V_{op} = 3\ V_{off(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig. 4.

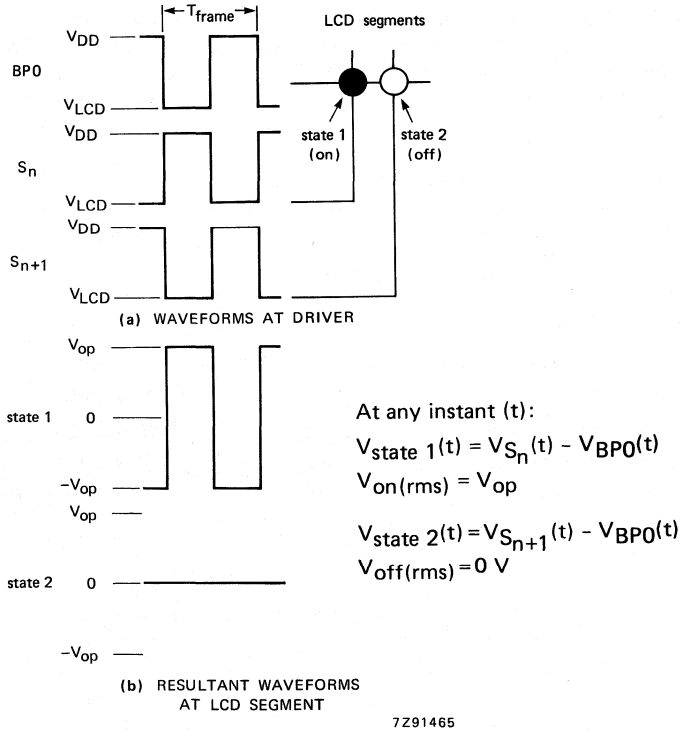


Fig. 4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8566 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

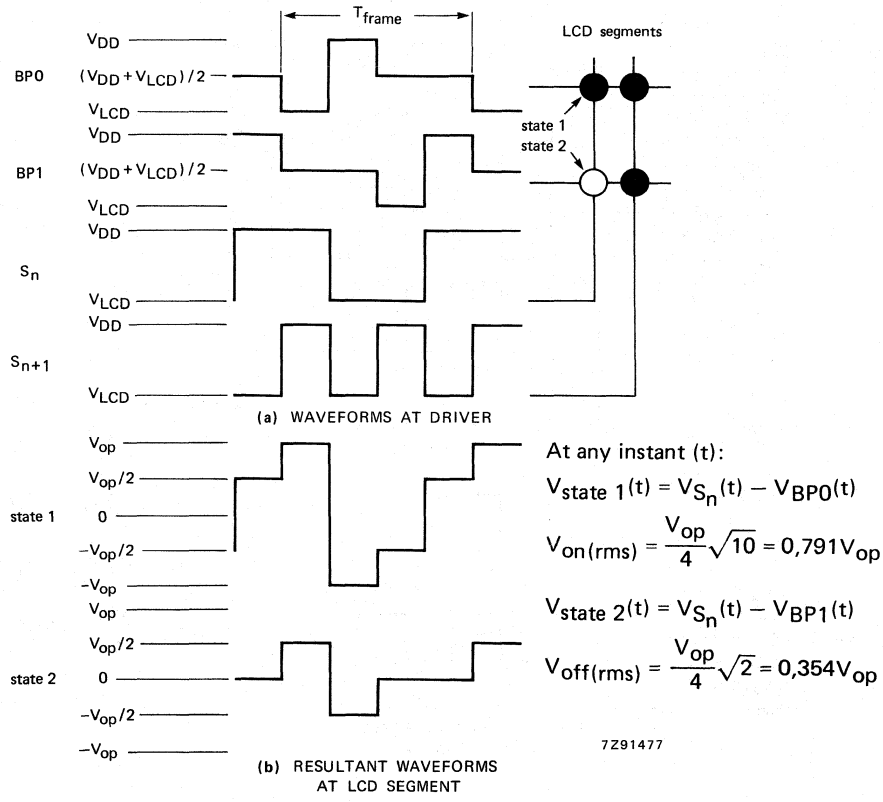


Fig. 5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

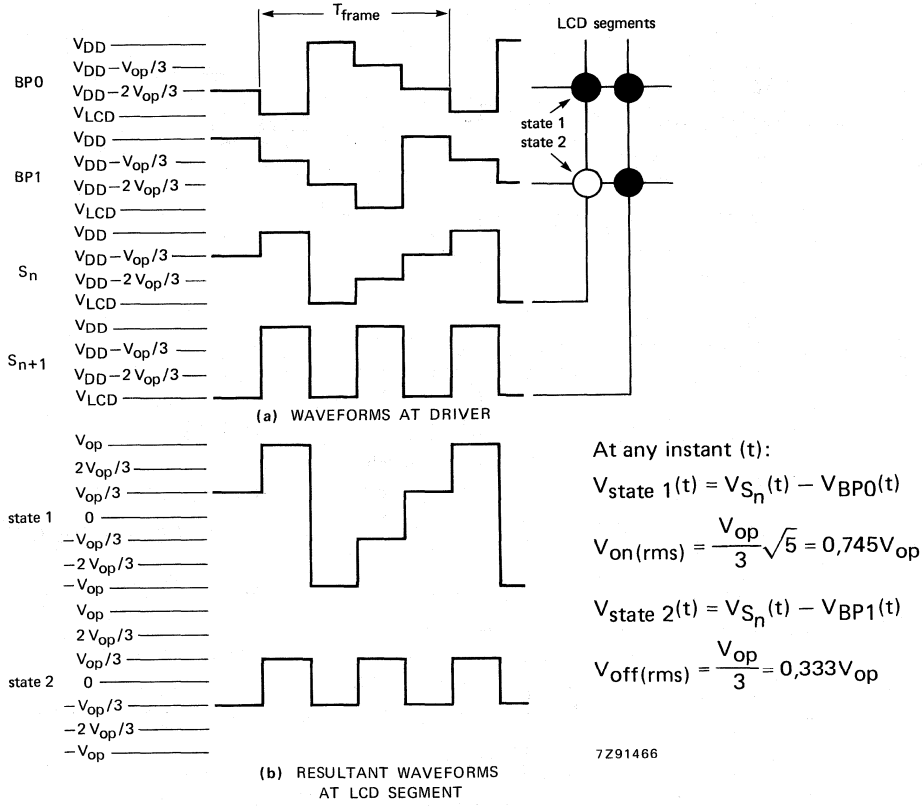


Fig. 6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive wavefront for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

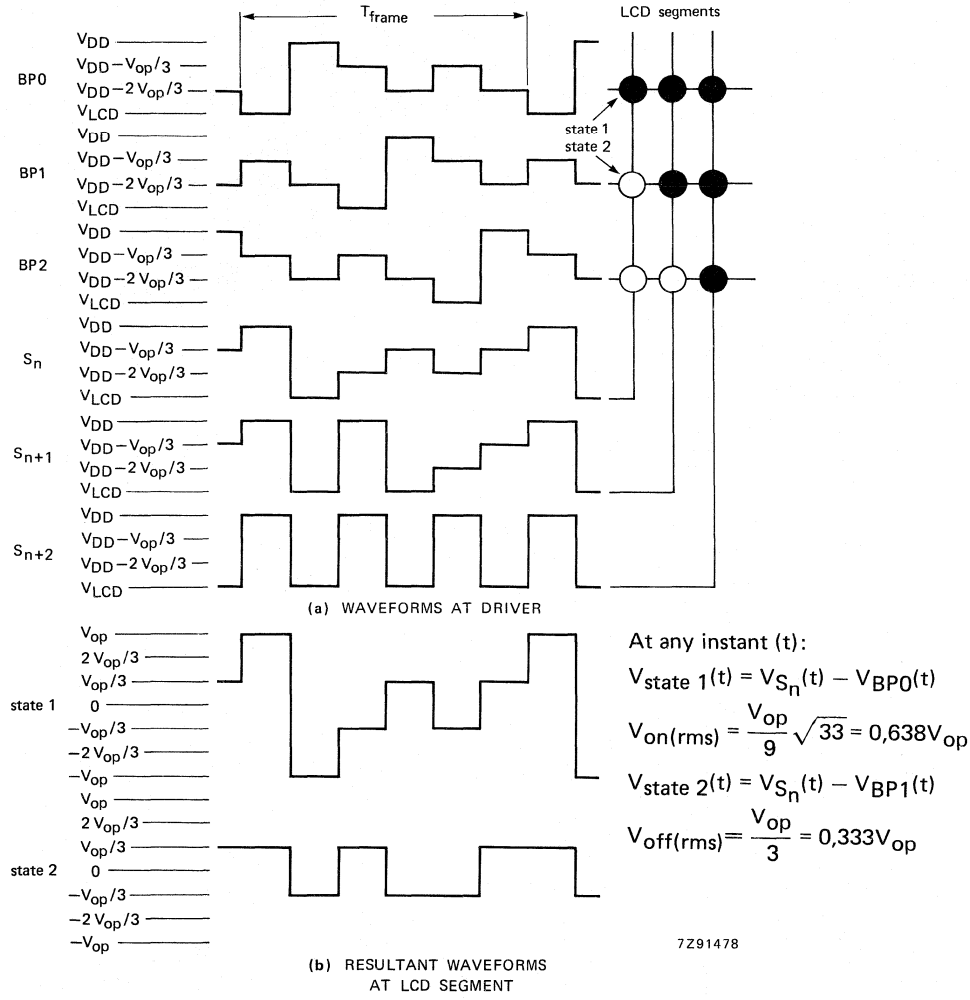


Fig. 7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

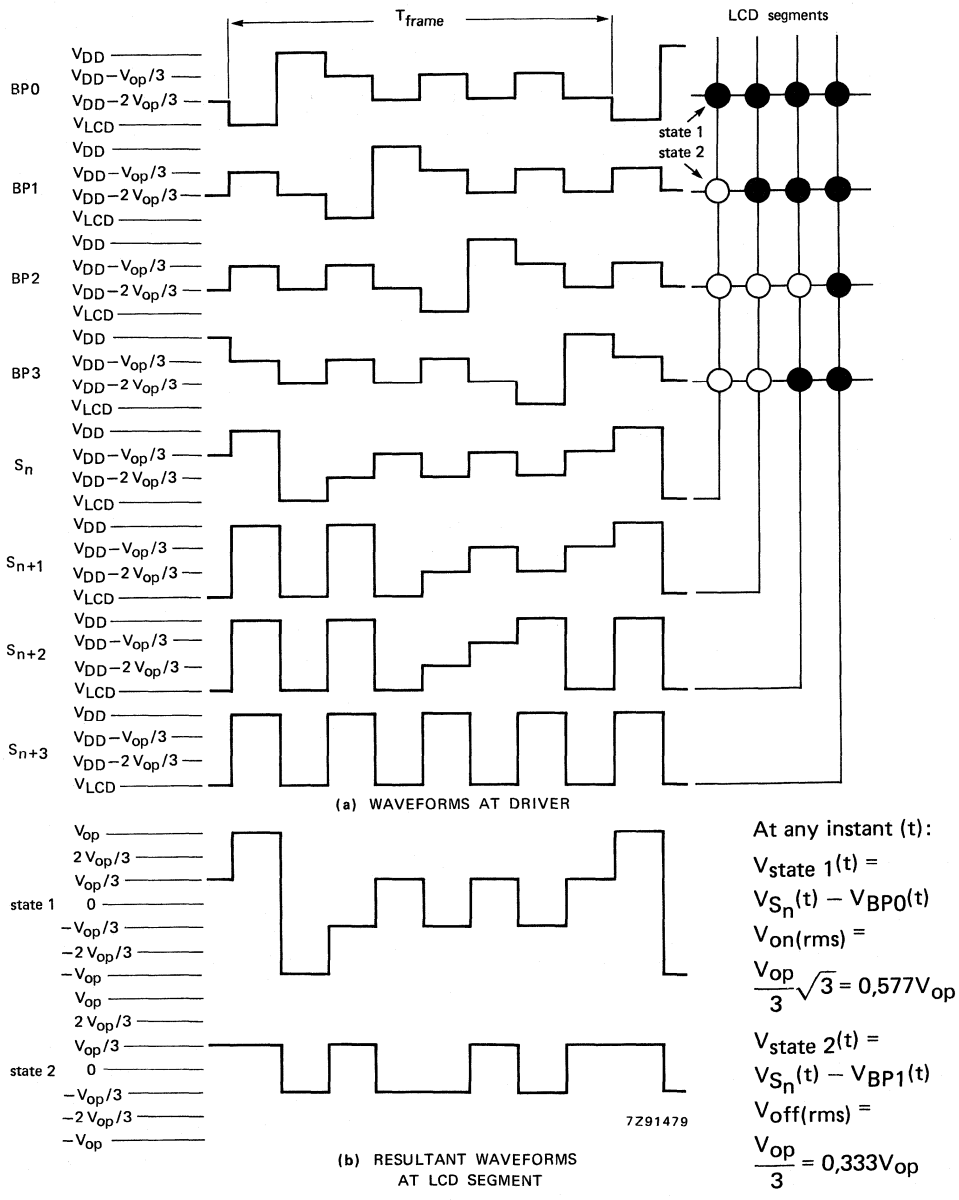


Fig. 8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

The internal logic and the LCD drive signals of the PCF8566 or PCF8576 are timed either by the built-in oscillator or from an external clock.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I^2C bus. To allow I^2C bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

Internal clock

When the internal oscillator is used, OSC (pin 6) should be tied to V_{SS}. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8566s and PCF8576s in the system.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

Timing

The timing of the PCF8566 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8566s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by MODE SET commands when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8566 mode	f_{frame}	nominal f_{frame} (Hz)
normal mode	$f_{CLK}/2880$	64
power-saving mode	$f_{CLK}/480$	64

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line low until the first display data byte is stored. This slows down the transmission rate of the I^2C bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 24 segment outputs S0 to S23 (pins 17 to 40) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 24 segment outputs are required the unused segment outputs should be left open-circuit.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 24 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 24 segments operated with respect to backplane BP0 (Fig. 9). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

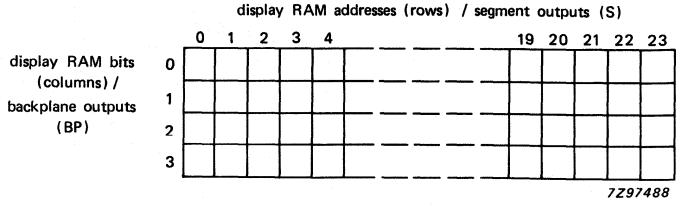


Fig. 9 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8566 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig. 10; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig. 10, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig. 10. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). A0, A1 and A2 should be tied to V_{SS} or V_{DD}. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8566 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

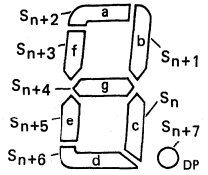
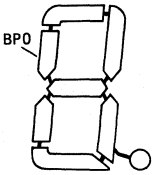
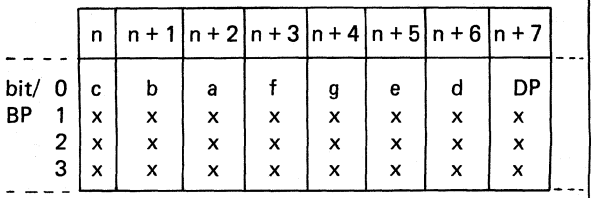
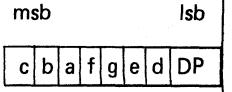
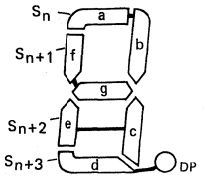
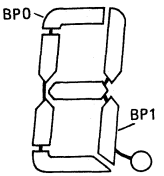
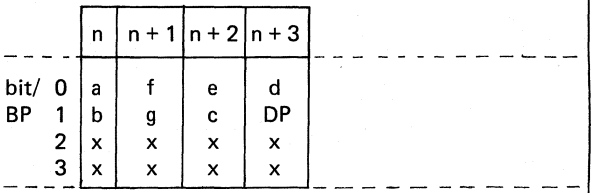
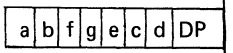
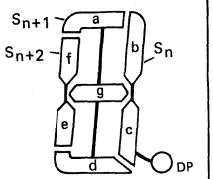
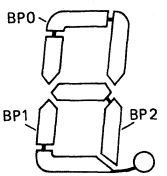
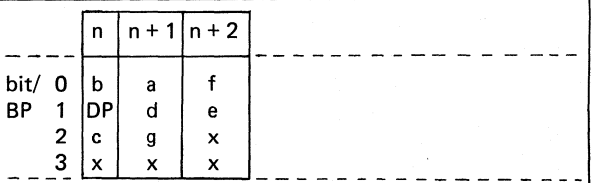
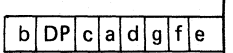
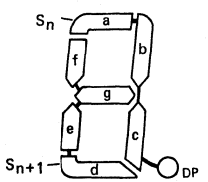
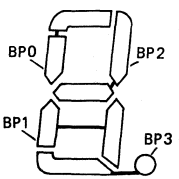
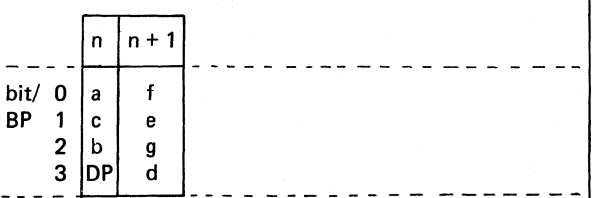
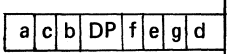
drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte
static				
1 : 2 multiplex				
1 : 3 multiplex				
1 : 4 multiplex				

Fig. 10 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

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Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8566 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8566 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0,5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0,5

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

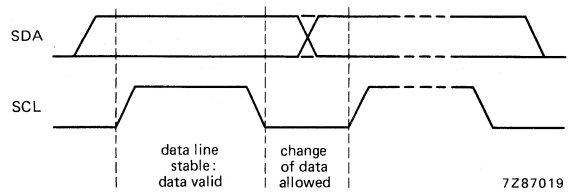


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

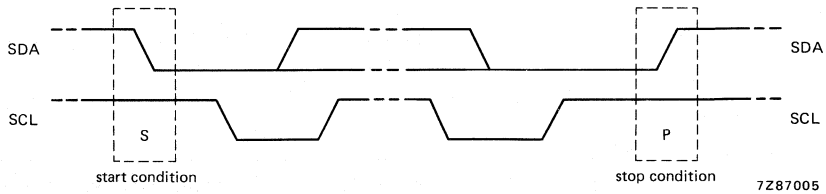


Fig. 12 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

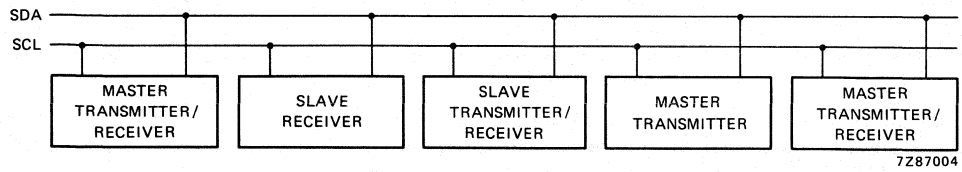


Fig. 13 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

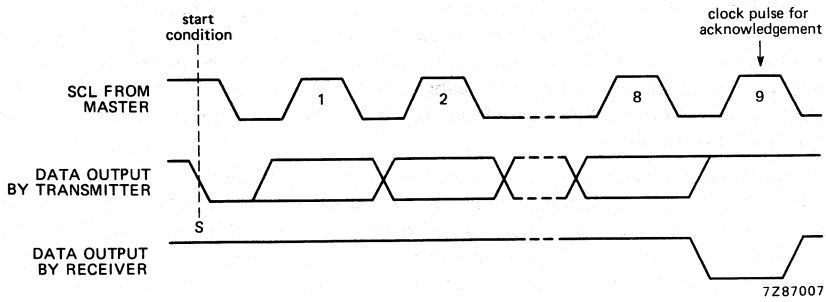


Fig. 14 Acknowledgement on the I^2C bus.

PCF8566 I²C bus controller

The PCF8566 acts as an I²C slave receiver. It does not initiate I²C bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8566 are the acknowledge signals of the selected devices. Device selection depends on the I²C bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally left open-circuit or tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are left open-circuit or tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8566 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8566 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C bus protocol

Two I²C bus slave addresses (0111110 and 0111111) are reserved for PCF8566. The least-significant bit of the slave address that a PCF8566 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8566 can be distinguished on the same I²C bus which allows:

(a) up to 16 PCF8566s on the same I²C bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C bus.

The I²C bus protocol is shown in Fig. 15. The sequence is initiated with a start condition (S) from the I²C bus master which is followed by one of the two PCF8566 slave addresses available. All PCF8566s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8566s with the alternative SA0 level ignore the whole I²C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8566s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8566s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8566 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8566. After the last display byte, the I²C bus master issues a stop condition (P).

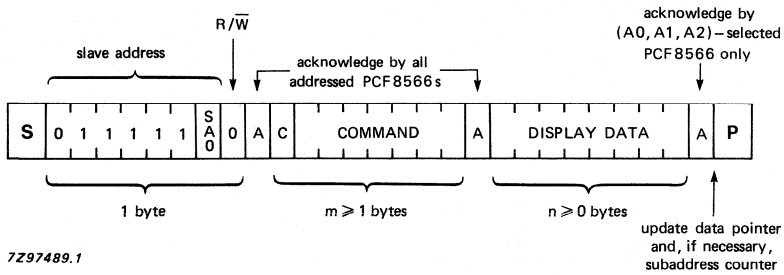


Fig. 15 I^2C bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I^2C bus. All available commands carry a continuation bit C in their most-significant bit position (Fig. 16). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

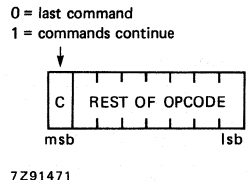


Fig. 16 General format of command byte.

The five commands available to the PCF8566 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8566 commands

<table>
<tr><th>command/opcode</th><th>options</th><th>description</th></tr>
<tr><td>MODE SET

C | 1 | 0 | LP | E | B | M1 | M0</td><td>LCD drive mode | bits M1 M0
static (1 BP) | 0 1
1 : 2 MUX (2 BP) | 1 0
1 : 3 MUX (3 BP) | 1 1
1 : 4 MUX (4 BP) | 0 0

LCD bias | bit B
1/3 bias | 0
1/2 bias | 1

display status | bit E
disabled (blank) | 0
enabled | 1

mode | bit LP
normal mode | 0
power-saving mode | 1</td><td>Defines LCD drive mode

Defines LCD bias configuration

Defines display status
The possibility to disable the display allows implementation of blinking under external control

Defines power dissipation mode</td></tr>
<tr><td>LOAD DATA POINTER

C | 0 | 0 | P4 P3 P2 P1 P0</td><td>bits P4 P3 P2 P1 P0
5-bit binary value of 0 to 23</td><td>Five bits of immediate data, bits P4 to P0, are transferred to the data pointer to define one of twenty-four display RAM addresses</td></tr>
<tr><td>DEVICE SELECT

C | 1 1 0 0 | A2 A1 A0</td><td>bits A0 A1 A2
3-bit binary value of 0 to 7</td><td>Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses</td></tr>
</table>

<table>
<tr><th>command/opcode</th><th>options</th><th>description</th></tr>
<tr><td>BANK SELECT

C 1 1 1 1 0 I O</td><td>
<table>
<tr><td>static</td><td>1 : 2 MUX</td><td>bit I</td></tr>
<tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr>
</table>
<table>
<tr><td>static</td><td>1 : 2 MUX</td><td>bit O</td></tr>
<tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr>
</table>
</td><td>Defines input bank selection (storage of arriving display data)

Defines output bank selection (retrieval of LCD display data)

The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
<tr><td>BLINK

C 1 1 1 0 A BF1 BF0</td><td>
<table>
<tr><td>blink frequency</td><td>bits BF1</td><td>BF0</td></tr>
<tr><td>off</td><td>0</td><td>0</td></tr>
<tr><td>2 Hz</td><td>0</td><td>1</td></tr>
<tr><td>1 Hz</td><td>1</td><td>0</td></tr>
<tr><td>0,5 Hz</td><td>1</td><td>1</td></tr>
</table>
<table>
<tr><td>blink mode</td><td>bit A</td></tr>
<tr><td>normal blinking
alternation blinking</td><td>0
1</td></tr>
</table>
</td><td>Defines the blinking frequency

Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
</table>

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8566 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8566s can be distinguished on the same I²C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I²C slave address (SA0). It is also possible to cascade up to 16 PCF8566s. When cascaded, several PCF8566s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8566s of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (Fig. 17).

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF8566s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8566s with differing SA0 levels are cascaded). $\overline{SYNC}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8566 asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8566 to assert $\overline{SYNC}$. The timing relationships between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF8576 are shown in Fig. 18. The waveforms are identical with the parent device PCF8576. Casadability between PCF8566s and PCF8576s is possible, giving cost effective LCD applications.

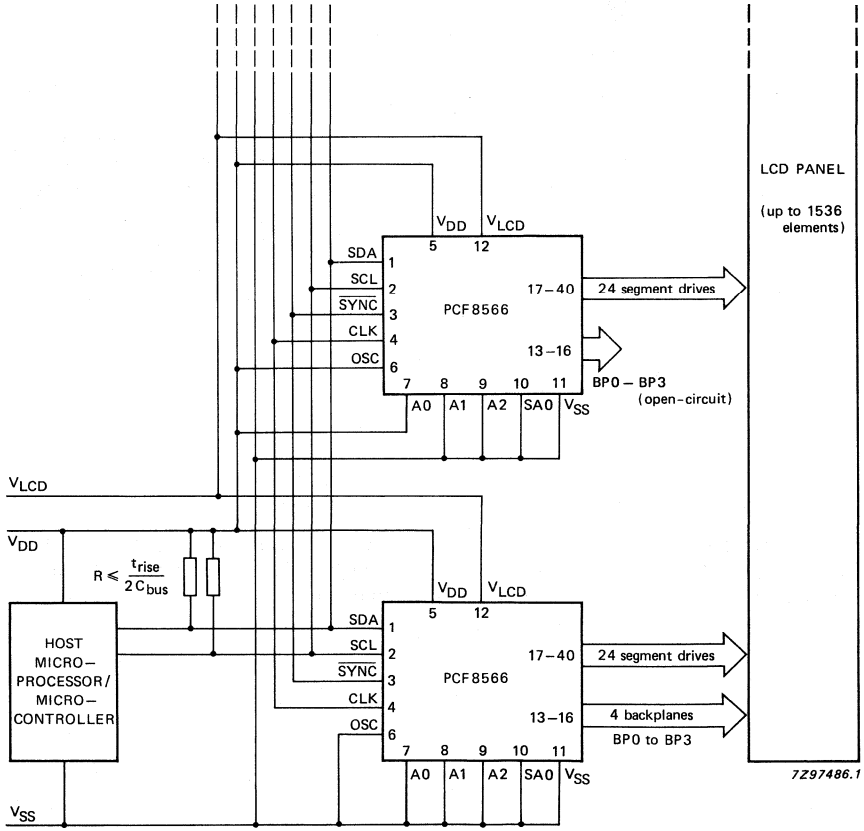


Fig. 17 Cascaded PCF8566 configuration.

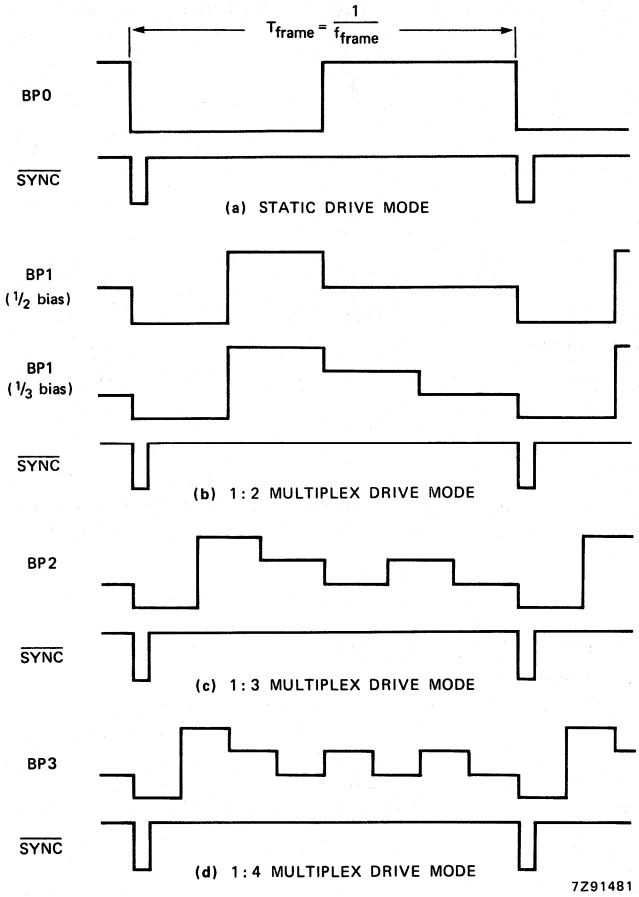


Fig. 18 Synchronization of the cascade for the various PCF8566 drive modes.

For single plane wiring of PCF8566s, see section "APPLICATION INFORMATION".

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range; see note	V_{DD}		−0,5 to + 7 V
LCD supply voltage range	V_{LCD}		V_{DD} −7 to V_{DD} V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I		V_{SS} −0,5 to V_{DD} + 0,5 V
Output voltage range (S0 to S23; BP0 to BP3)	V_O		V_{LCD} −0,5 to V_{DD} + 0,5 V
DC input current	$\pm I_I$	max.	20 mA
DC output current	$\pm I_O$	max.	25 mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	400 mW
Power dissipation per output	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C

Note

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2,5 to 6 V; V_{LCD} = V_{DD} −2,5 to V_{DD} −6 V;

T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6	V
LCD supply voltage	V_{LCD}	V_{DD} −6	–	V_{DD} −2,5	V
Operating supply current (normal mode) at f_{CLK} = 200 kHz (note 1)	I_{DD}	–	30	90	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz; A0, A1 and A2 tied to V_{SS} (note 1)	I_{LP}	–	15	40	μA

parameter	symbol	min.	typ.	max.	unit
Logic					
Input voltage LOW	V_{IL}	V_{SS}	–	0,3 V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD} –0,05	–	–	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	–	–	–1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current (SA0, CLK, OSC, A0, A1, A2, SCL, SDA) at $V_I = V_{SS}$ or V_{DD}	$\pm I_L$	–	–	1	μA
Pull-down current (A0; A1; A2; OSC) at V_I = 1 V and V_{DD} = 5 V	I_{pd}	15	50	150	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	15	25	60	kΩ
Power-on reset level (note 2)	V_{REF}	–	1,3	2,0	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 3)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S23) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD}$ –5 V (note 4)	R_{BP}	–	1	5	kΩ
Output impedance (S0 to S23) at $V_{LCD} = V_{DD}$ –5 V (note 4)	R_S	–	3	7,0	kΩ

AC CHARACTERISTICS (note 5)

V_{SS} = 0 V; V_{DD} = 2,5 to 6 V; V_{LCD} = V_{DD} −2,5 to V_{DD} −6 V;

T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) at V_{DD} = 5 V (note 6)	f_{CLK}	125	200	315	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay	t_{PSYNC}	–	–	400	ns
$\overline{SYNC}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at V_{LCD} = V_{DD} −5 V	t_{PLCD}	–	–	30	μs
I²C bus					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_r	–	–	1	μs
Fall time	t_f	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs

Notes to characteristics

1. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I²C bus inactive.
2. Resets all logic when $V_{DD} < V_{REF}$.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
6. At $f_{CLK} < 125$ kHz, I²C bus maximum transmission speed is derated.

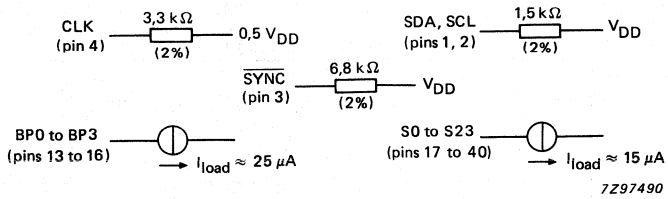


Fig. 19 Test loads.

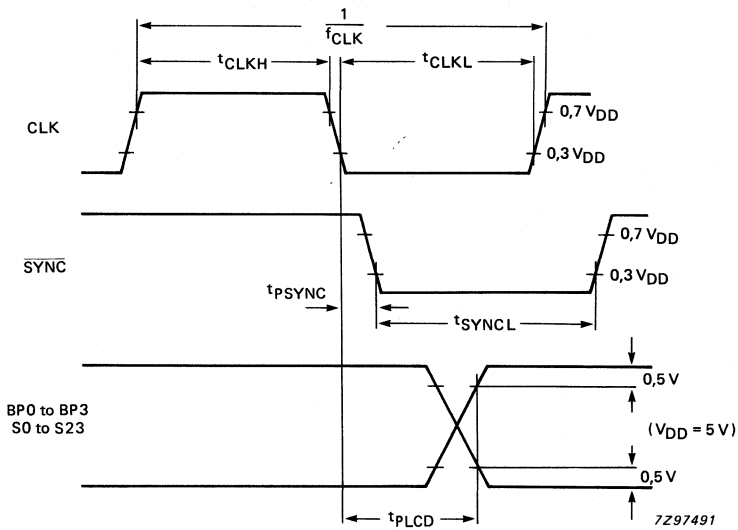


Fig. 20 Driver timing waveforms.

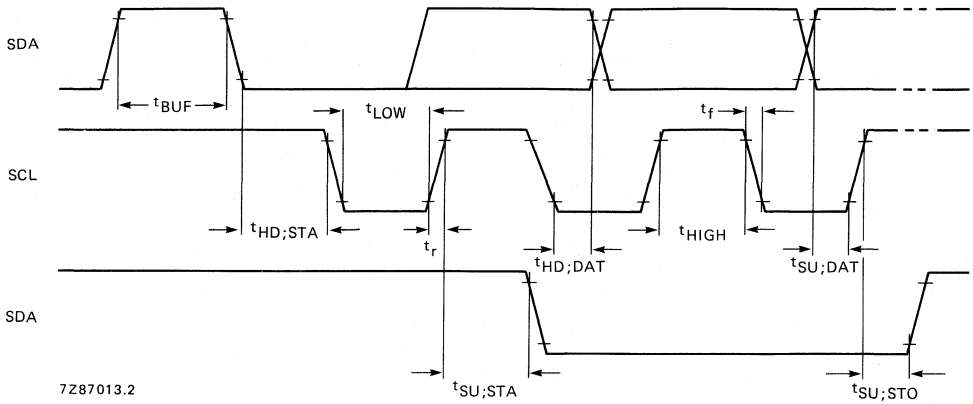
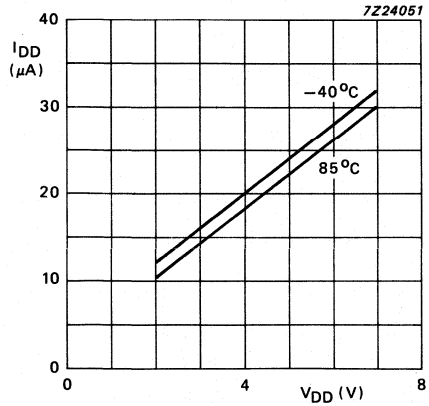
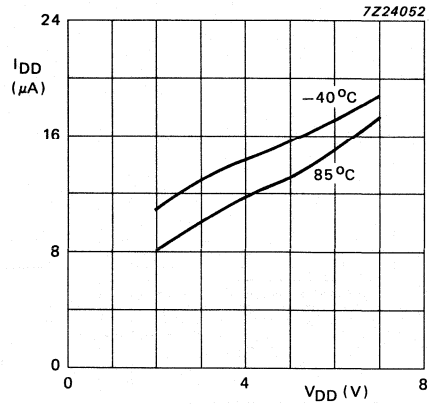


Fig. 21 I²C bus timing waveforms.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

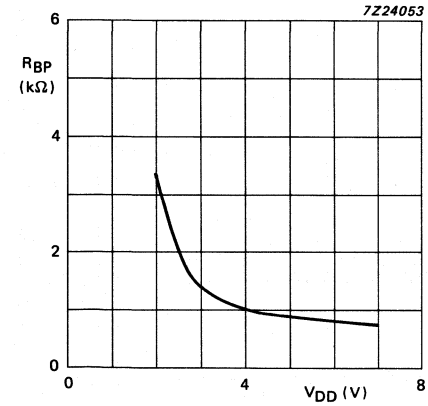


(a) Normal mode; V_{LCD} = 0 V; external clock = 200 kHz.

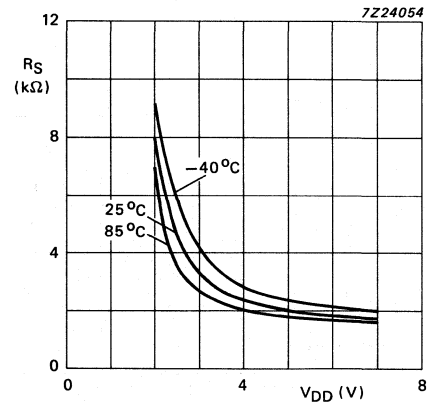


(b) Low power mode; V_{LCD} = 0 V; external clock = 35 kHz.

Fig. 22 Typical supply current characteristics.



(a) Backplane output impedance BP0 to BP3 (R_{BP}); V_{DD} = 5 V; T_{amb} = −40 to + 85 °C.



(b) Segment output impedance S0 to S23 (R_S); V_{DD} = 5 V.

Fig. 23 Typical characteristics of LCD outputs.

APPLICATION INFORMATION

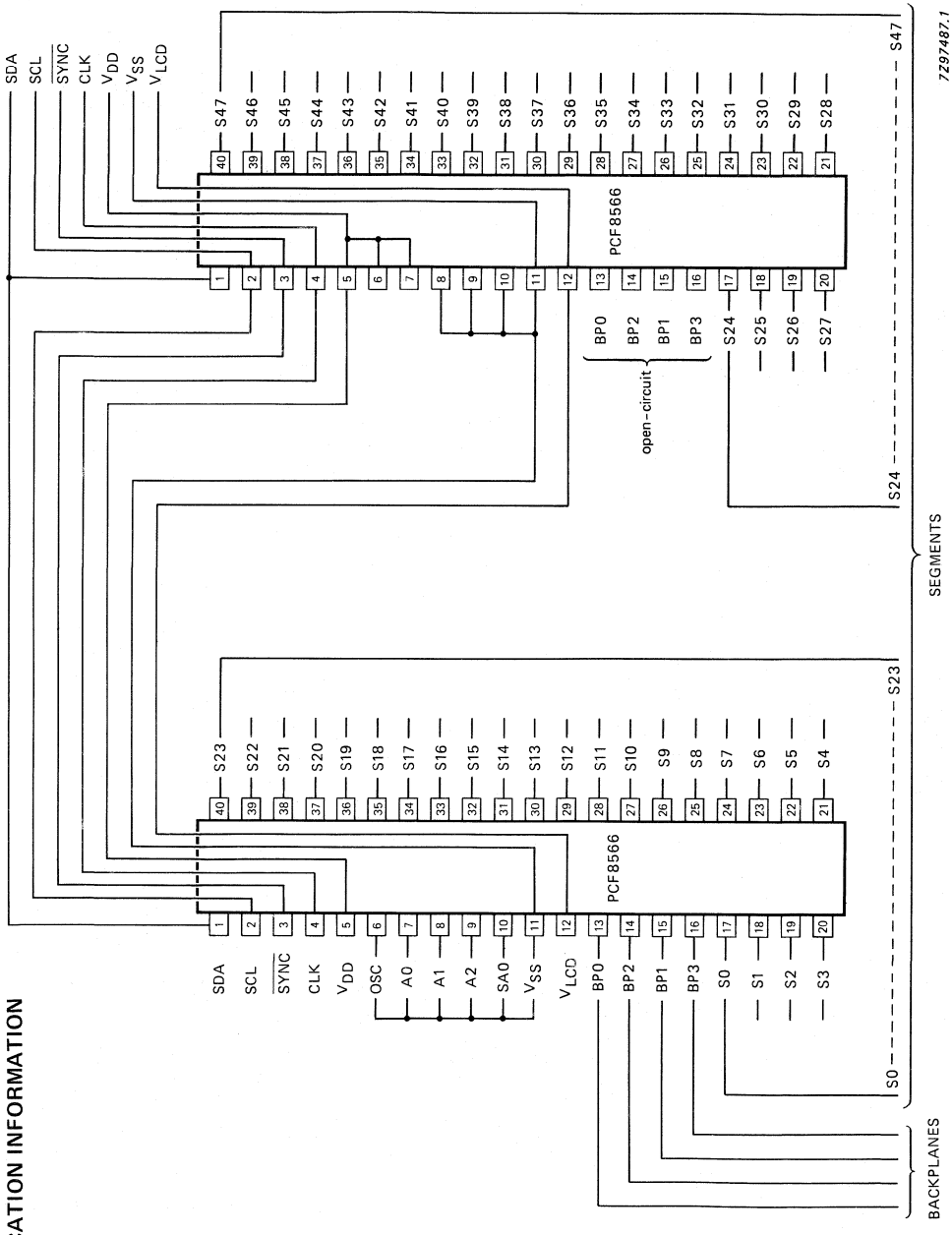


Fig. 24 Single plane wiring of packaged PCF8566s.

LCD row driver for dot matrix displays

PCF8568

FEATURES

- Single chip LCD row driver with 16 outputs
- Low power consumption
- Selectable multiplex rate 1:8, 1:16, 1:24, 1:32
- Cascadable to 1:24 or 1:32 multiplex rates
- Internally generated intermediate LCD bias voltages
- LCD column bias voltages available at pins VO3 and VO4
- Minimizes display system power requirements
- On-chip oscillator, requires only one external resistor
- Power-on reset blanks display
- Logic voltage range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9.0 V
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring
- Available in 28-lead plastic DIL or space saving mini-pack
- Compatible with chip-on-glass technology.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- General instrumentation
- Consumer products.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range	+2.5	-	+6.0	V
V_{LCD}	LCD supply voltage range voltage	V_{DD} –9	-	V_{DD} –3.5	V
I_{DD2}	supply current with internal clock (R_{OSC} = 330 kΩ)	-	67	150	µA
T_{amb}	operating ambient temperature range	–40	-	+85	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8568P	28	DIL	plastic	SOT117
PCF8568T	28	SO28	plastic	SOT136A
PCF8568U/7	(28 pads)	die: bumped chip on tape	-	-

GENERAL DESCRIPTION

The PCF8568 is a low power LCD row driver, designed to drive dot matrix graphic displays with multiplex rates of 1:8 or 1:16. The device has 16 row outputs. Two devices may be cascaded to drive displays with multiplex rates of 1:24 or 1:32. The PCF8568 is optimised for use with the PCF8569 and PCF8579 LCD dot matrix column drivers. Intermediate LCD bias voltages are internally generated. LCD column bias voltages are available at pins VO3 and VO4 for connection to the column drivers. The PCF8568 is compatible with most microcontrollers and communicates via a two- line bidirectional bus (I²C).

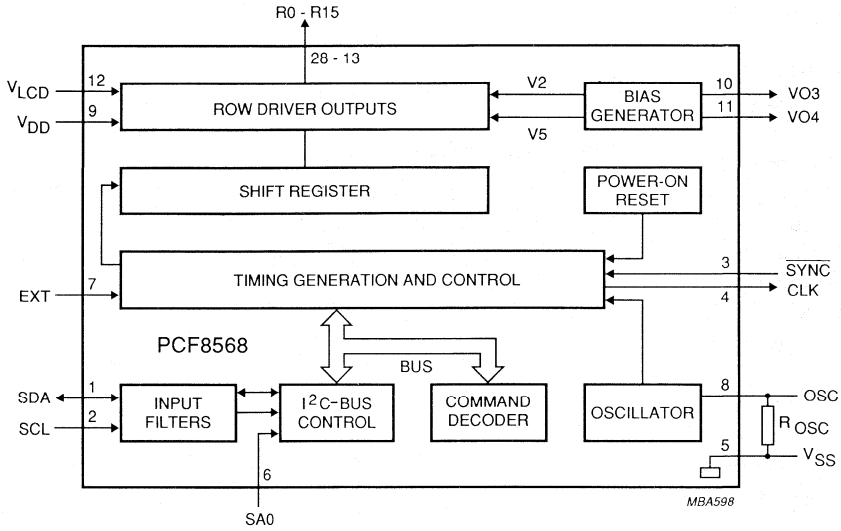


Fig.1 Block diagram.

LCD row driver for dot matrix displays

PCF8568

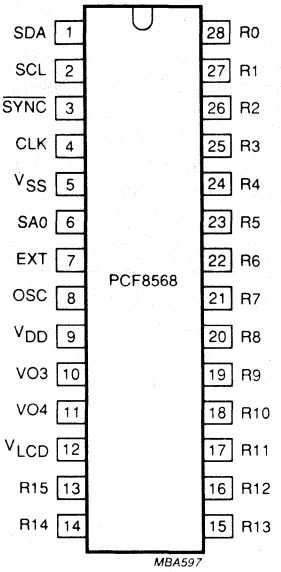


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus serial data line
SCL	2	I²C-bus serial clock line
$\overline{SYNC}$	3	cascade synchronization input/output
CLK	4	clock output
V_{SS}	5	ground (logic)
SA0	6	I²C-bus slave address input (bit 0)
EXT	7	external clock select pin
OSC	8	oscillator or external clock input pin
V_{DD}	9	positive supply voltage
VO3	10	LCD bias voltage output (V3)
VO4	11	LCD bias voltage output (V4)
V_{LCD}	12	LCD supply voltage
R15 to R0	13 to 28	LCD row driver outputs

FUNCTIONAL DESCRIPTION

A single PCF8568 functions as a row driver with up to 16 row outputs and provides the clock and synchronization signals for the PCF8569 and PCF8579 column drivers.

System types and cascaded operation

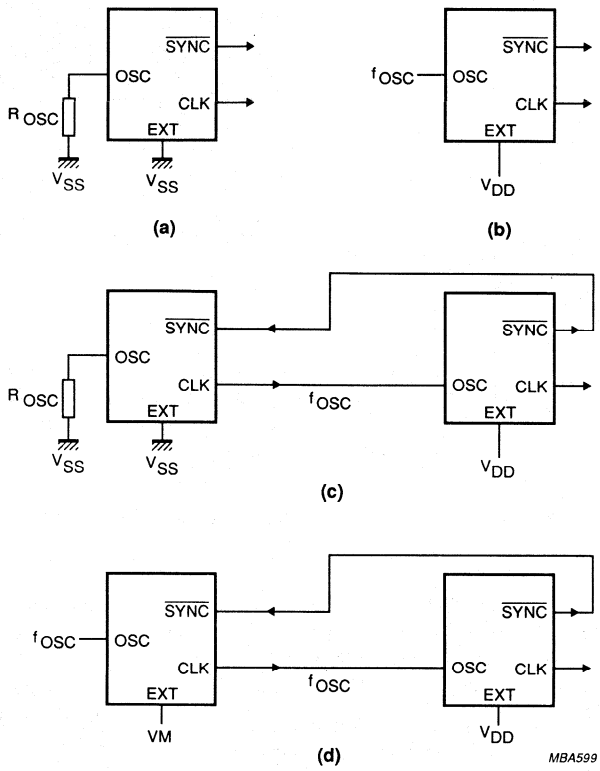
The PCF8568 may be configured in one of four different system types as shown in Fig. 3. The device operating mode is defined by the EXT and multiplex rate. EXT is programmed to one of three states by application of a DC level V_{DD}, V_M or V_{SS} to pin 7 (see DC characteristics).

A single PCF8568 may be used to drive up to 16 rows with a 1:8 or 1:16 multiplex rate. Two PCF8568s may be cascaded in order to drive up to 32 rows with a multiplex rate of 1:24 or 1:32. The device driving the last 16 rows provides the synchronization signal for the first device and the column drivers. LCD column bias voltages are available for connection from both devices at pins VO3 and VO4. Pins VO3 and VO4 from the first device must NOT be connected to pins VO3 and VO4 of the second device.

The system type is undefined before the first SET MODE command is sent. In order to avoid system conflicts during this time, the multiplex rate is set to 1:32, the CLK output oscillates with a frequency of 12 kHz, the $\overline{SYNC}$ pin outputs a high (V_{DD}) level and the row outputs toggle at a frequency of 12 kHz. This also ensures that the LCD remains blank at power-on for all system types. This information is summarized in Table 1.

Table 1 Cascade control.
Typically: R_{OSC} = 330 kΩ; f_{OSC} = 12 kHz; f_{CLK1} = 2 kHz; f_{CLK2} = 1.5 kHz.

EXT	DEVICE MODE	MULTIPLEX RATE	OSC	CLK OUTPUT	$\overline{SYNC}$
SYSTEM STATUS: after first SET-MODE					
V_{SS}	single	1:8; 1:16	connect R_{OSC}	f_{CLK1}	output
V_{DD}	single	1:8; 1:16	input f_{OSC}	f_{CLK1}	output
V_{SS}	first	1:24; 1:32	connect R_{OSC}	f_{OSC}	input
V_M	first	1:24; 1:32	input f_{OSC}	f_{OSC}	input
V_{DD}	second	1:24; 1;32	input f_{OSC}	$f_{CLK2/1}$	output
SYSTEM STATUS: before first SET-MODE					
V_{SS}	undefined	1:32	connect R_{OSC}	f_{OSC}	output V_{DD}
V_M	undefined	1:32	input f_{OSC}	f_{OSC}	output V_{DD}
V_{DD}	undefined	1:32	input f_{OSC}	f_{OSC}	output V_{DD}



(a) single device, internal clock.
(b) single device, external clock.
(c) cascaded system, internal clock.
(d) cascaded system, external clock.

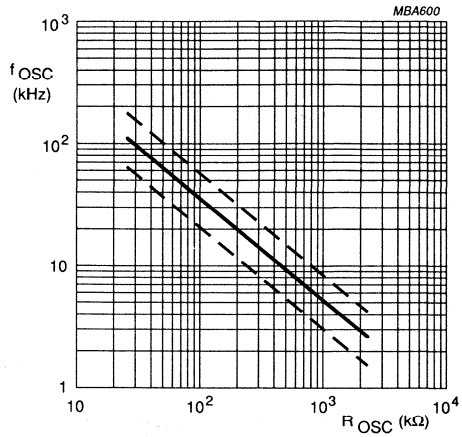
Fig.3 System types.

Oscillator

Timing signals are derived from an on-chip oscillator, whose frequency is determined by the value of the resistor connected between OSC and V_{SS}.

Internal clock

The clock signal for the system may be generated by the internal oscillator and prescaler. The frequency is determined by the value of the resistor R_{OSC}, see Fig. 4. For normal use a value of 330 kΩ is recommended. When a single PCF8568 is used, the clock signal for the column drivers is output at CLK and has a frequency one-sixth (multiplex rate 1:8, 1:16 and 1:32) or one-eighth (multiplex rate 1:24) of the oscillator frequency. In a cascaded system, the CLK output from the second device is fed to the column drivers.



Note: to avoid capacitive coupling, which could adversely affect oscillator stability, R_{OSC} should be placed as closely as possible to the OSC pin. If this proves to be a problem, a filtering capacitor may be connected in parallel to R_{OSC}.

Fig.4 Oscillator frequency as a function of R_{OSC}.

External clock

If an external clock is used, EXT must be connected to either V_{DD}, or V_M and the external clock signal to OSC. The external clock should have a 50% duty cycle in order to guarantee a DC free LCD waveform between power-on and the first set mode command. Table 2 summarizes the nominal CLK and $\overline{SYNC}$ frequencies.

Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the LCD threshold voltage (V_{th}). V_{th} is typically defined as the RMS voltage at which the LCD exhibits 10% contrast.

The PCF8568 generates the intermediate voltage bias levels internally using the V_{DD} and V_{LCD} supplies. For multiplex rates of 1:16, 1:24 and 1:32 a total of six bias levels are used including V_{DD}, V2, V3, V4 and V_{LCD}. Five bias levels are used for the 1:8 multiplex rate (V3 is set equal to V4 with a value half of the total operating voltage V_{OP}).

Buffered bias voltages are available for connection to the column drivers at pins VO3 and VO4. Table 3 shows the generated voltage bias levels for the PCF8568 as a function of V_{OP} (V_{OP} = V_{DD}-V_{LCD}), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{OP} is obtained by equating $V_{OFF(RMS)}$ with V_{th}.

Table 2 Signal frequencies required for nominal 64 Hz frame frequency.
A clock signal must always be present otherwise the LCD may be frozen in a DC state.

OSCILLATOR FREQUENCY f_{osc} (Hz) (R_{osc} = 330 kΩ)	FRAME FREQUENCY $f_{\overline{SYNC}}$ (Hz)	MULTIPLEX RATE	DIVISION RATIO	CLOCK FREQUENCY f_{CLK} (Hz)
12288	64	1:8; 1:16; 1:32	6	2048
12288	64	1:24	8	1536

Table 3 LCD bias generation

PARAMETER	MULTIPLEX RATE LEVEL 5	MULTIPLEX RATE LEVEL 6		
mux rate	1:8	1:16	1:24	1:32
$V2/V_{OP}$	0.750	0.800	0.830	0.850
$V3/V_{OP}$	0.500	0.600	0.661	0.700
$V4/V_{OP}$	0.500	0.400	0.339	0.300
$V5/V_{OP}$	0.250	0.200	0.170	0.150
$V_{OFF(RMS)}/V_{OP}$	0.293	0.245	0.214	0.193
$V_{ON(RMS)}/V_{OP}$	0.424	0.316	0.263	0.230
$D = V_{ON(RMS)}/V_{OFF(RMS)}$	1.446	1.291	1.230	1.196
V_{OP}/V_{th}	3.41	4.08	4.68	5.19

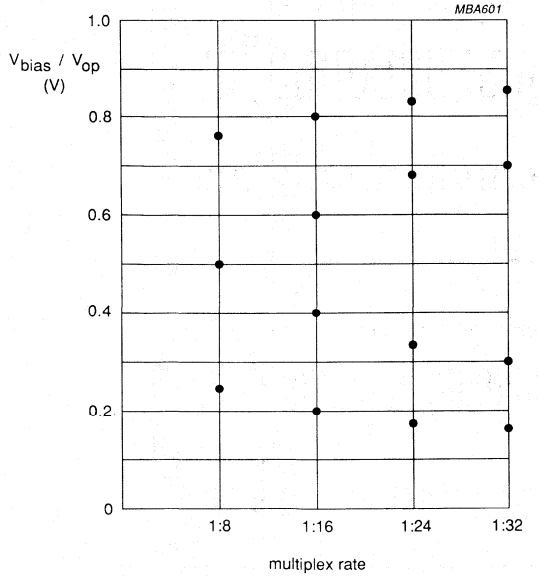


Fig.5 LCD bias voltages as a function of the multiplex rate.

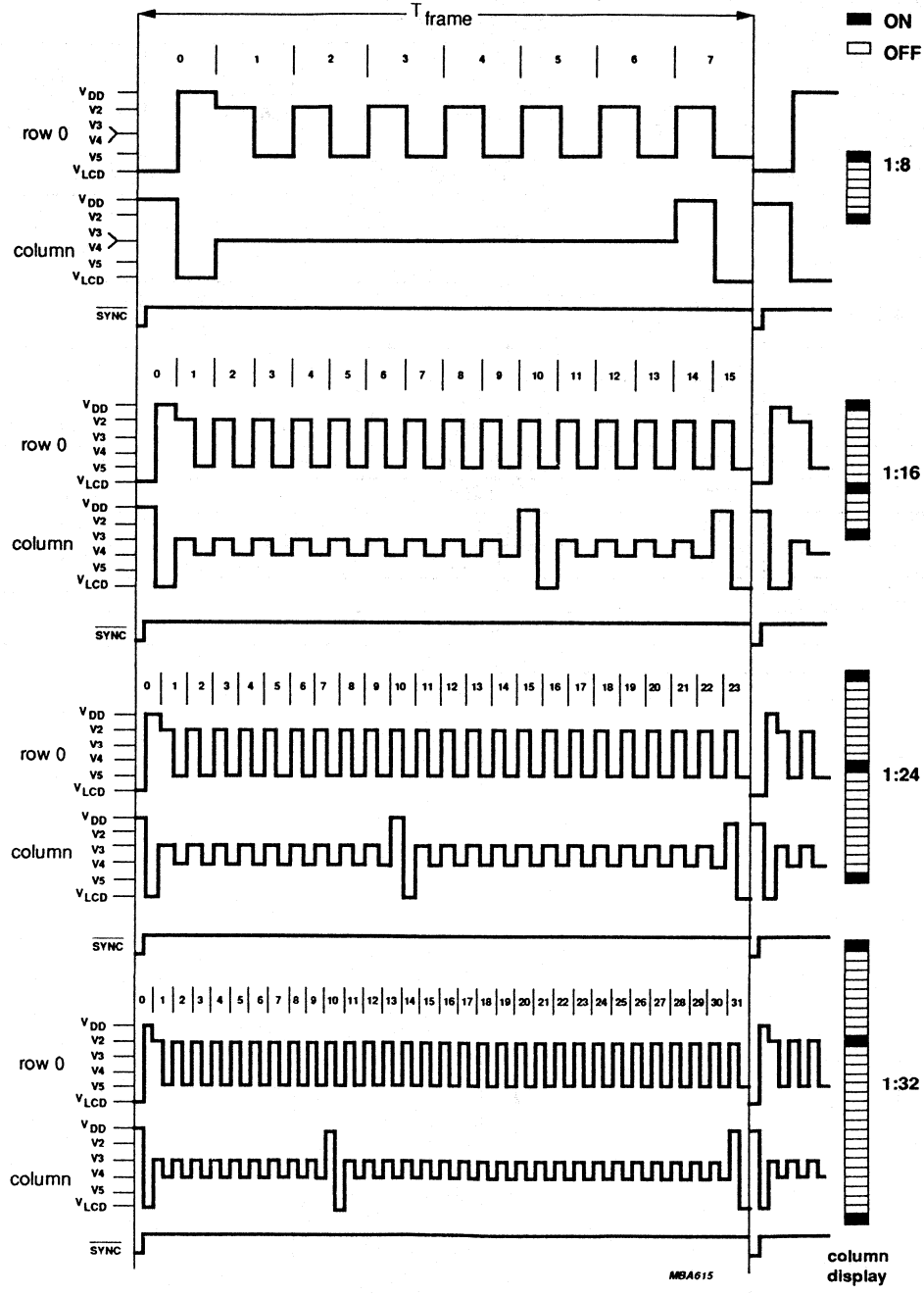


Fig.6 LCD row/column waveforms.

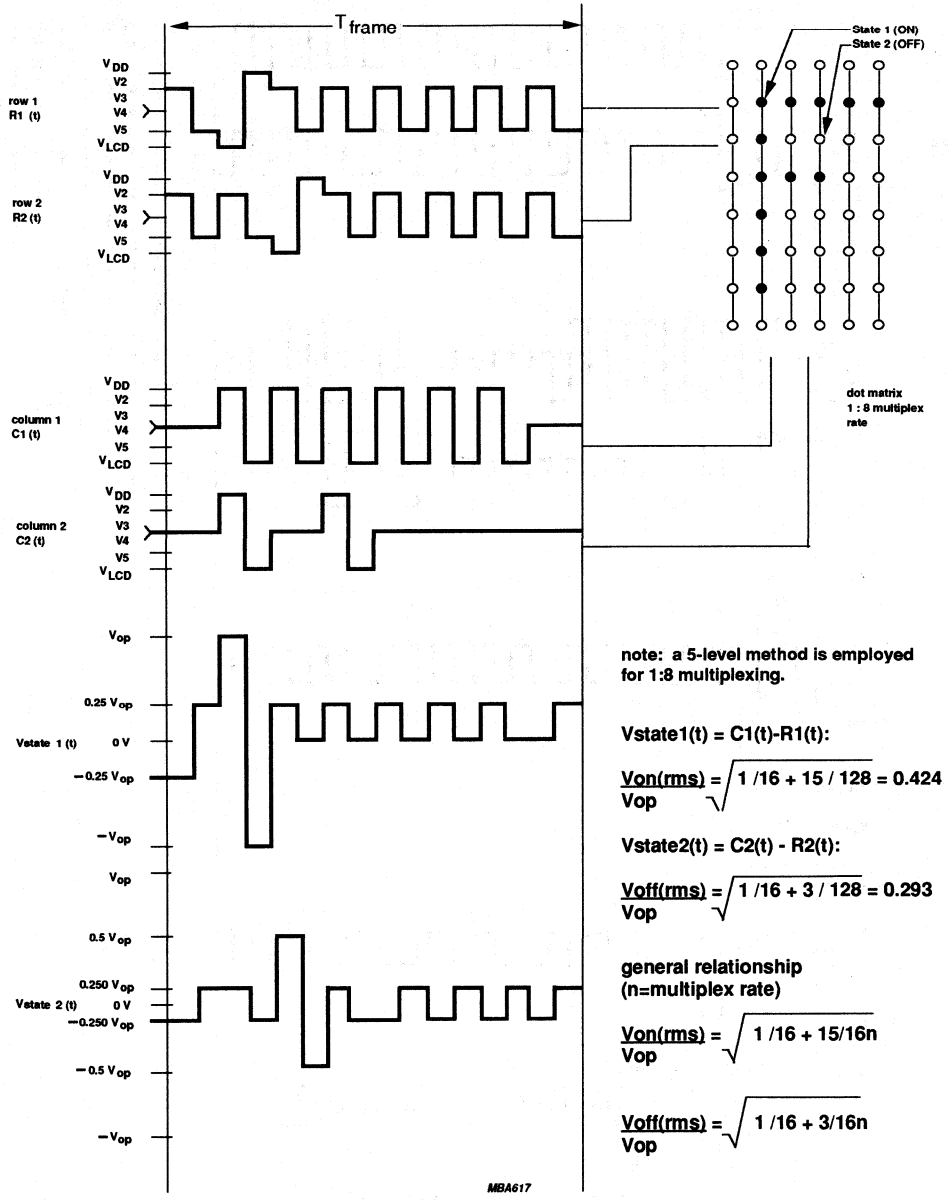


Fig.7 LCD drive mode waveforms for 1:8 multiplex.

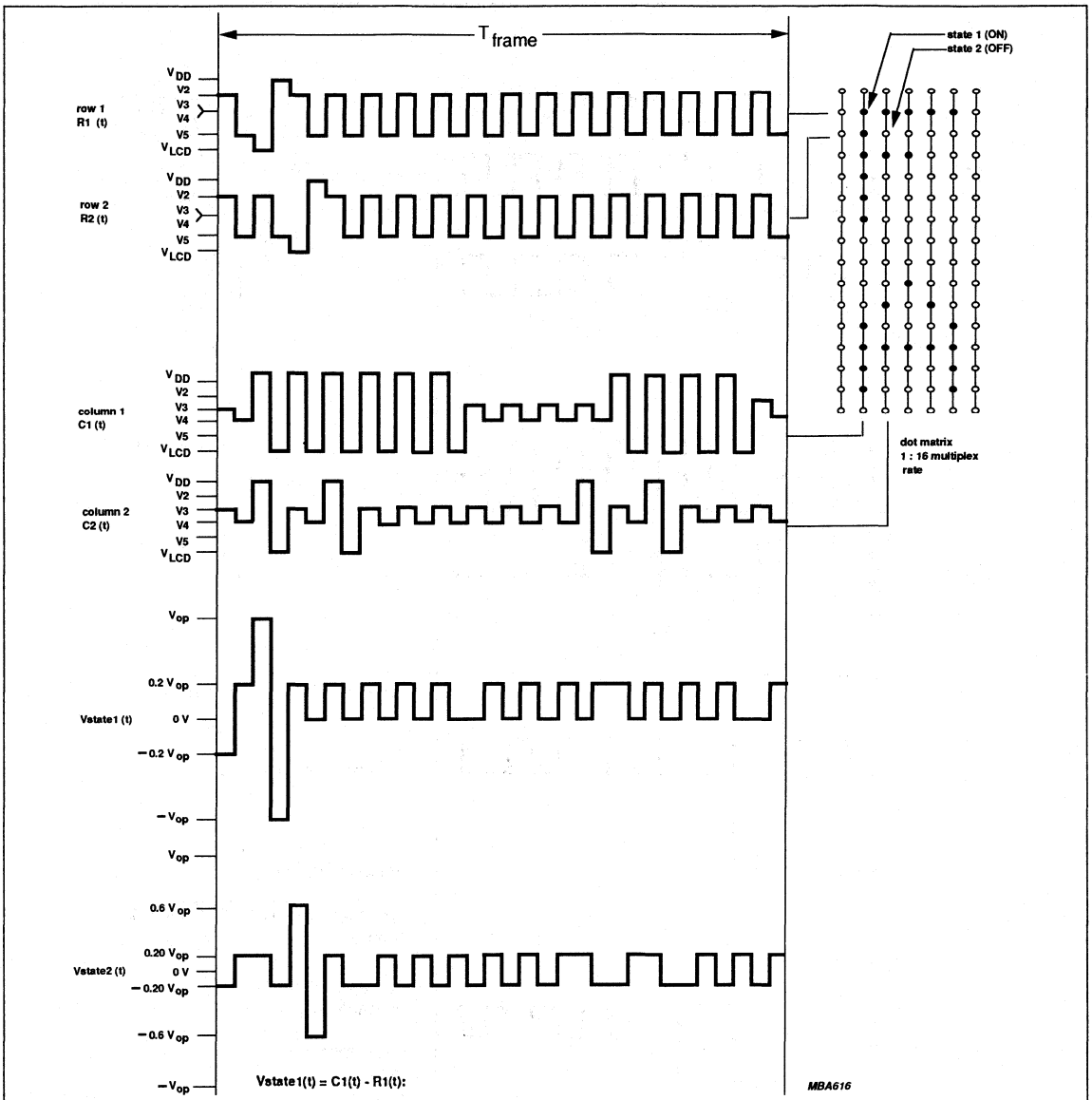


Fig.8 LCD drive mode waveforms for 1:16 multiplex.

Power-on Reset

At power-on the PCF8568 resets to a defined starting condition as follows:

1. Display blank.
2. I²C-bus interface is initialized.
3. Device in reset state awaiting first SET MODE (see Table 1).

Data transfers on the I²C-bus should be avoided for 1 ms following power-on to allow completion of the reset action.

Timing generation and control

The timing generation and control block of the PCF8568 organizes the internal data flow of the device and either generates or synchronizes with the LCD frame synchronization pulse $\overline{SYNC}$, whose period is an integer multiple of the clock period. This signal maintains the correct timing relationship between the PCF8568 and the column drivers (and, if also used, a cascaded PCF8568).

Row driver outputs

R0 to R15 are row outputs which must be connected to the LCD. Unused outputs should be left open-circuit. Using a multiplex rate of 1:8, two sets of row outputs are driven, thus facilitating split screen configurations; i.e. a row pulse appears simultaneously at R0 and R9, R1 and R10 etc.

Shift register

The row select pulse is shifted through the shift register. Timing is derived from the timing and control block.

Bias generator

The intermediate LCD bias voltages are generated in this block. Buffered row bias voltages (V2 and V5 in Fig. 1) are connected internally to the row driver outputs. Buffered column bias voltages are available at pins VO3 and VO4.

I²C-bus control

The I²C-bus controller detects the I²C-bus protocol, slave address and command bytes. It performs the conversion of the data input (serial-to-parallel). The PCF8568 acts as an I²C-bus slave receiver.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C-bus protocol

Two 7-bit slave addresses (0111100 and 0111101) are reserved for the PCF8568 and PCF8569 or PCF8579 column drivers (see note below). Depending on the address, which is defined by SA0, two types of LCD display systems can be distinguished on the same I²C-bus. This allows:

(a) one PCF8568 to operate with up to 32 PCF8579s on the same I²C-bus for very large applications

(b) the use of two types of LCD multiplex schemes on the same I²C-bus.

In most applications the PCF8568 will have the same slave address as the column drivers.

The I²C-bus protocol is shown in Fig.9. All communications are initiated with a start condition (S) from the I²C-bus master, which is followed by the desired slave address and the read/write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

The PCF8568 operates in slave receiver mode only, hence the read/write bit $R/\overline{W} = 0$. The device receives one or more commands following slave address acknowledgement. The commands are also acknowledged by all addressed devices on the bus. The last command must clear the continuation bit C. After the last command a series of data bytes for the column drivers may follow. The acknowledgement after each byte is made only by the (A0, A1, A2 and A3) addressed column driver. The PCF8568 ignores data bytes and does not acknowledge. After the last data byte has been acknowledged, the I²C-bus master issues a stop condition (P).

Note: the PCF8578 row/column driver also uses the slave addresses above and is also designed for use with the PCF8569 or PCF8579 column drivers. Either the PCF8578 row/column driver or the PCF8568 row driver can be used depending upon the application.

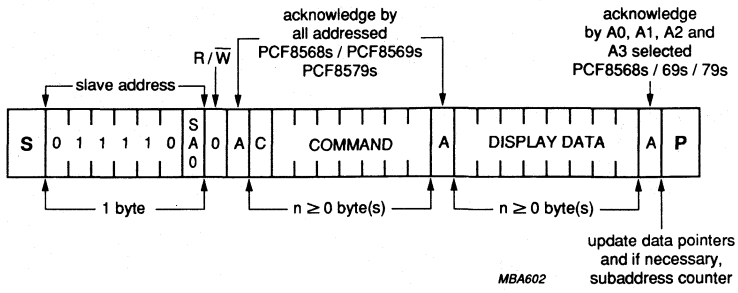


Fig.9 I²C-Bus protocol: master transmits to slave receiver.

Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. The most significant bit of a command is the continuation bit C (see Fig.10). When this bit is set, it indicates that the next byte to be transferred will also be a command. If the bit is reset, it indicates the conclusion of command transfer. Further bytes will be regarded as data. Commands are always transferred after a slave address with R/$\overline{W}$ = 0.

In an LCD system including the PCF8568, there are five commands. For the PCF8568 only one command, SET MODE, is relevant. All other commands are treated as NOP (No Operation) by the PCF8568. The SET MODE command is defined in Fig. 11.

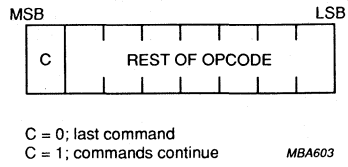


Fig.10 General format of command byte.

COMMAND / OPCODE	OPTIONS			DESCRIPTION
SET MODE C 1 0 0 E1 E0 M1 M0 Note: this bit must be zero	LCD DRIVE MODE BITS	M1	M0	DEFINES LCD DRIVE MODE
	1:8 MUX (8 ROWS)	0	1	
	1:16 MUX (16 ROWS)	1	0	
	1:24 MUX (24 ROWS)	1	1	
	1:32 MUX (32 ROWS)	0	0	
	DISPLAY STATUS BITS	E1	E0	DEFINES DISPLAY STATUS
	BLANK	0	0	
	NORMAL	0	1	
	ALL SEGMENTS ON	1	0	
	INVERSE VIDEO	1	1	

MBA604

Fig.11 Definition of the PCF8568 SET MODE command

CHARACTERISTICS OF THE I²C BUS

The I²C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

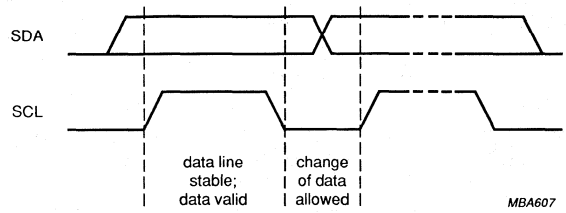


Fig.12 Bit transfer.

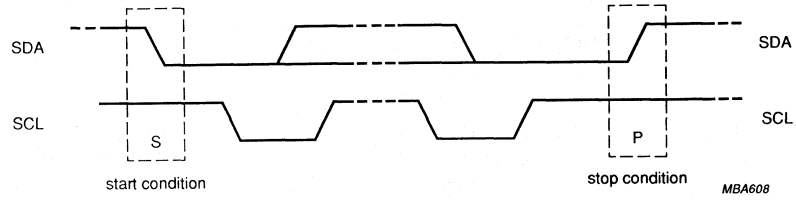


Fig.13 Definition of start and stop conditions.

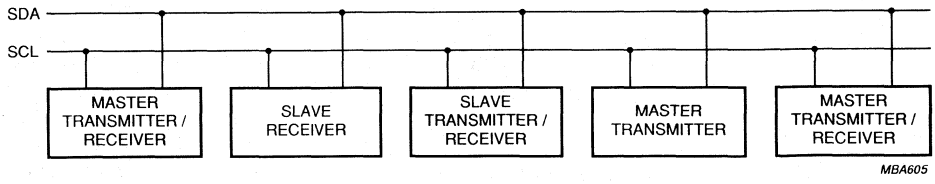
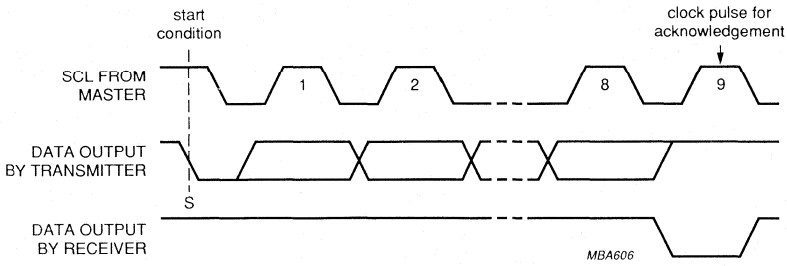


Fig.14 System configuration.



Note: the general characteristics and detailed specification of the I²C- bus are available on request.

Fig.15 Acknowledgement on the I²C-bus.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range	−0.5	+8.0	V
V_{LCD}	LCD supply voltage range voltage	V_{DD} −11	V_{DD}	V
$V_{I(1)}$	input voltage range at SDA, SCL, $\overline{SYNC}$, SA0, EXT, and OSC	V_{SS} −0.5	V_{DD} +0.5	V
$V_{O(1)}$	output voltage range at SDA, OSC, and $\overline{SYNC}$	V_{SS} −0.5	V_{DD} +0.5	V
$V_{O(2)}$	VO3, VO4, and RO-R15	V_{LCD} −0.5	V_{DD} +0.5	V
I_I	DC input current	−10	10	mA
I_O	DC output current	−10	10	mA
I_{DD}, I_{SS} or I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	−50	50	mA
P_{tot}	power dissipation per package	-	400	mW
P_O	power dissipation per output	-	100	mW
T_{stg}	storage temperature range	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices (see 'Handling MOS Devices'.)

CHARACTERISTICS

V_{DD} = 2.5 V to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9.0 V; T_{amb} = −40 to +85 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC						
V_{DD}	supply voltage		2.5	-	6.0	V
V_{LCD}	LCD supply voltage		V_{DD} −9	-	V_{DD} −3.5	V
$I_{DD(1)}$	supply current external clock	note 1; f_{OSC} = 12 kHz	-	62	120	µA
$I_{DD(2)}$	supply current internal clock	note 1; R_{OSC} = 330 kΩ	-	67	150	µA
V_{POR}	power-on reset level	note 2	-	1.3	1.8	µA
logic (except EXT)						
V_{IL}	input logic LOW		V_{SS}	-	0.3 V_{DD}	V
V_{IH}	input voltage HIGH		0.7 V_{DD}	-	V_{DD}	V
EXT						
$V_{IL(E)}$	input voltage LOW		V_{SS}	-	V_{SS} +0.1	V
$V_{IH(E)}$	input voltage HIGH		V_{DD} −0.1	-	V_{DD}	V
V_M	input voltage V_M		1.15	-	V_{DD} −1.15	V
$I_{OL(1)}$	output current LOW at $\overline{SYNC}$ and CLK	V_{OL} = 1.0 V V_{DD} = 5.0 V	1	-	-	mA
$I_{OH(1)}$	output current HIGH at $\overline{SYNC}$ and CLK	V_{OH} = 4.0 V V_{DD} = 5.0 V	-	-	−1	mA
$I_{OL(2)}$	SDA output current LOW	V_{OL} = 0.4 V V_{DD} = 5.0 V	3.0	-	-	mA
$I_{L(1)}$	leakage current at SDA, SCL, $\overline{SYNC}$, SA0 and EXT	V_I = V_{DD} or V_{SS}	−1	-	1	µA
$I_{L(2)}$	leakage current at OSC	note 3; V_I = V_{DD} or V_{SS}	−1	-	1	µA
CI	input capacitor	note 4	-	-	5	pF
LCD Outputs						
R_O	output resistance at R0-R15	note 5	-	1.5	3.0	kΩ
±VTOL	V2, VO3, VO4 and V5 tolerance	note 6	-	20	100	mV
ISO	I (source) on VO3; VO4	note 7	-	-	−1.5	mA
ISI	I (sink) on VO3, VO4	note 8	1.5	-	-	mA
AC (note 9)						
f_{CLK1}	clock frequency at multiplex rates of 1:8, 1:16 and 1:32	R_{OSC} = 330 kΩ; V_{DD} = 6 V	1.2	2.1	3.3	kHz
f_{CLK2}	clock frequency at multiplex rate of 1:24	R_{OSC} = 330 kΩ; V_{DD} = 6 V	0.9	1.6	2.5	kHz
f_{OSC}	external clock		7.7	12.4	19.2	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AC (note 9)						
$t_{P\overline{SYNC}}$	$\overline{SYNC}$ propagation delay		-	-	500	ns
t_{PLCD}	driver delays	$V_{DD} - V_{LCD} = 9$ V	-	-	100	µs
I²C-bus						
f_{SCL}	SCL clock frequency		-	-	100	kHz
t_{SW}	tolerable spike width on bus		-	-	100	ns
t_{BUF}	bus free time		4.7	-	-	µs
$t_{SU;STA}$	start condition set-up time	repeated start codes only	4.7	-	-	µs
$t_{HD;STA}$	start condition on hold time		4.0	-	-	µs
t_{LOW}	SCL LOW time		4.7	-	-	µs
t_{HIGH}	SCL HIGH time		4.0	-	-	µs
t_r	SCL and SDA rise time		-	-	1.0	µs
t_f	SCL and SDA fall time		-	-	0.3	µs
$t_{SU;DAT}$	data set-up time		250	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{VD;DAT}$	SCL LOW to data out valid		-	-	3.4	µs
$t_{SU;STO}$	stop condition set-up time		4.0	-	-	µs

Notes

1. Outputs are open; inputs at V_{DD} or V_{SS}; I²C-bus inactive; external clock with 50% duty cycle (I_{DD1} only).
2. Resets all logic when $V_{DD} < V_{POR}$.
3. EXT = V_{DD} or V_M.
4. Periodically sampled; not 100% tested.
5. Resistance of output terminal (R0 to R15) with $I_{LOAD} = 150$ µA; $V_{OP} = V_{DD}-V_{LCD} = 9.0$ V; outputs measured one at a time.
6. LCD outputs open.
7. $V_{OP} = V_{DD}-V_{LCD} = 9.0$ V; VO3 = 5.8 V; VO4 = 2.2 V; 1:32 multiplex.
8. $V_{OP} = V_{DD}-V_{LCD} = 9.0$ V; VO3 = 6.8 V; VO4 = 3.2 V; 1:32 multiplex.
9. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

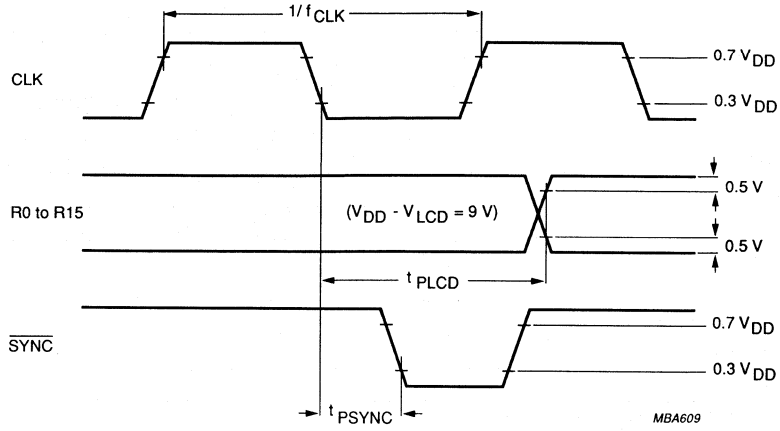


Fig.16 Driver timing waveforms.

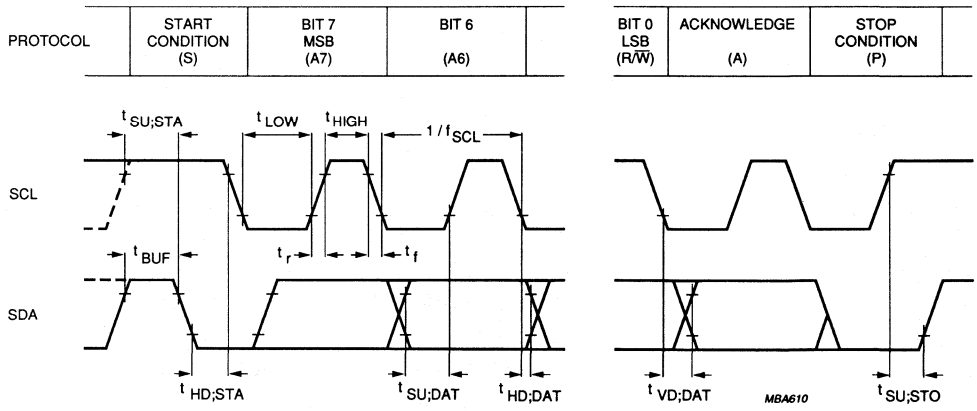


Fig.17 I²C timing diagram.

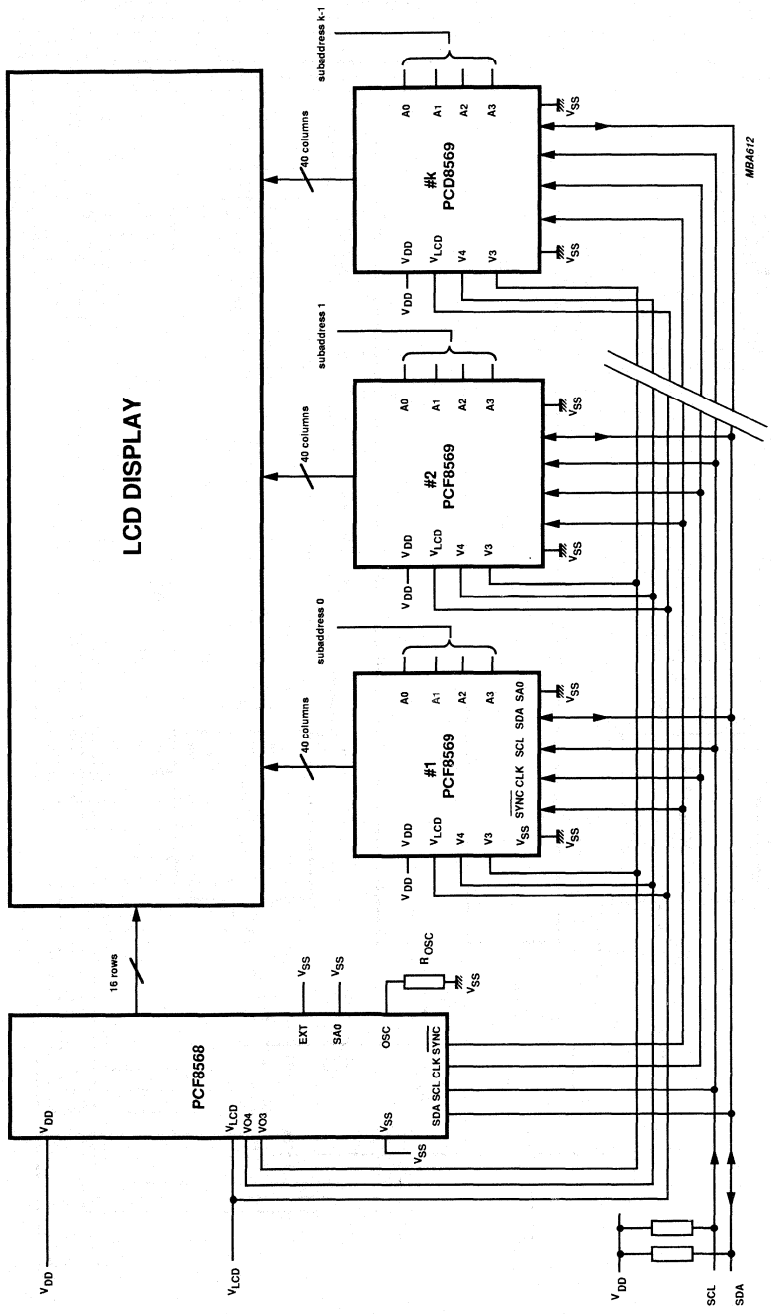


Fig.18 Typical driver system with 1:16 multiplex.

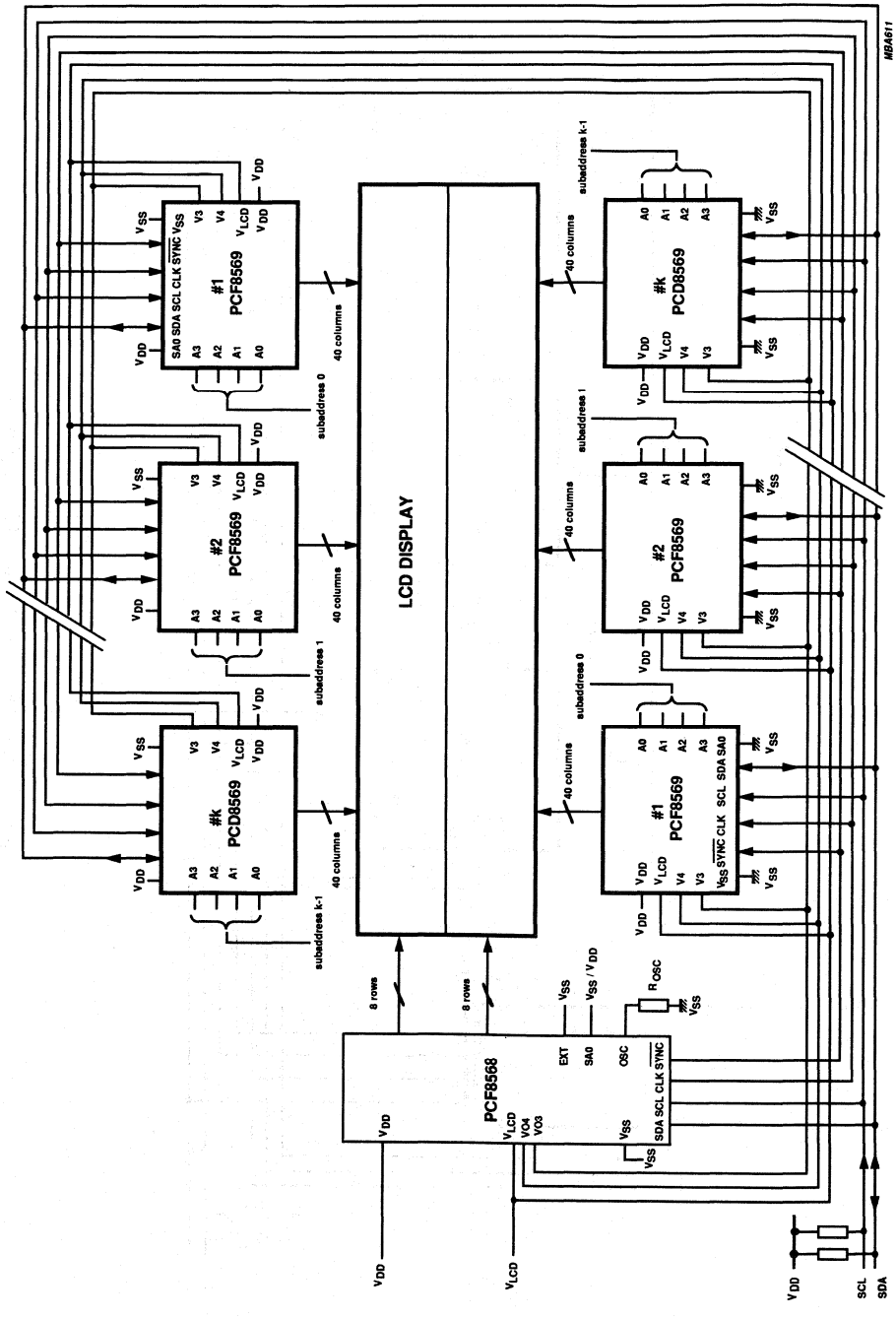


Fig.19 Split screen application with 1:8 multiplex for improved contrast.

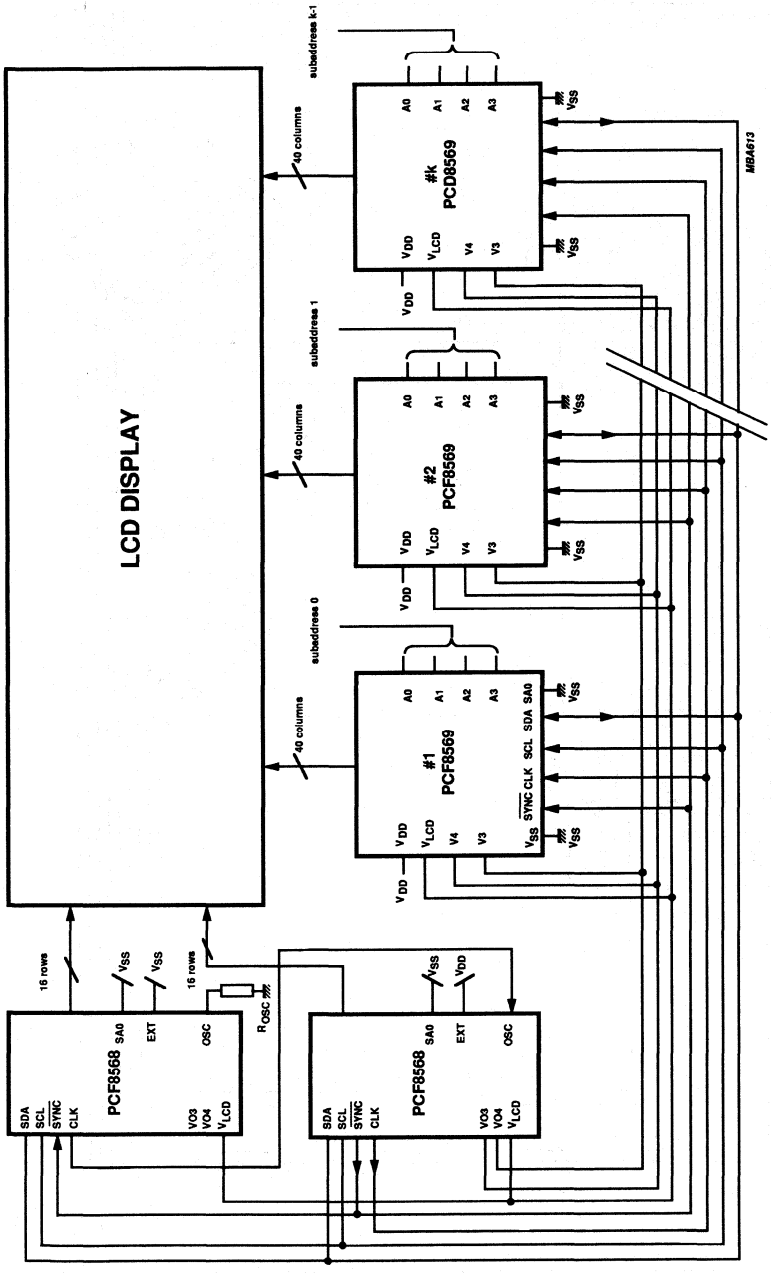


Fig.20 Cascaded LCD driver system with 1:32 multiplex rate.

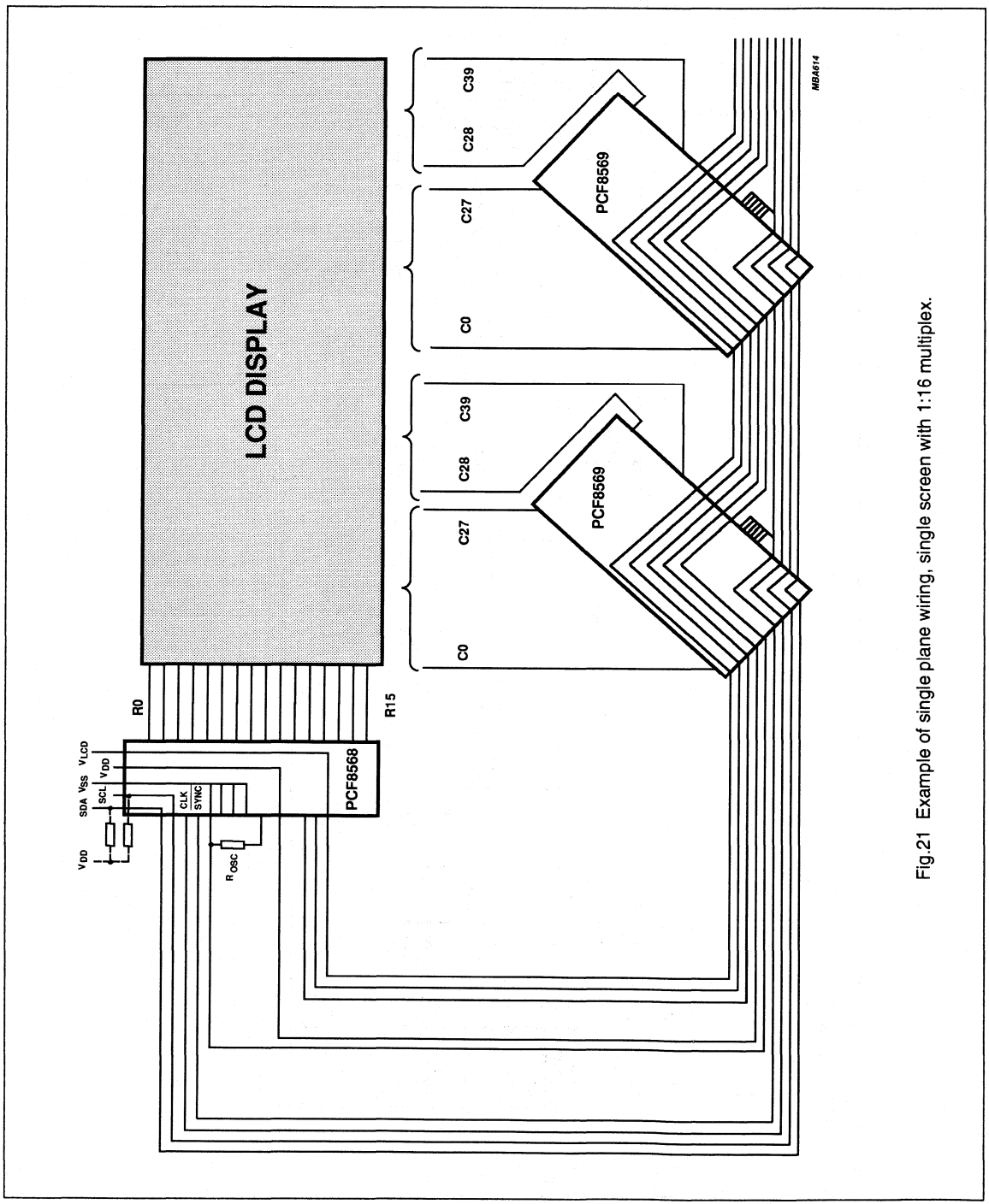
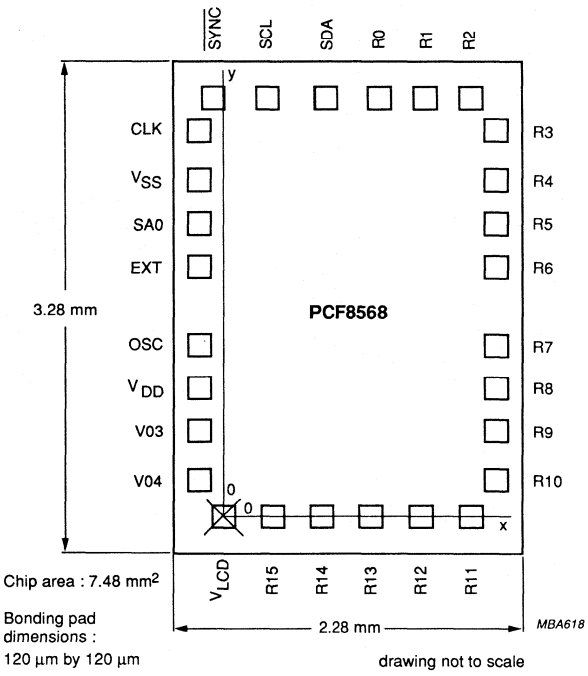


Fig.21 Example of single plane wiring, single screen with 1:16 multiplex.



See table 4: Bonding pad locations (X Y coordinates)

Fig.24 Bonding pad locations (PCF8568U/7 un-encapsulated).

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8569 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8 or 1:16. The device has 40 outputs and can drive 16 x 40 dots in a 16 row multiplexed LCD. Up to 16 PCF8569s can be cascaded and up to 32 devices may be used on the same I^2C-bus (using the two slave addresses). The device is optimized for use with the PCF8568/78/79 family of LCD row/column drivers. Together the PCF8568, PCF8578 and PCF8569 form a general LCD dot matrix driver chip set, capable of driving displays of up to 20 480 dots. The PCF8569 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

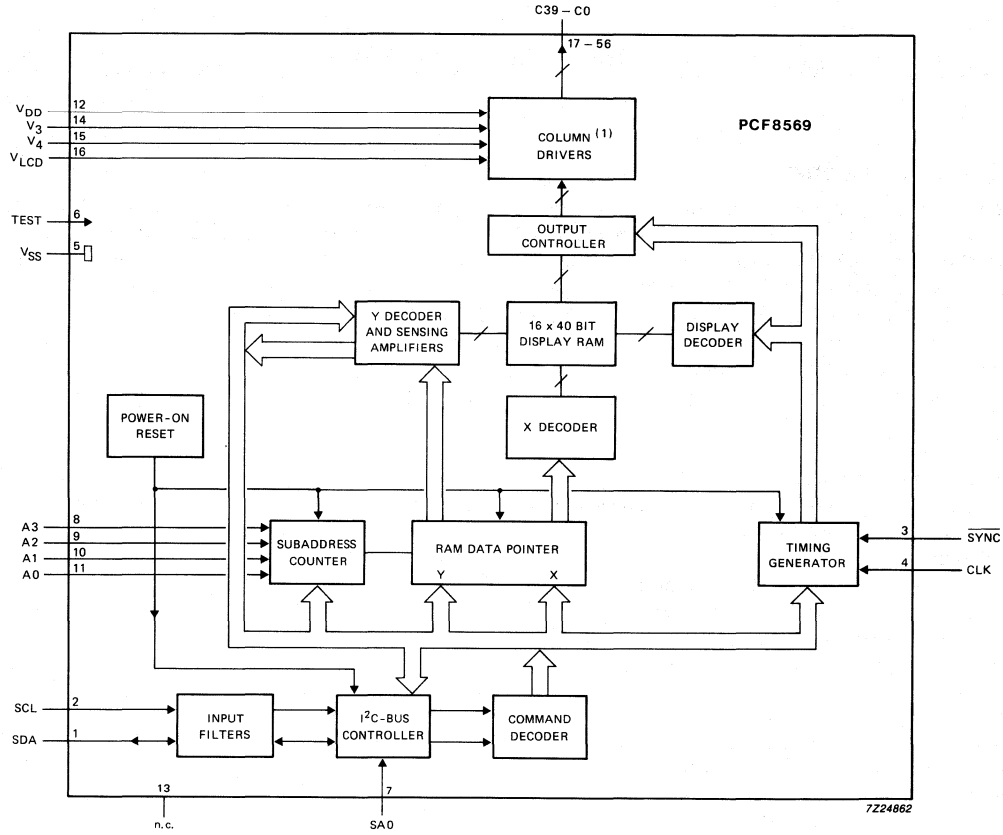
- LCD column driver
- Used in conjunction with the PCF8568 or PCF8578, this device forms part of a chip set capable of driving up to 20 480 dots.
- 40 column outputs
- Selectable multiplex rates; 1:8 or 1:16
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications
- 640-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack or 64-lead tab module

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8569T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8569V: 64-lead tape-automated-bonding (tab) module (SOT267).



(1) LCD voltage levels, all other blocks operate at logic levels.

Fig.1 Block diagram (pin numbers shown for VSO56; SOT190).

PINNING

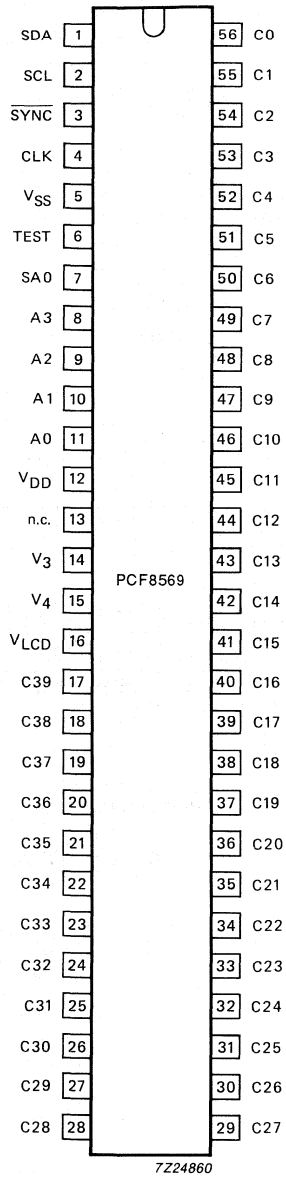
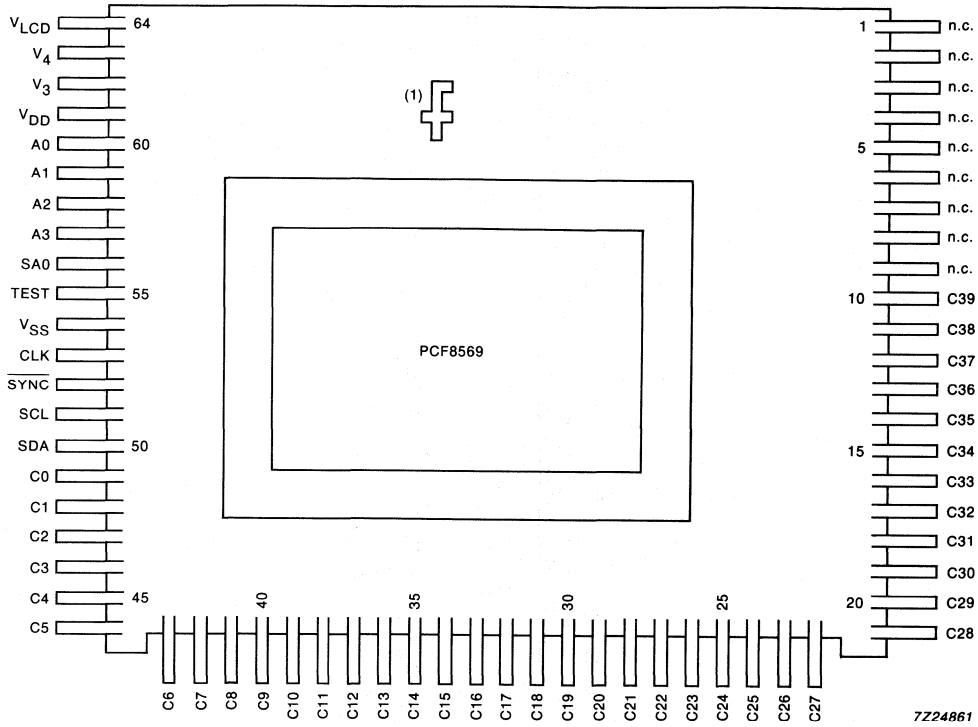


Fig.2 (a) Pinning diagram: VSO56; SOT190.

PINNING (continued)



(1) Orientation mark.

Fig.2 (b) Pinning diagram: SOT267.

mnemonic	pin number		description
	SOT190	SOT267	
SDA	1	50	I^2C-bus serial data line
SCL	2	51	I^2C-bus serial clock line
$\overline{SYNC}$	3	52	cascade synchronization input
CLK	4	53	external clock input
V_{SS}	5	54	ground (logic)
TEST	6	55	test pin (connect to V_{SS})
SA0	7	56	I^2C-bus slave address input (bit 0)
A3 to A0	8 to 11	57 to 60	I^2C-bus subaddress inputs
V_{DD}	12	61	positive supply voltage
n.c.	13 *	1 - 9	not connected
V_3 to V_4	14 to 15	62 to 63	LCD bias voltage inputs
V_{LCD}	16	64	LCD supply voltage
C39 to C0	17 to 56	10 to 49	LCD column driver outputs

* Do not connect, this pin is reserved.

FUNCTIONAL DESCRIPTION

The PCF8569 column driver is designed for use with the PCF8568. Together they form a general purpose LCD dot matrix chip set.

Typically up to 16 PCF8569s may be used with one PCF8568. Each of the PCF8569s is identified by a unique 4-bit hardware subaddress, set by pins A0 to A3. The PCF8568 can operate with up to 32 PCF8569s when using two I^2C-bus slave addresses. The two slave addresses are set by the logic level on input SA0.

The PCF8569 may also be used in mixed systems with the PCF8579 column driver and PCF8578 row/column driver.

Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the LCD threshold voltage (V_{th}). V_{th} is typically defined as the RMS voltage at which the LCD exhibits 10% contrast. Table 1 shows the optimum voltage bias levels for the PCF8568/PCF8569 chip set as functions of V_{op} ($V_{op} = V_{DD} - V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{op} is obtained by equating $V_{off(rms)}$ with V_{th}.

Table 1 Optimum LCD bias voltages

parameter	multiplex rate	
	1:8	1:16
$\frac{V_2}{V_{op}}$	0.739	0.800
$\frac{V_3}{V_{op}}$	0.522	0.600
$\frac{V_4}{V_{op}}$	0.478	0.400
$\frac{V_5}{V_{op}}$	0.261	0.200
$\frac{V_{off(rms)}}{V_{op}}$	0.297	0.245
$\frac{V_{on(rms)}}{V_{op}}$	0.430	0.316
$D = \frac{V_{on(rms)}}{V_{off(rms)}}$	1.447	1.291
$\frac{V_{op}}{V_{th}}$	3.37	4.08

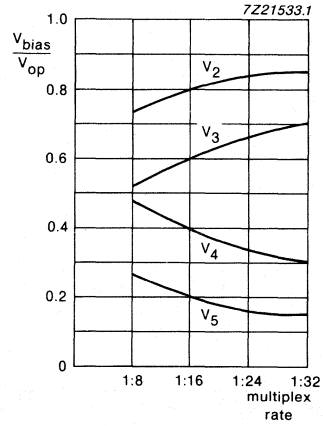


Fig.3 LCD bias voltage as a function of the multiplex rate.

Power-on reset

At power-on the PCF8569 resets to a defined starting condition as follows:

1. Display blank (in conjunction with PCF8568 or PCF8578)
2. Start bank 0 selected
3. Data pointer is set to X, Y address 0, 0
4. Character mode
5. Subaddress counter is set to 0
6. I^2C-bus is initialized.

Data transfers on the I^2C-bus should be avoided for 1 ms following power-on, to allow completion of the reset action.

FUNCTIONAL DESCRIPTION (continued)

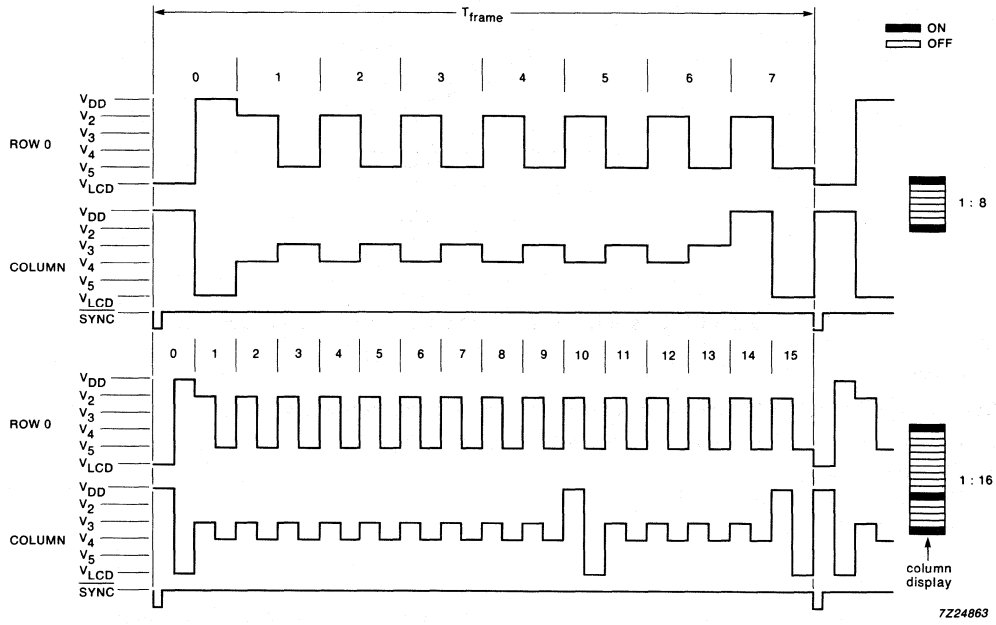
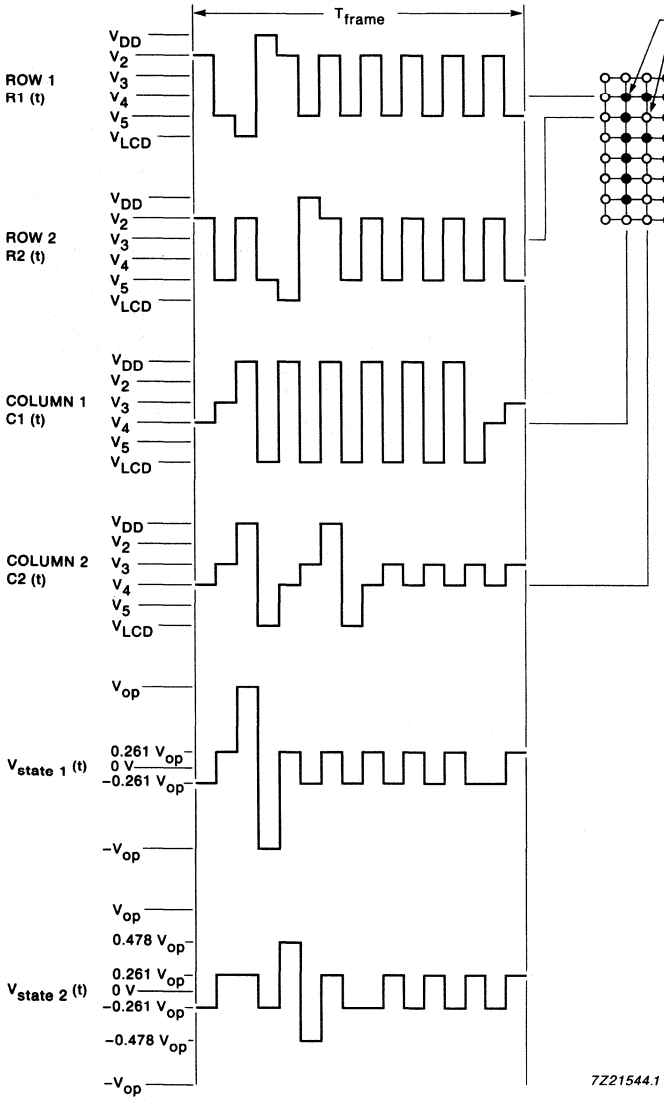


Fig.4 LCD row/column waveforms.



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{8} + \frac{\sqrt{8}-1}{8(\sqrt{8}+1)}} = 0.430$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{8}-1)}{\sqrt{8}(\sqrt{8}+1)^2}} = 0.297$$

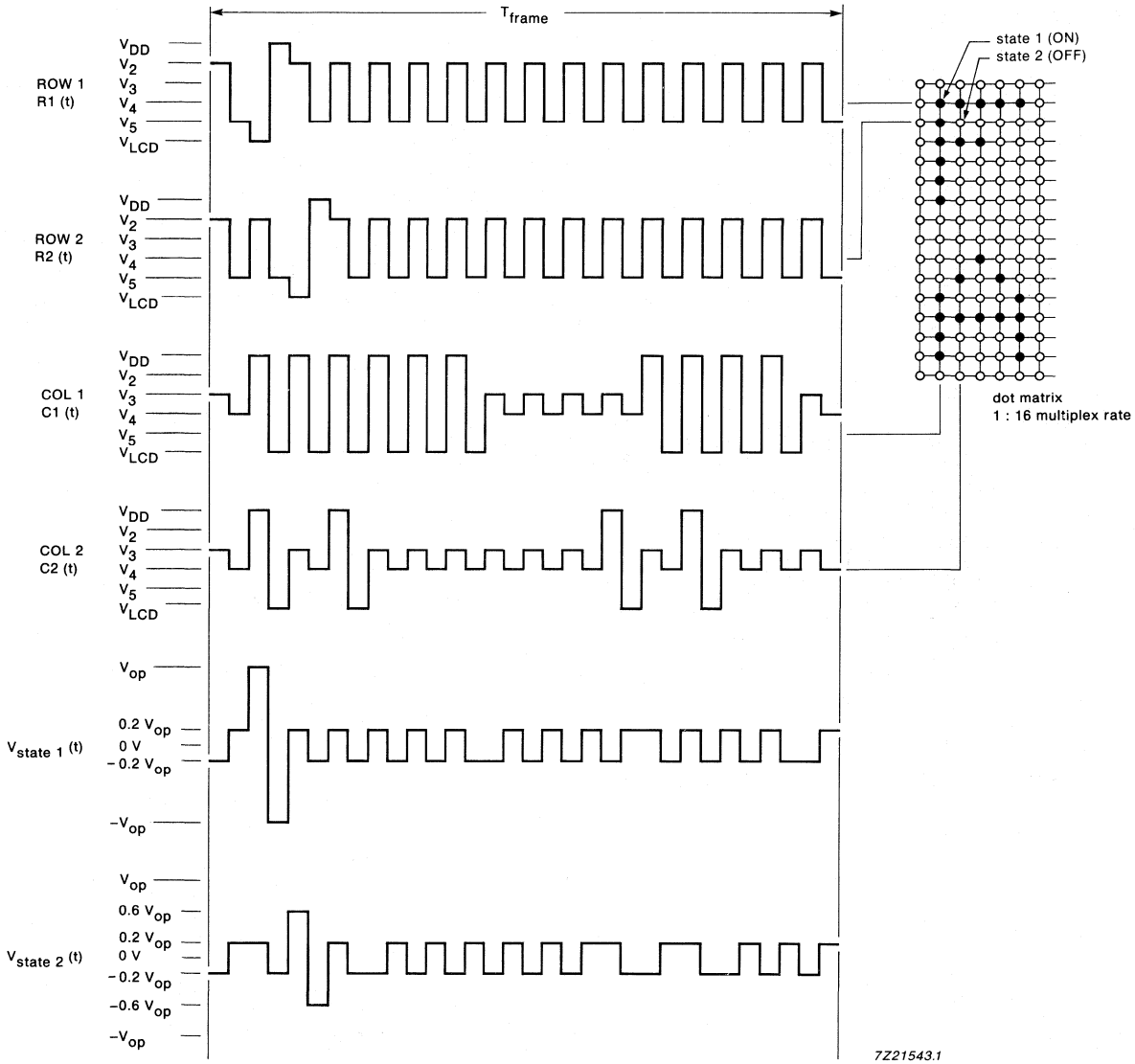
general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$$

Fig.5 LCD drive mode waveforms for 1:8 multiplex rate.

FUNCTIONAL DESCRIPTION (continued)



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{16} + \frac{\sqrt{16} - 1}{16\,(\sqrt{16} + 1)}} = 0.316$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{16} - 1)}{\sqrt{16}\,(\sqrt{16} + 1)^2}} = 0.245$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n} - 1}{n\,(\sqrt{n} + 1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{n} - 1)}{\sqrt{n}\,(\sqrt{n} + 1)^2}}$$

Fig.6 LCD drive mode waveforms for 1:16 multiplex rate.

Timing generator

The timing generator of the PCF8569 organizes the internal data flow from the RAM to the display drivers. An external synchronization pulse $\overline{SYNC}$ is received from the PCF8568 or PCF8578. This signal maintains the correct timing relationship between cascaded devices.

Column drivers

Outputs C0 to C39 are column drivers which must be connected to the LCD. Unused outputs should be left open-circuit.

Display RAM

The PCF8569 contains a 16 x 40 bit static RAM which stores the display data. The RAM is divided into 2 banks of 40 bytes (2 x 8 x 40 bits). During RAM access, data is transferred to/from the RAM via the I^2C-bus.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows an individual data byte or a series of data bytes to be written into or read from the display RAM, as specified by commands sent on the I^2C-bus.

Subaddress counter

The storage and retrieval of display data is dependent on the content of the subaddress counter. Storage and retrieval take place only when the contents of the subaddress counter agree with the hardware subaddress at pins A0, A1, A2 and A3.

I^2C-bus controller

The I^2C-bus controller detects the I^2C-bus protocol, slave address, commands and display data bytes. It performs the conversion of the data input (serial-to-parallel) and the data output (parallel-to-serial). The PCF8569 acts as an I^2C-bus slave transmitter/receiver. Device selection depends on the I^2C-bus slave address, the hardware subaddress and the commands transmitted.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

FUNCTIONAL DESCRIPTION (continued)

RAM access

There are two RAM ACCESS modes:

- Character
- Half-graphic

These modes are specified by bits G1 and G0 of the RAM ACCESS command. The RAM ACCESS command controls the order in which data is written to or read from the RAM (see Fig.7).

To access RAM data, the user specifies the location for the first byte (see Fig.8):

- Device subaddress (specified by the DEVICE SELECT command)
- RAM X-address (specified by the LOAD X-ADDRESS command)
- RAM bank (specified by bit Y0 of the RAM ACCESS command)

Subsequent data bytes will be written or read according to the chosen RAM access mode. Device subaddresses are automatically incremented between devices until the last device is reached. If the last device has subaddress 15, further display data transfers will lead to a wrap-around of the subaddress to 0.

Display control

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD, via the column outputs. The number of rows scanned depends on the multiplex rate set by bits M1 and M0 of the SET MODE command.

The display status (all dots on/off and normal/inverse video) is set by bits E1 and E0 of the SET MODE command. For bank switching, the RAM bank corresponding to the top of the display is set by bits B0 of the SET START BANK command. This is shown in Fig.9. This feature is useful when scrolling in alphanumeric applications.

TEST pin

The TEST pin must be connected to V_{SS}.

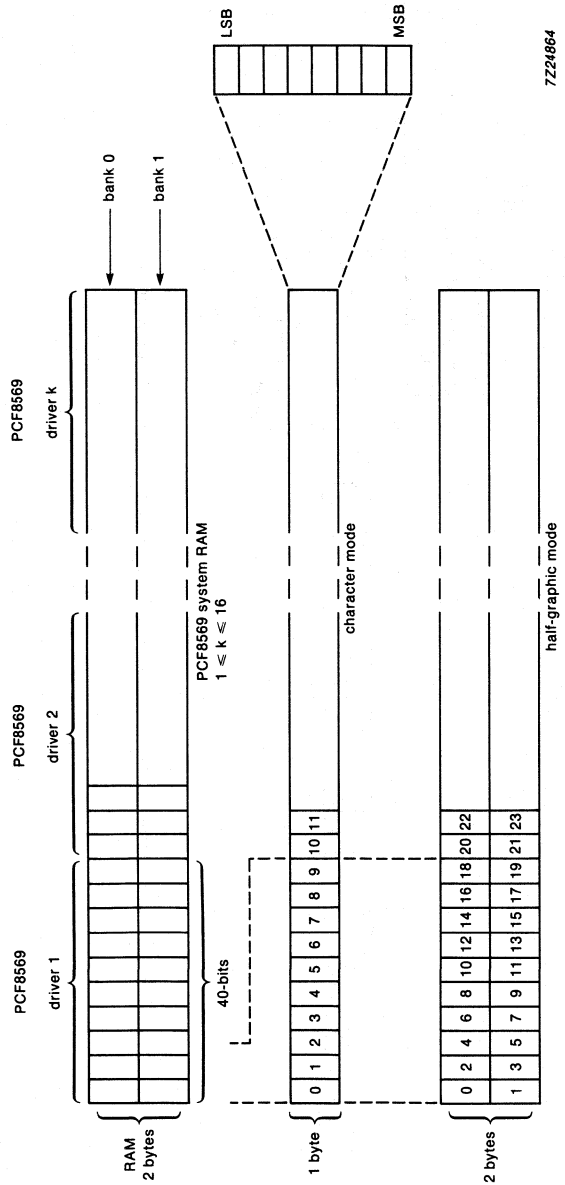


Fig.7 RAM ACCESS mode.

FUNCTIONAL DESCRIPTION (continued)

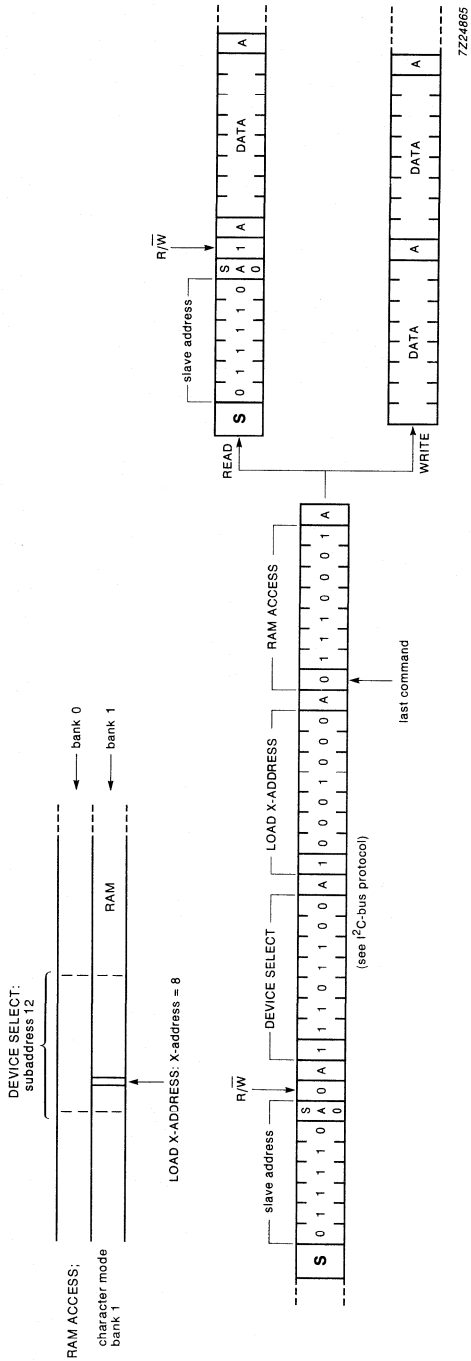


Fig.8 Example of commands specifying initial data byte RAM locations.

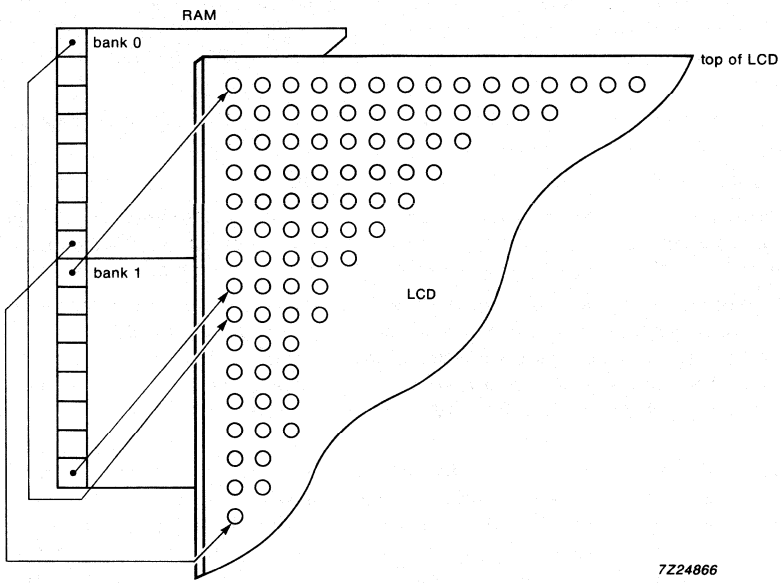


Fig.9 Relationship between display and SET START BANK; 1:16 multiplex rate and start bank = 1.

I²C-BUS PROTOCOL

Two 7-bit slave addresses (0111100 and 0111101) are reserved for the PCF8568/69/78/79 family. The least-significant bit of the slave address is set by connecting input SA0 to either 0 (V_{SS}) or 1 (V_{DD}). Therefore, two types of circuit can be distinguished on the same I²C-bus which allows for example:

(a) one PCF8568 to operate with up to 32 PCF8569s on the same I²C-bus for very large applications.
(b) the use of two types of LCD multiplex schemes on the same I²C-bus.

In most applications all circuits will have the same slave address.

The I²C-bus protocol is shown in Fig. 10. All communications are initiated with a start condition (S) from the I²C-bus master, which is followed by the desired slave address and read/write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

In WRITE mode (indicated by setting the read/write bit LOW) one or more commands follow the slave address acknowledgement. The commands are also acknowledged by all addressed devices on the bus. The last command must clear the continuation bit C. After the last command a series of data bytes may follow. The acknowledgement after each byte is made only by the (A0, A1, A2 and A3) addressed PCF8569. After the last data byte has been acknowledged, the I²C-bus master issues a stop condition (P).

In READ mode, indicated by setting the read/write bit HIGH, data bytes may be read from the RAM following the slave address acknowledgement. After this acknowledgement the master transmitter becomes a master receiver and the PCF8569 becomes a slave transmitter. The master receiver must acknowledge the reception of each byte in turn. The master receiver must signal an end of data to the slave transmitter, by **not** generating an acknowledge on the last byte clocked out of the slave. The slave transmitter then leaves the data line HIGH, enabling the master to generate a stop condition (P).

Display bytes are written into, or read from, the RAM at the address specified by the data pointer and subaddress counter. Both the data pointer and subaddress counter are automatically incremented, enabling a stream of data to be transferred either to, or from, the intended devices.

In multiple device applications, the hardware subaddress pins of the PCF8569s (A0, A1, A2 and A3) are connected to V_{SS} or V_{DD} to represent the desired hardware subaddress code. If two or more devices share the same slave address, then each device **must** be allocated a unique hardware subaddress.

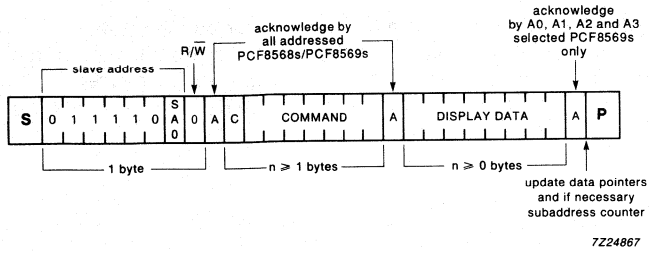


Fig.10(a) Master transmits to slave receiver (WRITE mode).

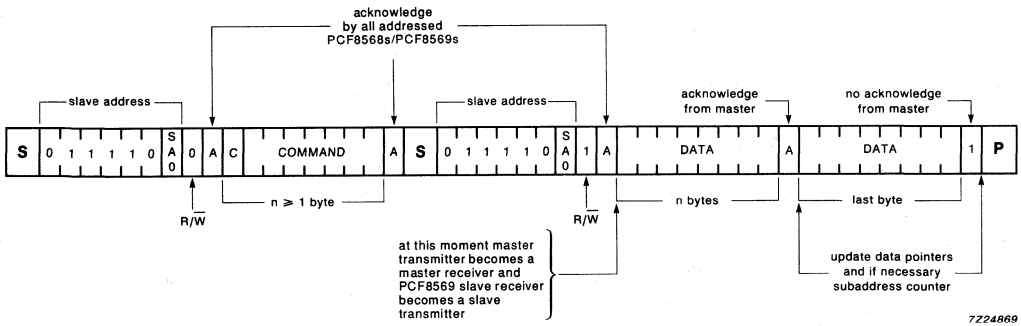


Fig.10(b) Master reads after sending command string (WRITE commands; READ data).

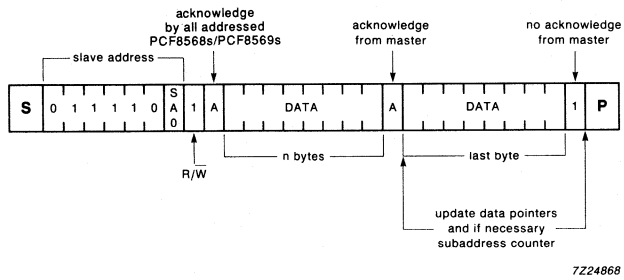
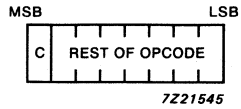


Fig.10(c) Master reads-slave immediately after sending slave address (READ mode).

I²C-BUS PROTOCOL (continued)

Command decoder

The command decoder indentifies command bytes that arrive on the I²C-bus. The most-significant bit of a command is the continuation bit C (see Fig.11). When this bit is set, it indicates that the next byte to be transferred will be a command. If the bit is reset, it indicates the conclusion of the command transfer. Further bytes will be regarded as display data. Commands are transferred in WRITE mode only.



C = 0; last command
C = 1; commands continue

Fig.11 General format of command byte.

The five commands available to the PCF8569 are defined in Table 2.

Table 2 Summary of commands

code	command	description
C 0 D D D D D D	LOAD X-ADDRESS	0 to 39
C 1 0 D D D D D	SET MODE	multiplex rate, display status
C 1 1 0 D D D D	DEVICE SELECT	defines device subaddress
C 1 1 1 0 D 0 D	RAM ACCESS	access modes, bank select
C 1 1 1 1 1 0 D	SET START BANK	defines bank at top of LCD

Where:

C = command continuation bit
D = may be a logic 1 or 0.

Table 3 Definition of PCF8569 commands

command / opcode	options	description
SET MODE C 1 0 T E1 E0 M1 M0	LCD drive mode bits M1 M0 1:8 MUX (8 rows) 0 1 1:16 MUX (16 rows) 1 0 1 1 0 0	defines LCD drive mode not used not used
	display status bits E1 E0 blank 0 0 normal 0 1 all segments on 1 0 inverse video 1 1	defines display status
	system type bit T PCF8568/78 row only 0 PCF8578 mixed mode 1 or PCF8568 test mode	defines system type no operation (reserved for row driver)
SET START BANK C 1 1 1 1 1 0 B0	start bank pointer bit B0 bank 0 0 bank 1 1	defines pointer to RAM bank corresponding to the top of the LCD. Useful for scrolling, pseudo-motion and background preparation of new display
DEVICE SELECT C 1 1 0 A3 A2 A1 A0	bits A3 A2 A1 A0 4-bit binary value of 0 to 15	four bits of immediate data, bits A0 to A3 are transferred to the subaddress counter to define one of sixteen hardware subaddresses

I²C BUS PROTOCOL (continued)

Table 3 (continued)

command / opcode	options	description
RAM ACCESS C 1 1 1 0 G0 0 Y0	RAM access mode bit G0 character 0 half graphic 1	defines the auto-increment behaviour of the address for RAM access
	bit Y0 start bank 0 0 start bank 1 1	one bit of immediate data, bit Y0 is transferred to the Y-address pointer to define one of two banks for RAM access
LOAD X-ADDRESS C 0 X5 X4 X3 X2 X1 X0	bits X5 X4 X3 X2 X1 X0 6-bit binary value of 0 to 39	six bits of immediate data, bits X0 to X5 are transferred to the X-address pointer to define one of forty display RAM columns

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

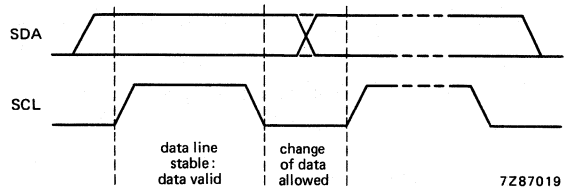


Fig.12 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

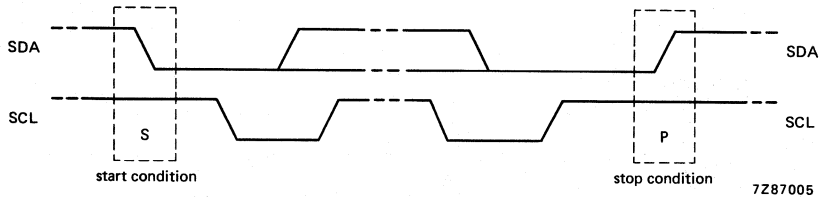


Fig.13 Definition of start and stop condition.

CHARACTERISTICS OF THE I²C-BUS (continued)

System configuration

A device transmitting a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message flow is the "master" and the devices which are controlled by the master are the "slaves".

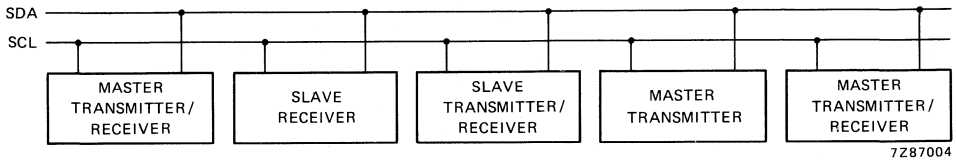


Fig.14 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal the end of a data transmission to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

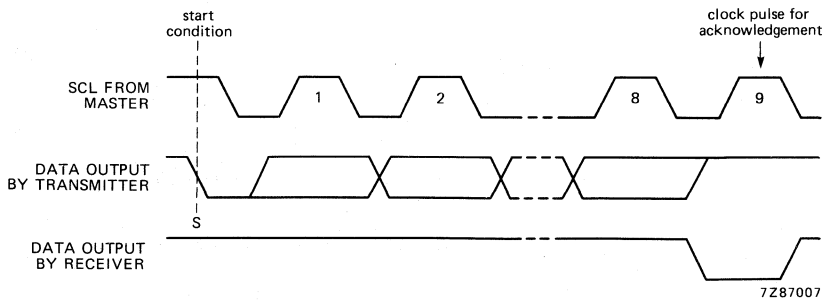


Fig.15 Acknowledgement on the I²C-bus.

Note

The general characteristics and detailed specification of the I²C-bus is available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	+8.0	V
LCD supply voltage range	V_{LCD}	V_{DD} −11	V_{DD}	V
Input voltage range at				
SDA, SCL, $\overline{SYNC}$, CLK, TEST, SA0, A0, A1, A2 and A3	V_{I1}	V_{SS} −0.5	V_{DD} + 0.5	V
V_3 to V_4	V_{I2}	V_{LCD} −0.5	V_{DD} + 0.5	V
Output voltage range at				
SDA	V_{O1}	V_{SS} −0.5	V_{DD} + 0.5	V
C0 to C39	V_{O2}	V_{LCD} −0.5	V_{DD} + 0.5	V
DC input current	I_I	−10	10	mA
DC output current	I_O	−10	10	mA
V_{DD}, V_{SS} or V_{LCD} current	I_{DD}, I_{SS}, I_{LCD}	−50	50	mA
Power dissipation per package	P_{tot}	−	400	mW
Power dissipation per output	P_o	−	100	mW
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DC CHARACTERISTICS

V_{DD} = 2.5 V to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
LCD supply voltage		V_{LCD}	V_{DD} −9	–	V_{DD} −3.5	V
Supply current	note 1; f_{CLK} = 2 kHz	I_{DD1}	–	9	20	μA
Power-on reset level	note 2	V_{POR}	–	1.3	1.8	V
Logic						
Input voltage LOW		V_{IL}	V_{SS}	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Leakage current at SDA, SCL, $\overline{SYNC}$, CLK, TEST, SA0, A0, A1, A2 and A3	V_I = V_{DD} or V_{SS}	I_{L1}	−1	–	1	μA
SDA output current LOW	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL}	3	–	–	mA
Input capacitance	note 3	C_I	–	–	5	pF
LCD outputs						
Leakage current at V_3 to V_4	V_I = V_{DD} or V_{LCD}	I_{L2}	−2	–	2	μA
DC component of LCD drivers C0 to C39		± V_{DC}	–	20	–	mV
Output resistance at C0 to C39	note 4	R_{COL}	–	3	6	kΩ

AC CHARACTERISTICS (note 5)

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Clock frequency	50% duty factor	f_{CLK}	–	*	10	kHz
Driver delays	$V_{DD} - V_{LCD}$ = 9 V; with test loads	t_{PLCD}	–	–	100	μs
I²C-bus						
SCL clock frequency		f_{SCL}	–	–	100	kHz
Tolerable spike width on bus		t_{SW}	–	–	100	ns
Bus free time		t_{BUF}	4.7	–	–	μs
Start condition set-up time	repeated start codes only	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time		$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time		t_{LOW}	4.7	–	–	μs
SCL HIGH time		t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time		t_r	–	–	1.0	μs
SCL and SDA fall time		t_f	–	–	0.3	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	0	–	–	ns
Stop condition set-up time		$t_{SU;STO}$	4.0	–	–	μs

* Typically 0.9 to 3.3 kHz.

Notes to the characteristics

1. Outputs are open; inputs at V_{DD} or V_{SS}; I^2C-bus inactive; clock with 50% duty factor.
2. Resets all logic when $V_{DD} < V_{POR}$.
3. Periodically sampled; not 100% tested.
4. Resistance measured between output terminal (C0 to C39) and bias input (V_3 to V_4, V_{DD} and V_{LCD}) when the specified current flows through one output under the following conditions (see Table 1):

   $V_{OP} = V_{DD} - V_{LCD} = 9$ V;

   $V_3 - V_{LCD} \geqslant 4.70$ V; $V_4 - V_{LCD} \leqslant 4.30$ V; $I_{LOAD} = 100\ \mu$A.
5. All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

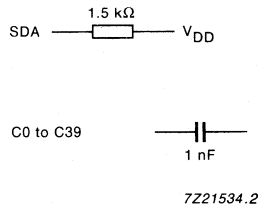


Fig.16 Test loads.

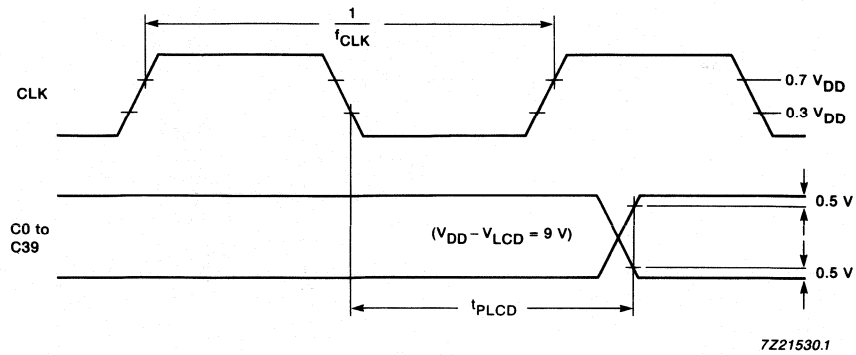


Fig.17 Driver timing waveforms.

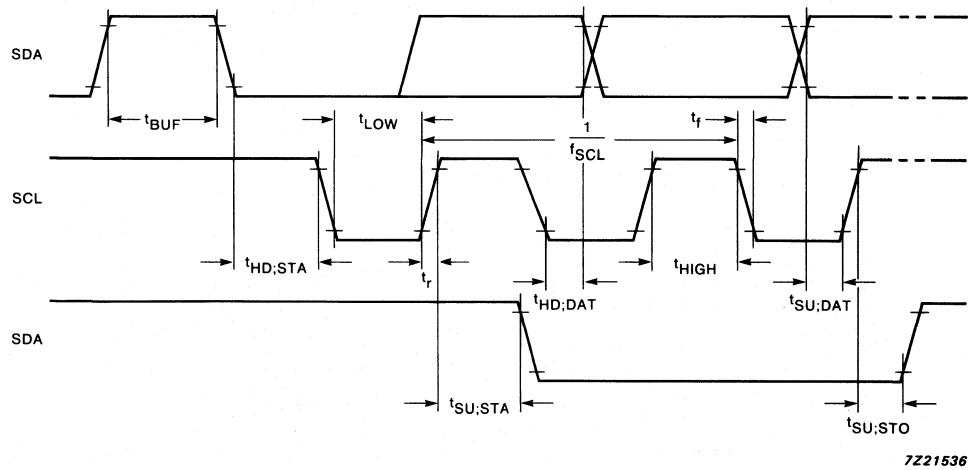


Fig.18 I^2C-bus timing waveforms.

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

APPLICATION INFORMATION

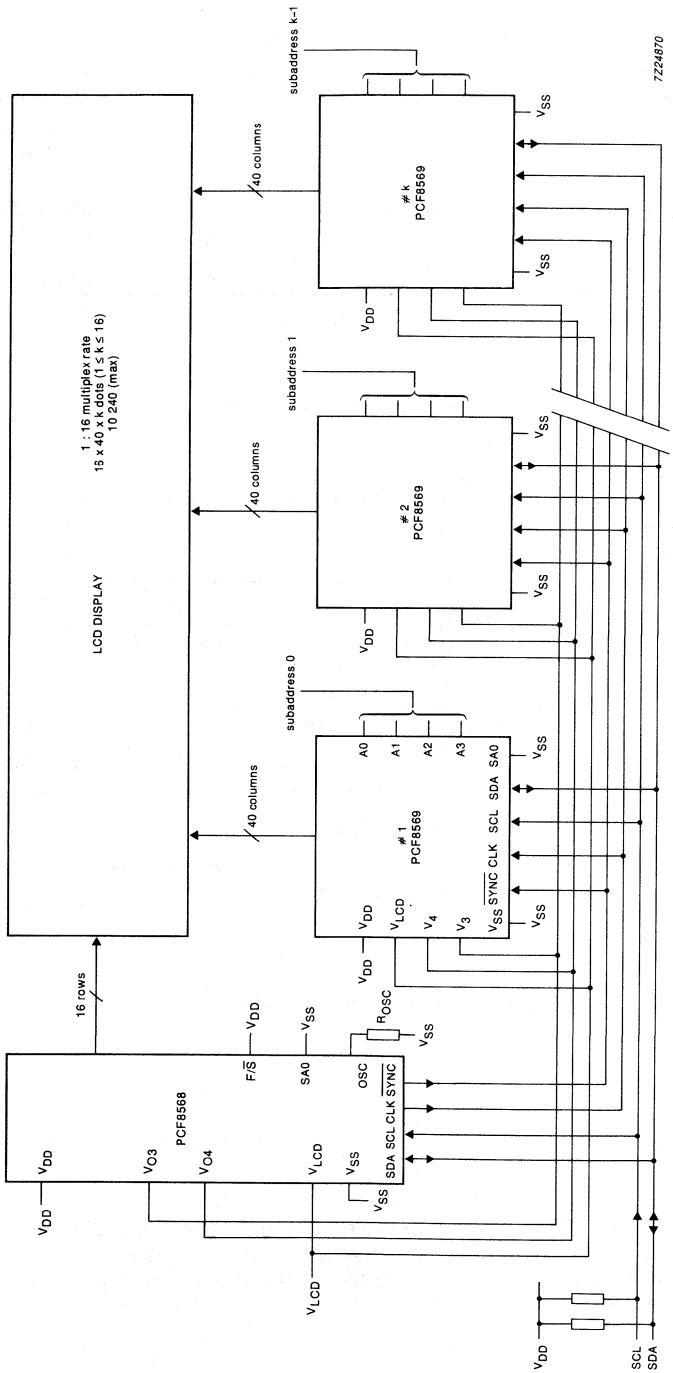


Fig.19 Typical LCD driver system with 1:16 multiplex rate.

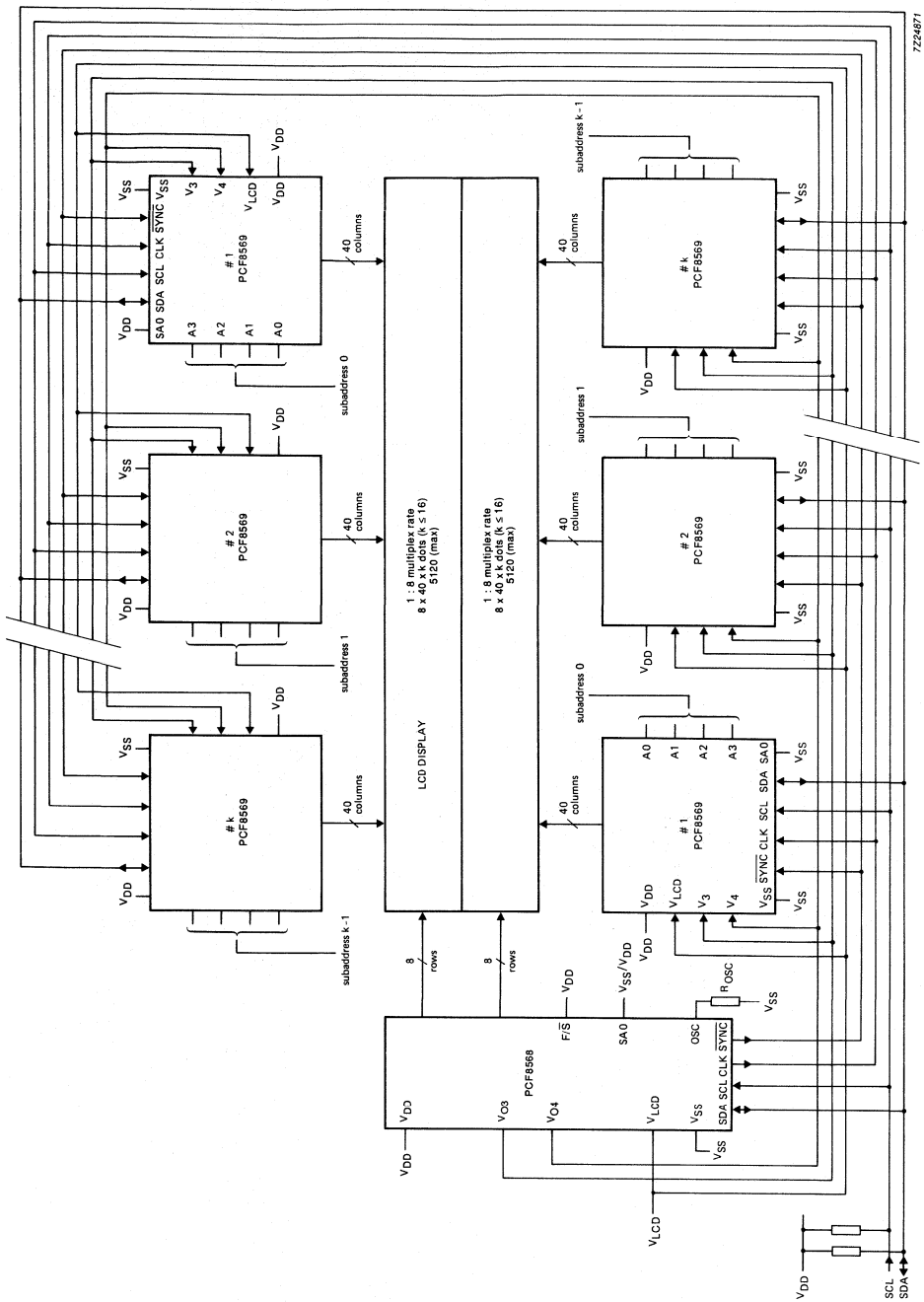


Fig.20 Split screen application with 1:8 multiplex rate for improved contrast.

APPLICATION INFORMATION (continued)

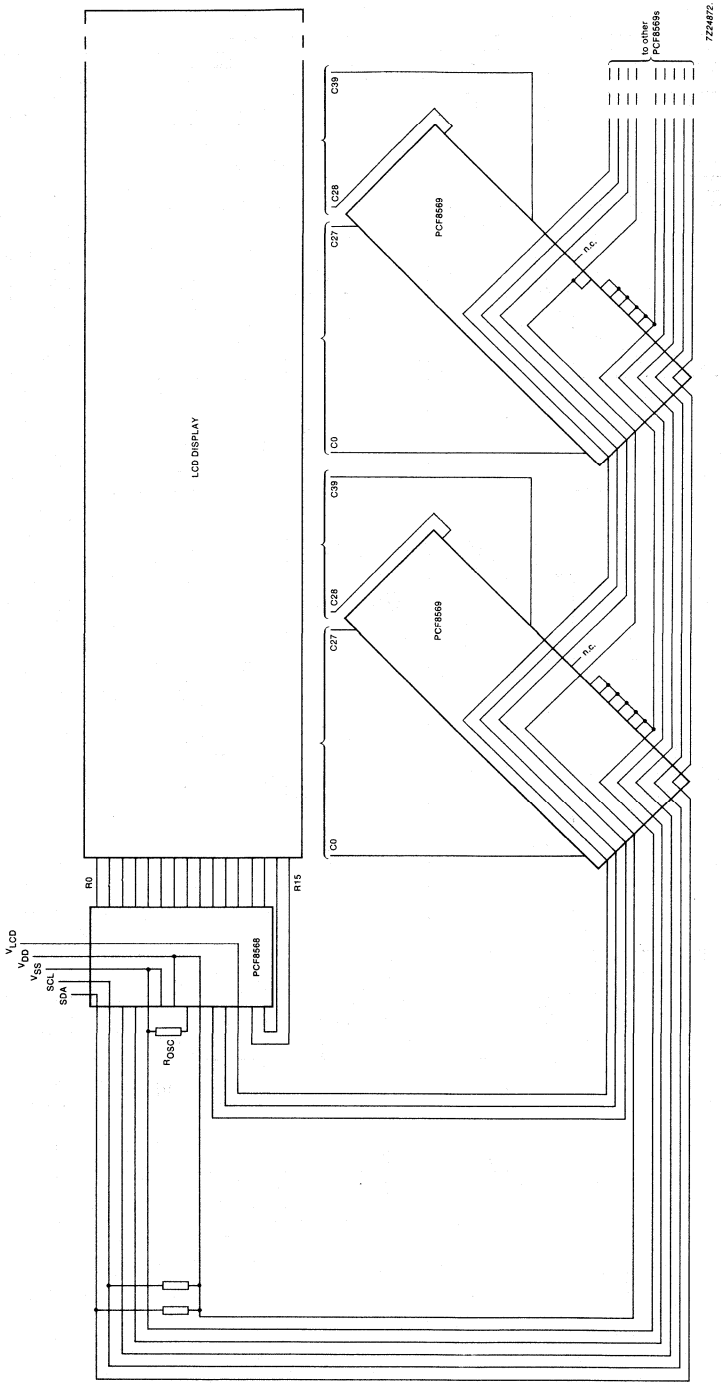


Fig.21 Example of single plane wiring, single screen with 1:16 multiplex rate.

256 × 8-bit static low-voltage RAM with I²C-bus interface

PCF8570

FEATURES

- Operating supply voltage 2.5 to 6.0 V
- Low data retention voltage; minimum 1.0 V
- Low standby current; maximum 15 μA
- Power saving mode; typical 50 nA
- Serial input/output bus (I²C-bus)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Available in DIP8 and SO8L packages.

APPLICATIONS

- Telephony:
  - RAM expansion for stored numbers in repertory dialling (e.g. PCD33XX applications)
- General purpose RAM for applications requiring extremely low current and low-voltage RAM retention (i.e. battery or capacitor backed)
- Radio, television and video cassette recorder:
  - channel presets
- General purpose:
  - RAM expansion for the microcontroller families PCD33XX, PCF84CXX, P80CLXXX and most other microcontrollers.

GENERAL DESCRIPTION

The PCF8570 is a low power static CMOS RAM.

The PCF8570 is organized as 256 words by 8-bits.

Addresses and data are transferred serially via a two-line bidirectional bus (I²C-bus). The built-in word address register is incremented automatically after each written or read data byte. Three address pins, A0, A1 and A2 are used to define the hardware address, allowing the use of up to 8 devices connected to the bus without additional hardware.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.5	6.0	
I_{DD}	supply current (standby)	f_{SCL} = 0 Hz	–	15	μA
I_{DDR}	supply current (power-saving mode)	T_{amb} = 25 °C	–	400	nA
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−65	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8570P	8	DIP8	plastic	SOT97-1
PCF8570T	8	SO8L	plastic	SOT176-1

256 × 8-bit static low-voltage RAM with I²C-bus interface

PCF8570

BLOCK DIAGRAM

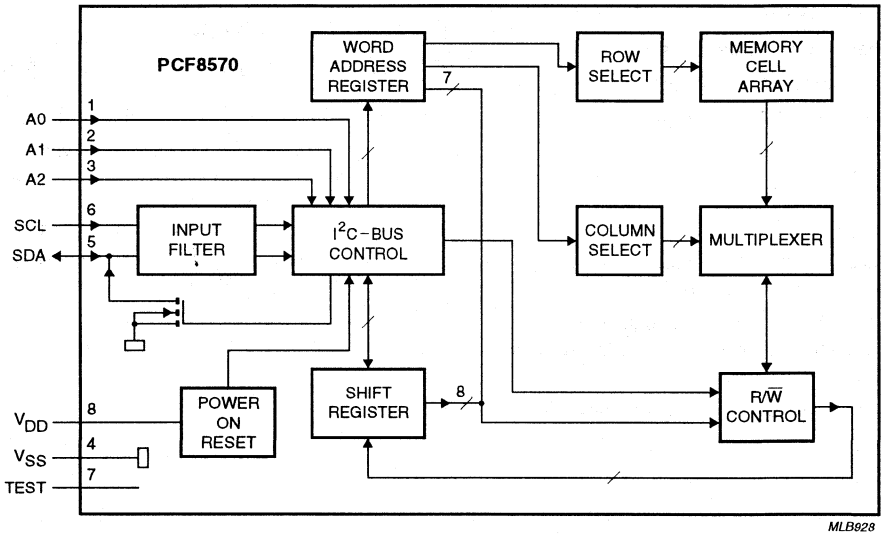


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	hardware address input 0
A1	2	hardware address input 1
A2	3	hardware address input 2
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
TEST	7	test output for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Figs 13 and 14)
V_{DD}	8	positive supply

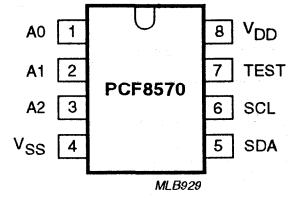


Fig.2 Pin configuration.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

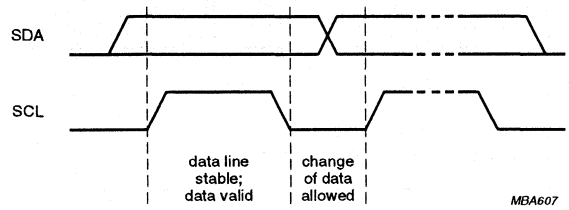


Fig.3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

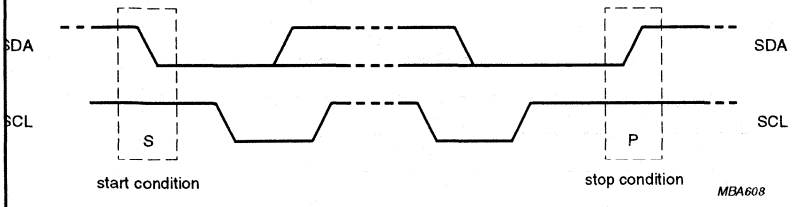


Fig.4 Definition of start and stop conditions.

System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

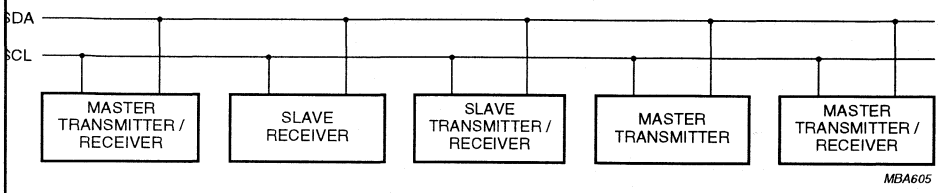


Fig.5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

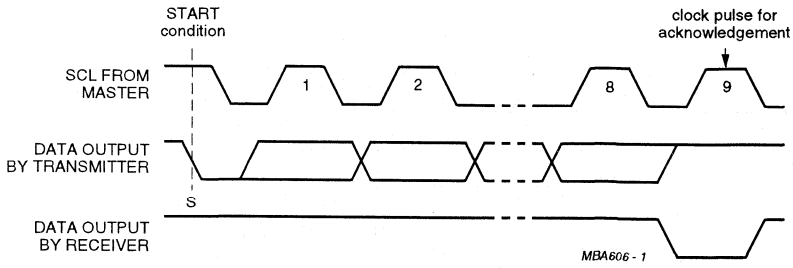


Fig.6 Acknowledgement on the I²C-bus.

I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF8570 WRITE and READ cycles is shown in Figs 7, 8 and 9.

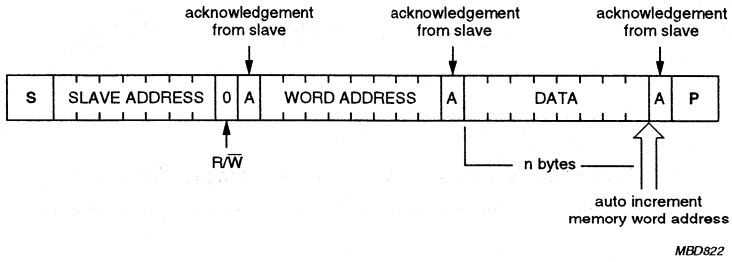


Fig.7 Master transmits to slave receiver (WRITE) mode.

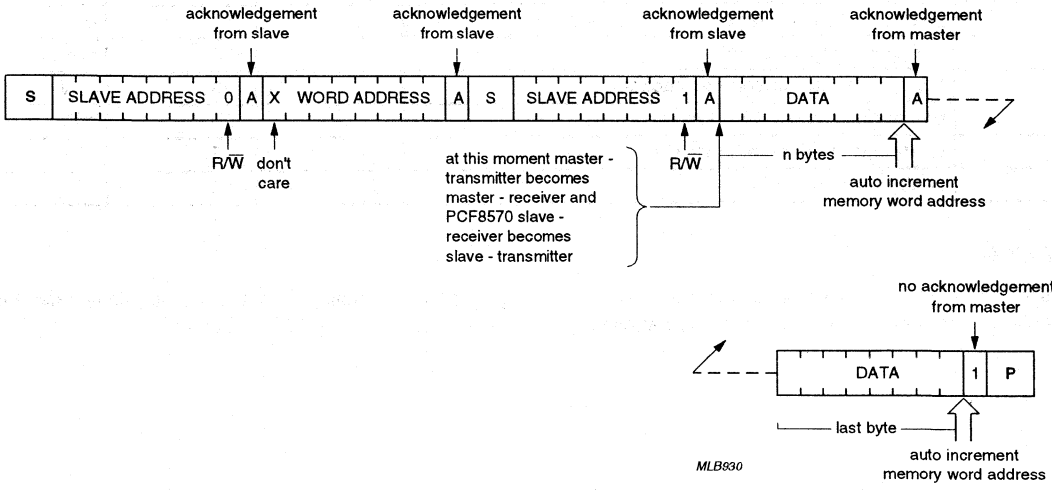


Fig.8 Master reads after setting word address (WRITE word address; READ data).

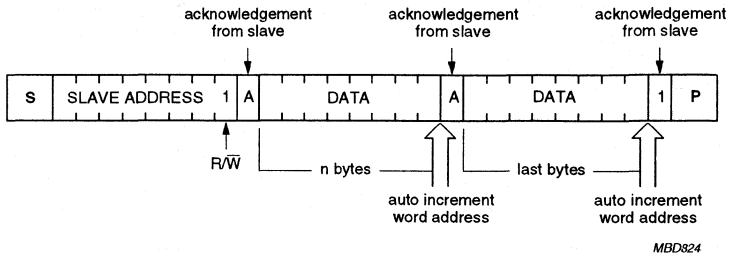


Fig.9 Master reads slave immediately after first byte (READ mode).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pin 8)	−0.8	+8.0	V
V_I	input voltage (any input)	−0.8	V_{DD} + 0.8	V
I_I	DC input current	–	±10	mA
I_O	DC output current	–	±10	mA
I_{DD}	positive supply current	–	±50	mA
I_{SS}	negative supply current	–	±50	mA
P_{tot}	total power dissipation per package	–	300	mW
P_O	power dissipation per output	–	50	mW
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

DC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.5	–	6.0	V
I_{DD}	supply current					
	standby mode	$V_I = V_{DD}$ or V_{SS}; f_{SCL} = 0 Hz; T_{amb} = −25 to +70 °C	–	–	5	μA
	operating mode	$V_I = V_{DD}$ or V_{SS}; f_{SCL} = 100 Hz	–	–	200	μA
V_{POR}	power-on reset voltage	note 1	1.5	1.9	2.3	V
Inputs, input/output SDA						
V_{IL}	LOW level input voltage	note 2	−0.8	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	note 2	$0.7V_{DD}$	–	V_{DD} + 0.8	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	–	–	mA
$\|I_{LI}\|$	input leakage current	$V_I = V_{DD}$ or V_{SS}	–	–	1	μA
Inputs A0, A1, A2 and TEST						
$\|I_{LI}\|$	input leakage current	$V_I = V_{DD}$ or V_{SS}	–	–	±250	nA
Inputs SCL and SDA						
C_I	input capacitance	$V_I = V_{SS}$	–	–	7	pF
Low V_{DD} data retention						
V_{DDR}	supply voltage for data retention		1	–	6	V
I_{DDR}	supply current	V_{DDR} = 1 V	–	–	5	μA
		V_{DDR} = 1 V; T_{amb} = −25 to +70 °C	–	–	2	μA
Power saving mode (see Figs 13 and 14)						
I_{DDR}	supply current	TEST = V_{DD}; T_{amb} = 25 °C	–	50	400	nA
t_{HD2}	recovery time		–	50	–	μs

Notes

1. The power-on reset circuit resets the I²C-bus logic when $V_{DD} < V_{POR}$. The status of the device after a power-on reset condition can be tested by sending the slave address and testing the acknowledge bit.
2. If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed ±0.5 mA.

AC CHARACTERISTICS

All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
I²C-bus timing (see Fig.10; note 1)					
f_{SCL}	SCL clock frequency	–	–	100	kHz
t_{SP}	tolerable spike width on bus	–	–	100	ns
t_{BUF}	bus free time	4.7	–	–	µs
$t_{SU;STA}$	start condition set-up time	4.7	–	–	µs
$t_{HD;STA}$	start condition hold time	4.0	–	–	µs
t_{LOW}	SCL LOW time	4.7	–	–	µs
t_{HIGH}	SCL HIGH time	4.0	–	–	µs
t_r	SCL and SDA rise time	–	–	1.0	µs
t_f	SCL and SDA fall time	–	–	0.3	µs
$t_{SU;DAT}$	data set-up time	250	–	–	ns
$t_{HD;DAT}$	data hold time	0	–	–	ns
$t_{VD;DAT}$	SCL LOW-to-data out valid	–	–	3.4	µs
$t_{SU;STO}$	stop condition set-up time	4.0	–	–	µs

Note

1. A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

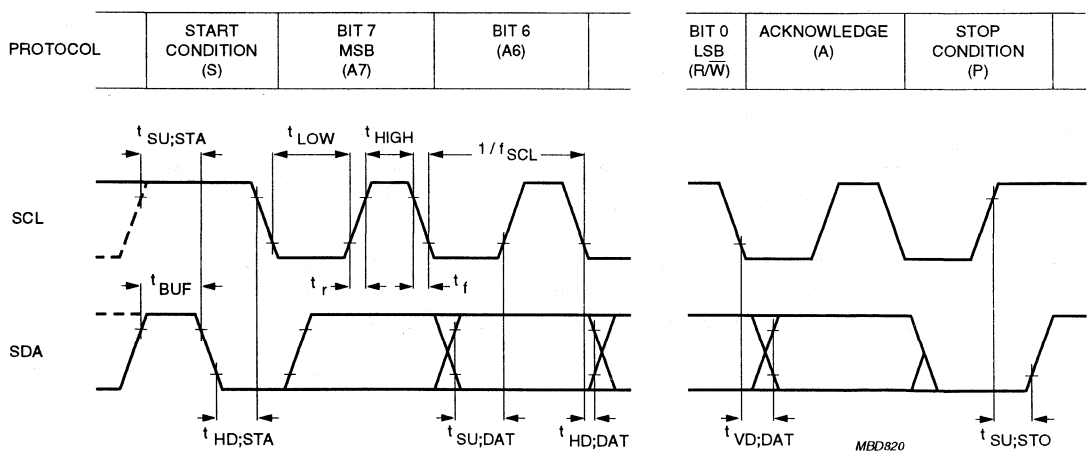


Fig.10 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

APPLICATION INFORMATION

Slave address

The PCF8570 has a fixed combination 1 0 1 0 as group 1, while group 2 is fully programmable (see Fig.11).

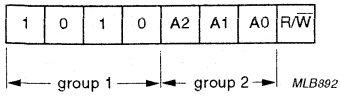
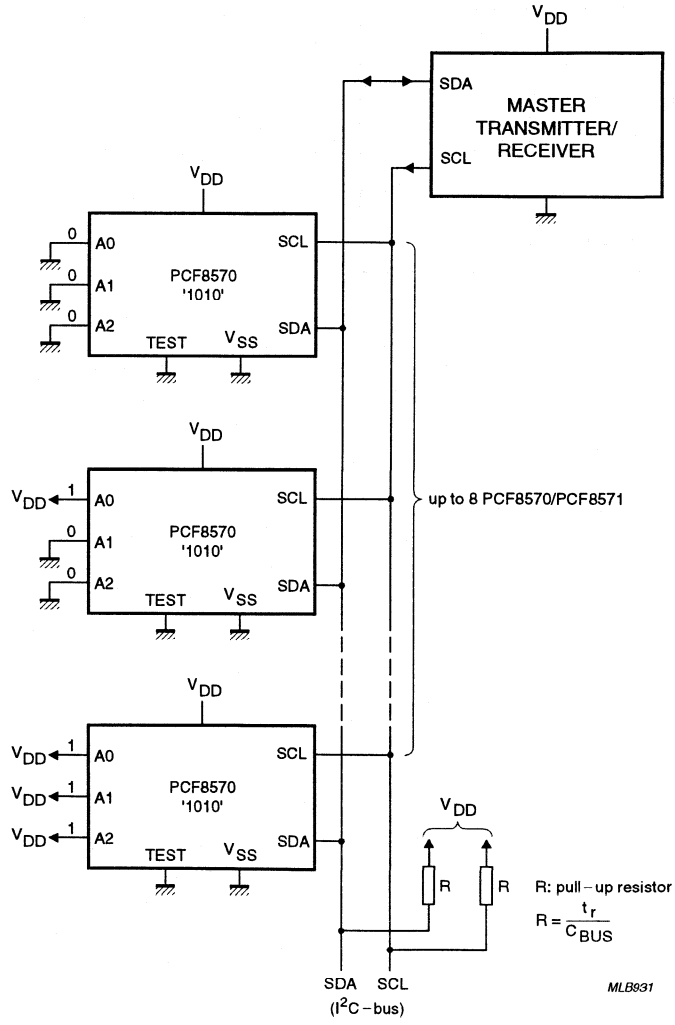


Fig.11 Slave address.

Application example

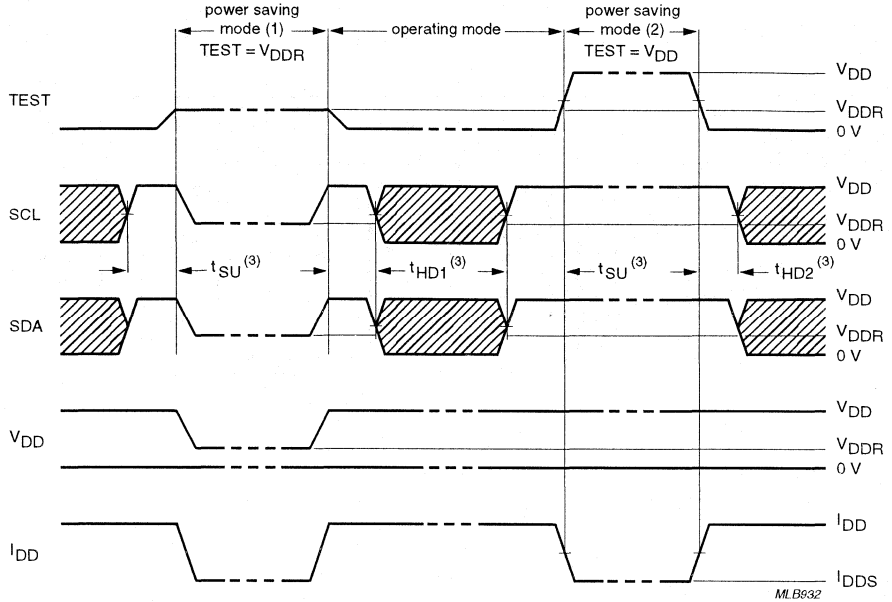


It is recommended that a 4.7 µF/10 V solid aluminium capacitor (SAL) be connected between V_{DD} and V_{SS}.

Fig.12 Application diagram.

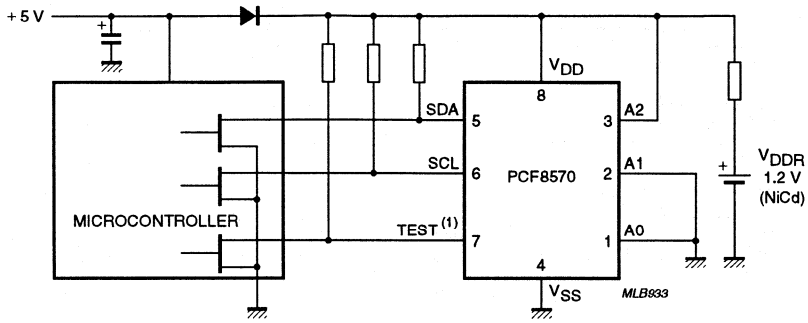
Power saving mode

With the condition TEST = V_{DD} or V_{DDR} the PCF8570 goes into the power saving mode and I²C-bus logic is reset.



(1) Power saving mode without 5 V supply voltage.
(2) Power saving mode with 5 V supply voltage.
(3) t_{SU} and $t_{HD1} \geq 4$ µs and $t_{HD2} \geq 50$ µs.

Fig.13 Timing for power saving mode.



It is recommended that a 4.7 µF/10 V solid aluminium capacitor (SAL) be connected between V_{DD} and V_{SS}.

(1) In the operating mode TEST = 0 V; in the power saving mode TEST = V_{DDR}.

Fig.14 Application example for power saving mode.

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCF8573 is a low threshold, CMOS circuit that functions as a real time clock/calendar with an I^2C-bus interface.
The IC incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred via a serial two-line bidirectional bus (I^2C). Back-up for the clock during supply interruptions is provided by a 1.2 V nickel cadium battery. The time base is generated from a 32.768 kHz crystal-controlled oscillator.

Features

- Serial input/output I^2C-bus interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32.768 kHz)

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range					
clock (pin 16 to pin 15)	$V_{DD}-V_{SS1}$	1.1	–	6.0	V
I^2C interface (pin 16 to pin 8)	$V_{DD}-V_{SS2}$	2.5	–	6.0	V
Crystal oscillator frequency	f_{osc}	–	32.768	–	kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT38).
PCF8573T: 16-lead mini-pack; plastic (SO16L; SOT162A).

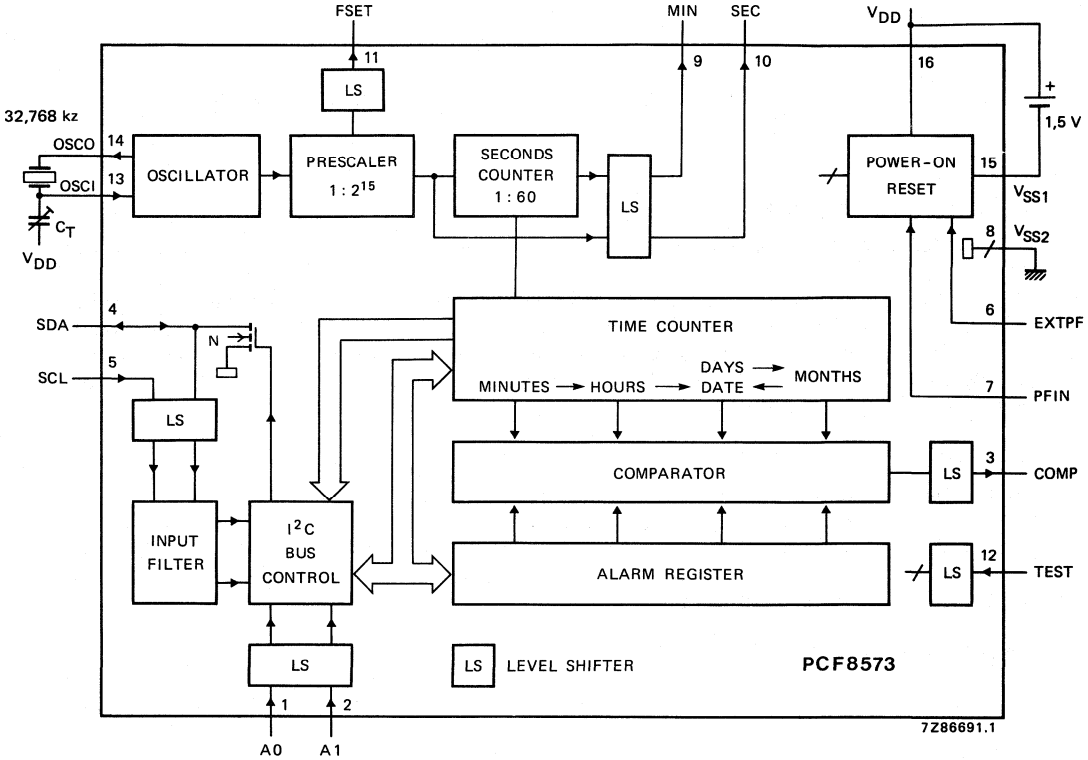


Fig.1 Block diagram.

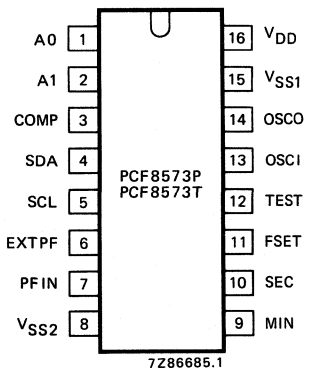


Fig.2 Pinning diagram.

PINNING

1	A0	address input	
2	A1	address input	
3	COMP	comparator output	
4	SDA	serial data line	I^2C-bus
5	SCL	serial clock line	I^2C-bus
6	EXTPF	enable power fail flag input	
7	PFIN	power fail flag input	
8	V_{SS2}	negative supply 2 (I^2C interface)	
9	MIN	one pulse per minute output	
10	SEC	one pulse per second output	
11	FSET	oscillator tuning output	
12	TEST	test input; must be connected to V_{SS2} when not in use	
13	OSCI	oscillator input	
14	OSCO	oscillator input/output	
15	V_{SS1}	negative supply 1 (clock)	
16	V_{DD}	common positive supply	

FUNCTIONAL DESCRIPTION

Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32.768 kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I²C-bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH-to-LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

Table 1 Cycle length of the time counter

unit	number of bits	counting cycle	carry for following unit	content of month counter
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days	6	01 to 28	28 → 01	2 (note 1)
			or 29 → 01	2 (note 1)
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note to Table 1

1. Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I²C-bus.

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I²C-bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I²C-bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I²C-bus.

FUNCTIONAL DESCRIPTION (continued)

Power on/power fail detection

If the voltage $V_{DD}-V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal for application with ($V_{DD}-V_{SS1}$) greater than V_{TH1}, or by an externally generated power fail signal for application with ($V_{DD}-V_{SS1}$) less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internally or externally controlled POWF can be selected by input EXTPF as shown in Table 2.

Table 2 Power fail selection

EXTPF	PFIN	function
0	0	power fail is sensed internally
0	1	test mode
1	0	power fail is sensed externally
1	1	no power fail sensed

0 : connected to V_{SS1} (LOW)
1 : connected to V_{DD} (HIGH)

The external power fail control operates by absence of the $V_{DD}-V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of $V_{DD}-V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C-bus. A power on reset for the I^2C-bus control is generated on-chip when the supply voltage $V_{DD}-V_{SS2}$ is less than V_{TH2}.

Interface level shifters

The level shifters adjust the 5 V operating voltage ($V_{DD}-V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD}-V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD}-V_{SS2}$ supply voltage. If the voltage $V_{DD}-V_{SS2}$ is absent ($V_{DD} = V_{SS2}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD}-V_{SS2}$ and the $V_{DD}-V_{SS1}$ supplies. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD}-V_{SS2} = 0$.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer (see Fig.3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

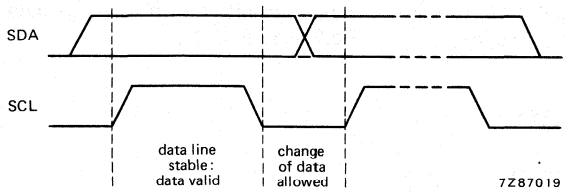


Fig.3 Bit transfer.

Start and stop conditions (see Fig. 4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

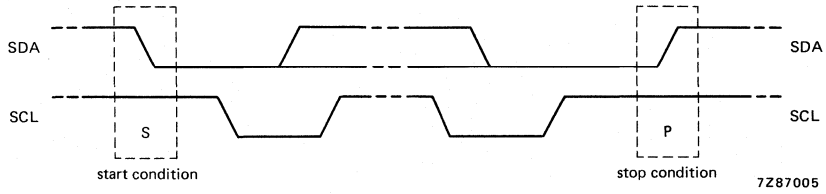


Fig.4 Definition of start and stop conditions.

System configuration (see Fig.5)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

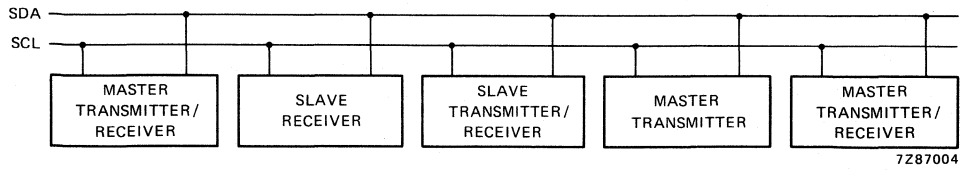


Fig.5 System configuration.

CHARACTERISTICS OF THE I²C-bus (continued)

Acknowledge (see Fig.6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition. (See Fig.10 and Fig.11).

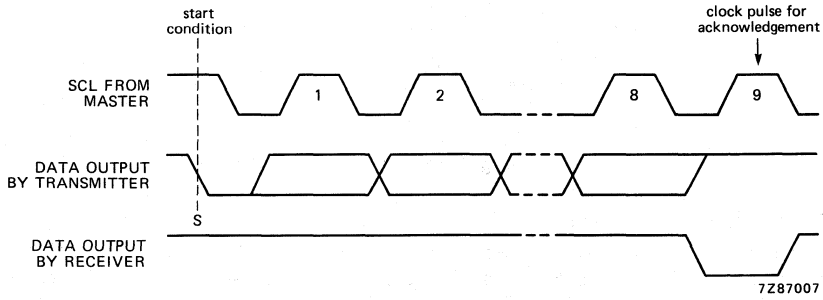


Fig.6 Acknowledgement on the I²C-bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

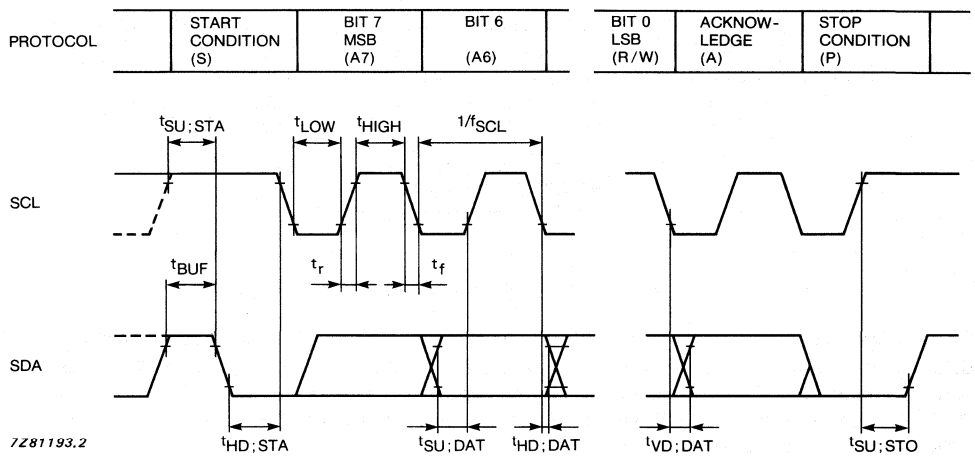


Fig.7 I^2C-bus timing diagram.

ADDRESSING

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Fig.8.

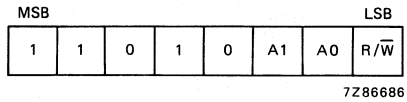


Fig.8 Slave address.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device to have 1 of 4 different addresses.

Clock/calendar READ/WRITE cycles

The I²C-bus configuration for different clock/calendar READ and WRITE cycles is shown in Figs 9, 10 and 11.

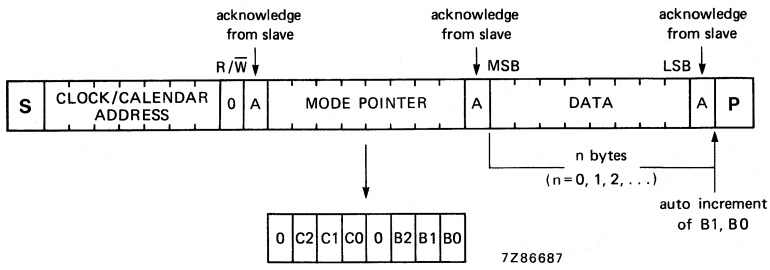


Fig.9 Master transmitter transmits to clock/calendar slave receiver.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nible is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

Table 3 CONTROL-nibble

	C2	C1	C0	function
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (see note)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. −30 s. From the count 30 there is a carry which adjusts the time by max. + 30 s.

Table 4 ADDRESS-nibble

	B2	B1	B0	addressed to:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 5 Placement of BCD digits in the DATA byte

MSB				DATA			LSB	
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to:
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Where:

"X" is the don't care bit
"D" is the data bit
Acknowledgement response of the clock calendar as slave receiver is shown in Table 6.

ADDRESSING (continued)

Table 6 Slave receiver acknowledgement

mode pointer								acknowledge on byte		
								address	mode pointer	data
	C2	C1	C0		B2	B1	B0			
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Where:

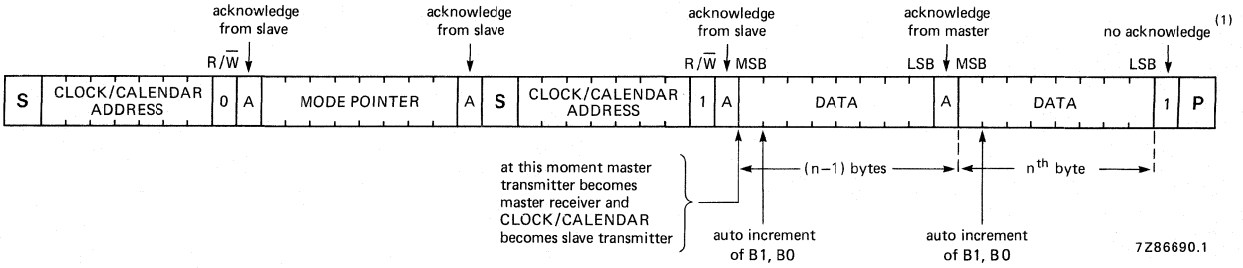
"X" is the don't care bit.

Table 7 Organization of the BCD digits in the DATA byte

MSB DATA LSB								
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to
0	0	D	D	D	D	D	D	hours
0	D	D	D	D	D	D	D	minutes
0	0	D	D	D	D	D	D	days
0	0	0	D	D	D	D	D	months
0	0	0	*	**	NODA	COMP	POWF	control/status flags

Where:

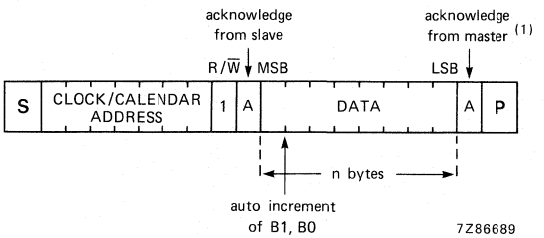
"D" is the data bit
* = minutes
** = seconds.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig.10 Master transmitter reads clock/calendar after setting mode pointer.

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig.11 Master reads clock/calendar immediately after first byte.

The status of the MODE-POINTER-WORD concerning the CONTROL-nibble remains unchanged until a write to MODE POINTER condition occurs.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	condition	symbol	min.	max.	unit
Supply voltage range					
pin 16 to pin 15		$V_{DD}-V_{SS1}$	−0.3	8.0	V
pin 16 to pin 8		$V_{DD}-V_{SS2}$	−0.3	8.0	V
Voltage input					
pins 4 and 5	note 1	V_I	$V_{SS2}-0.8$	$V_{DD}+0.8$	V
pins 6, 7, 13 and 14		V_I	$V_{SS1}-0.6$	$V_{DD}+0.6$	V
any other pin		V_I	$V_{SS2}-0.6$	$V_{DD}+0.6$	V
Input current		I_I	−	10	mA
Output current		I_O	−	10	mA
Power dissipation per output		P_O	−	100	mW
Total power dissipation		P_{tot}	−	200	mW
Operating ambient temperature range		T_{amb}	−40	+85	°C
Storage temperature range		T_{stg}	−55	+125	°C

Note to the Ratings

1. With input impedance of minimum 500 Ω.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified. Typical values at T_{amb} = +25 °C

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage						
I^2C interface		$V_{DD}-V_{SS2}$	2.5	5.0	6.0	V
clock	$t_{HD;DAT} \geqslant$ 300 ns	$V_{DD}-V_{SS1}$	1.1	1.5	$V_{DD}-V_{SS2}$	V
Supply current						
V_{SS1} (pin 15)	$V_{DD}-V_{SS1}$ = 1.5 V	$-I_{SS1}$	–	3	10	μA
	$V_{DD}-V_{SS1}$ = 5 V	$-I_{SS1}$	–	12	50	μA
V_{SS2} (pin 8)	$V_{DD}-V_{SS2}$ = 5 V; I_O = 0 all outputs	$-I_{SS2}$	–	–	50	μA
Input SCL; input/output SDA						
Input voltage LOW		V_{IL}	–	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Leakage current	$V_I = V_{SS2}$ or V_{DD}	$\|I_L\|$	–	–	1	μA
Input capacitance		C_I	–	–	7	pF
Inputs A0, A1, TEST						
Input voltage LOW		V_{IL}	–	–	0.2 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Input leakage current	$V_I = V_{SS2}$ or V_{DD}	$\pm I_{LI}$	–	–	250	nA
Inputs EXTPF, PFIN						
Input voltage LOW		V_{IL}	0	–	0.2 $V_{DD}-V_{SS1}$	V
Input voltage HIGH		V_{IH}	0.7 $V_{DD}-V_{SS1}$	–	–	V
Input leakage current	$V_I = V_{SS1}$ to V_{DD}	$\pm I_{LI}$	–	–	1.0	μA
	T_{amb} = 25 °C; $V_I = V_{SS1}$ to V_{DD}	$\pm I_{LI}$	–	–	0.1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output SDA						
(n channel open drain)						
Output "ON"	I_O = 3 mA; $V_{DD}-V_{SS2}$ = 2.5 to to 6 V	V_{OL}	–	–	0.4	V
Leakage current	$V_{DD}-V_{SS2}$ = 6 V; V_O = 6 V	$\|I_L\|$	–	–	1	μA
Outputs						
Outputs SEC, MIN, COMP, FSET (normal buffer outputs)						
Output voltage LOW	$V_{DD}-V_{SS2}$ = 2.5 V; I_O = 0.3 mA	V_{OL}	–	–	0.4	V
	$V_{DD}-V_{SS2}$ = 4 to 6 V; I_O = 1.6 mA	V_{OL}	–	–	0.4	V
Output voltage HIGH	$V_{DD}-V_{SS2}$ = 2.5 V; $-I_O$ = 0.1 mA	V_{OH}	$V_{DD}-0.4$	–	–	V
	$V_{DD}-V_{SS2}$ = 4 to 6 V; $-I_O$ = 0.5 mA	V_{OH}	$V_{DD}-0.4$	–	–	V
Internal threshold voltage						
Power failure detection		V_{TH1}	1	1.2	1.4	V
Power "ON" reset		V_{TH2}	1.5	2.0	2.5	V
Rise and fall times of input signals						
Input EXTPF		t_r, t_f	–	–	1	μs
Input PFIN		t_r, t_f	–	–	∞	μs
Input signals except EXTPF and PFIN between V_{IL} and V_{IH} levels						
rise time		t_r	–	–	1	μs
fall time		t_f	–	–	0.3	μs

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Integrated oscillator capacitance		C_{OUT}	–	40	–	pF
Oscillator feedback resistance		R_f	–	3	–	MΩ
Oscillator stability	$\Delta(V_{DD}-V_{SS1})$ = 100 mV; at $V_{DD}-V_{SS1}$ = 1.55 V; T_{amb} = 25 °C	f/f_{osc}	–	2×10^{-7}	–	–
Quartz crystal parameters	f = 32.768 kHz					
Series resistance		R_S	–	–	40	kΩ
Parallel capacitance		C_L	–	10	–	pF
Trimmer capacitance		C_T	5	–	25	pF

APPLICATION INFORMATION

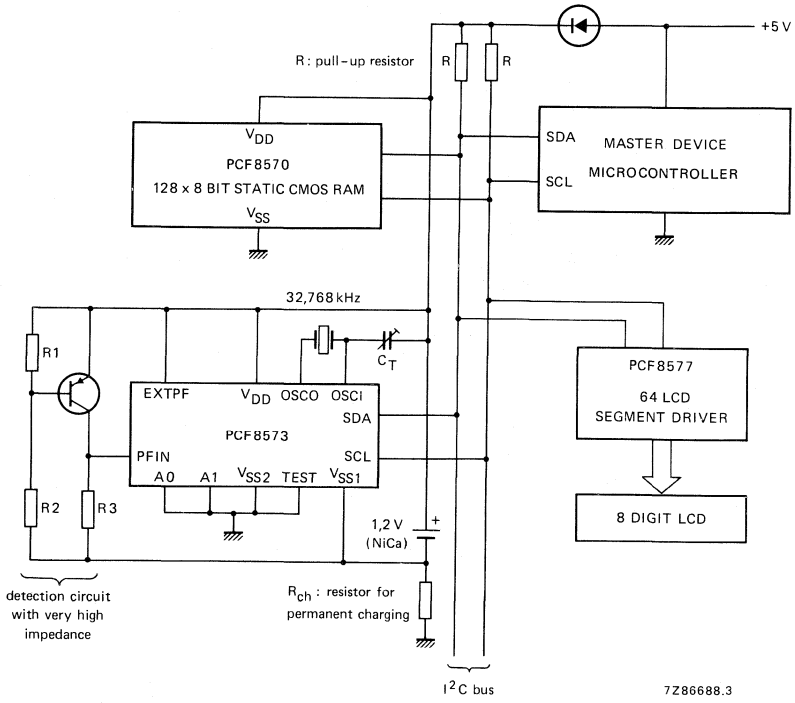


Fig.12 Application example of the PCF8573 clock/calendar.

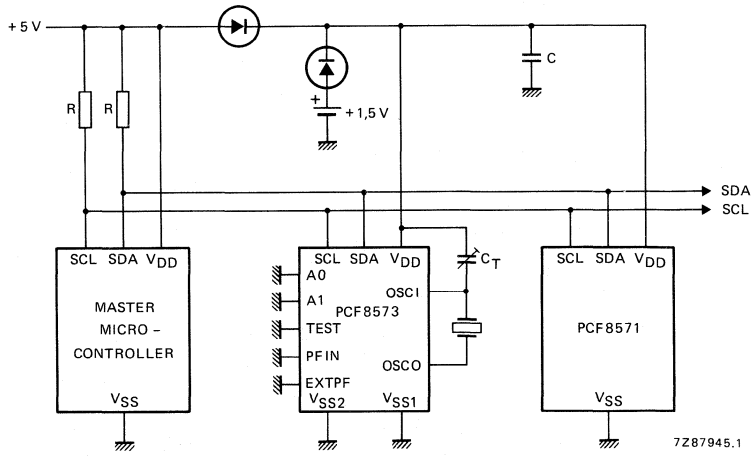


Fig.13 Application example of the PCF8573 with common V_{SS1} and V_{SS2} supply.

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Integrated oscillator capacitance		C_{OUT}	–	40	–	pF
Oscillator feedback resistance		R_f	–	3	–	MΩ
Oscillator stability	$\Delta(V_{DD}-V_{SS1})$ = 100 mV; at $V_{DD}-V_{SS1}$ = 1.55 V; T_{amb} = 25 °C	f/f_{osc}	–	2×10^{-7}	–	–
Quartz crystal parameters	f = 32.768 kHz					
Series resistance		R_S	–	–	40	kΩ
Parallel capacitance		C_L	–	10	–	pF
Trimmer capacitance		C_T	5	–	25	pF

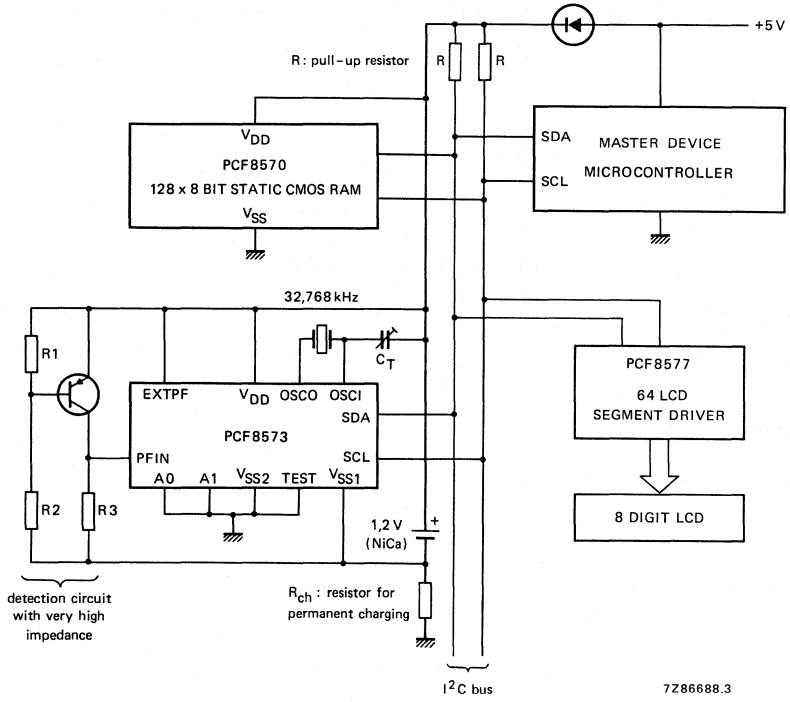


Fig.12 Application example of the PCF8573 clock/calendar.

APPLICATION INFORMATION

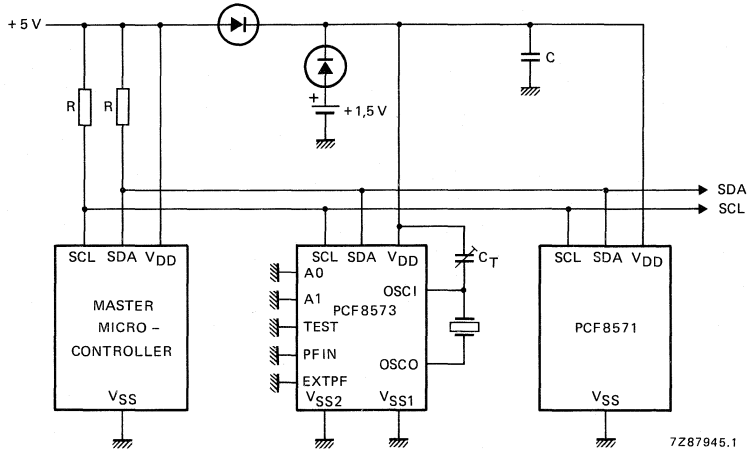


Fig.13 Application example of the PCF8573 with common V_{SS1} and V_{SS2} supply.

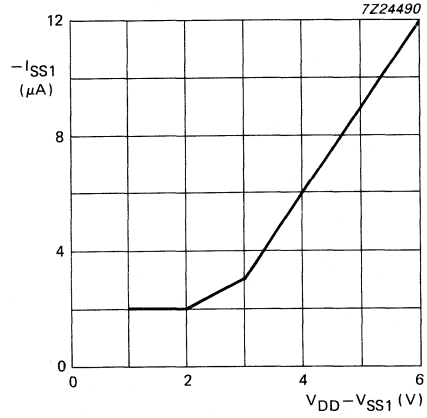


Fig.14 Typical supply current ($-I_{SS1}$) as a function of clock supply voltage ($V_{DD}-V_{SS1}$) at $T_{amb} = -40$ to $+85$ °C.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

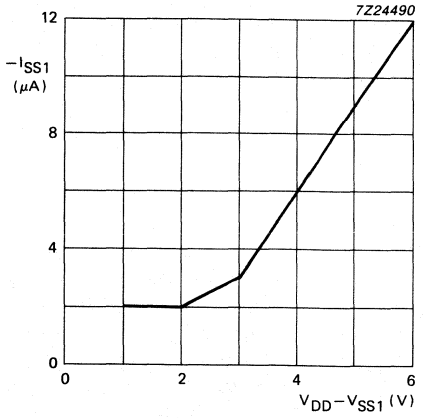


Fig. 14 Typical supply current ($-I_{SS1}$) as a function of clock supply voltage ($V_{DD}-V_{SS1}$) at $T_{amb} = -40$ to $+85$ °C.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Remote 8-bit I/O expander for I²C-bus PCF8574

FEATURES

- Operating supply voltage 2.5 to 6 V
- Low standby current consumption of 10 μA maximum
- I²C to parallel port expander
- Open-drain interrupt output
- 8-bit remote I/O Port for the I²C-bus
- Compatible with most microcontrollers
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)
- DIP16, space-saving SO16 or SSOP20 package.

GENERAL DESCRIPTION

The PCF8574 is a silicon CMOS circuit. It provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I²C).

The device consists of an 8-bit quasi-bidirectional Port and an I²C interface. The PCF8574 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line ($\overline{INT}$) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and PCF8574A versions differ only in their slave address as shown in Fig.9.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8574P; PCF8574AP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
PCF8574T; PCF8574AT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCF8574TS	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

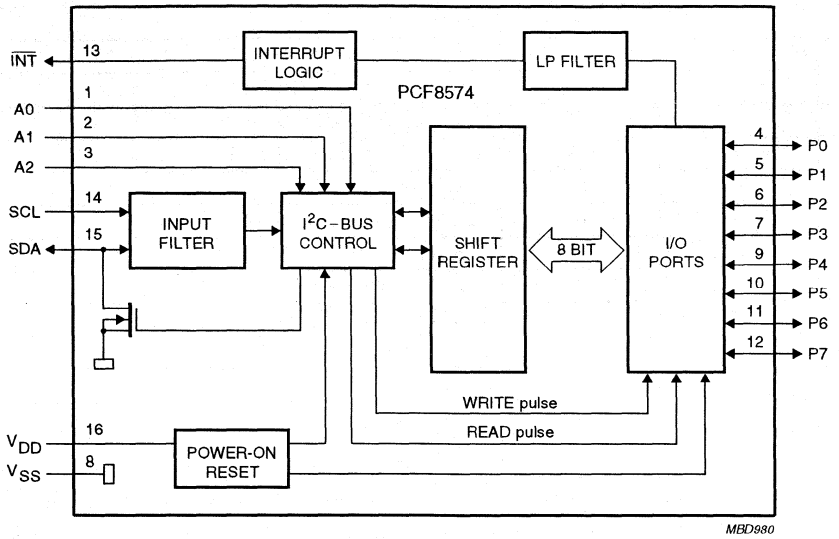


Fig.1 Block diagram (SOT38-1 and SOT162-1).

PINNING

SYMBOL	PIN		DESCRIPTION
	DIP16; SO16	SSOP20	
A0	1	6	address input 0
A1	2	7	address input 1
A2	3	9	address input 2
P0	4	10	quasi-bidirectional I/O Port 0
P1	5	11	quasi-bidirectional I/O Port 1
P2	6	12	quasi-bidirectional I/O Port 2
P3	7	14	quasi-bidirectional I/O Port 3
V_{SS}	8	15	supply ground
P4	9	16	quasi-bidirectional I/O Port 4
P5	10	17	quasi-bidirectional I/O Port 5
P6	11	19	quasi-bidirectional I/O Port 6
P7	12	20	quasi-bidirectional I/O Port 7
$\overline{INT}$	13	1	interrupt output (active LOW)
SCL	14	2	serial clock line
SDA	15	4	serial data line
V_{DD}	16	5	supply voltage
n.c.	–	3	not connected
n.c.	–	8	not connected
n.c.	–	13	not connected
n.c.	–	18	not connected

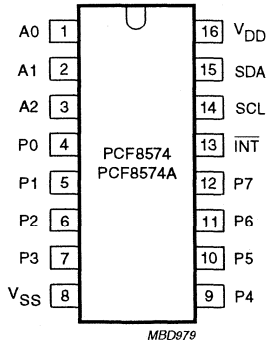


Fig.2 Pin configuration (DIP16; SO16).

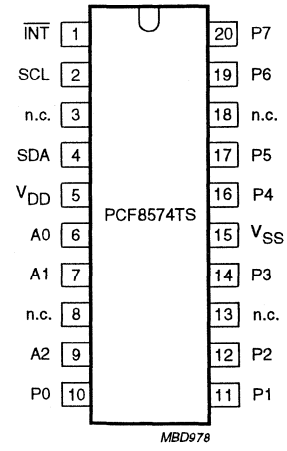


Fig.3 Pin configuration (SSOP20).

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Fig.4).

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S).
A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Fig.5).

System configuration

A device generating a message is a 'transmitter', a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Fig.6).

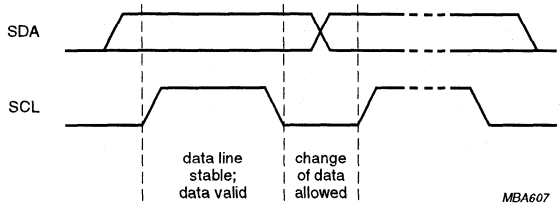


Fig.4 Bit transfer.

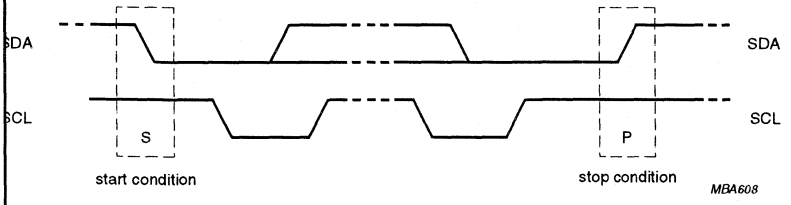


Fig.5 Definition of start and stop conditions.

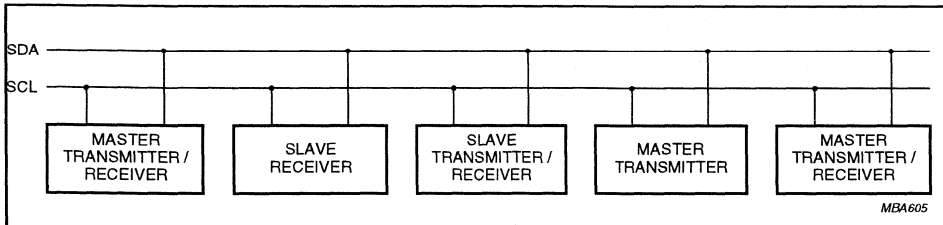


Fig.6 System configuration.

Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

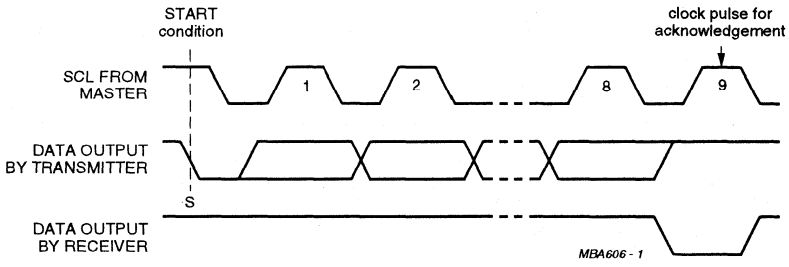


Fig.7 Acknowledgement on the I²C-bus.

FUNCTIONAL DESCRIPTION

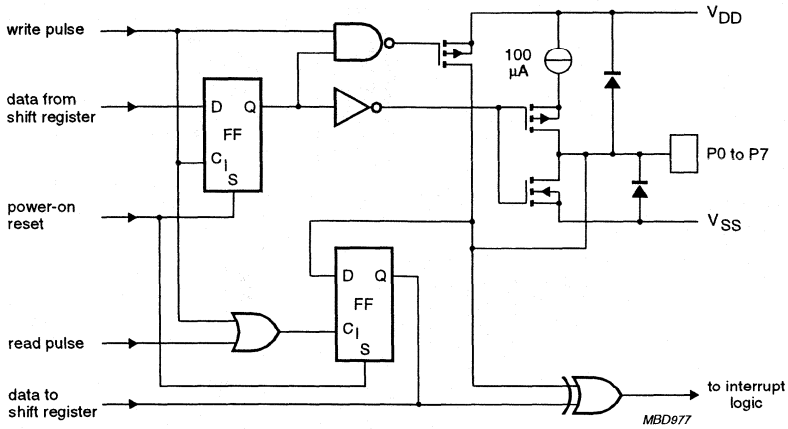
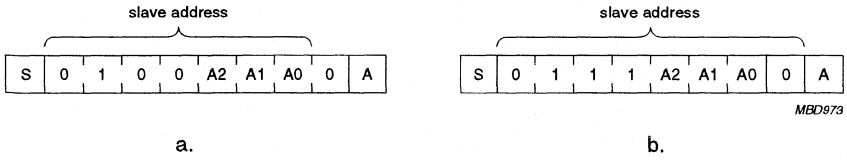


Fig.8 Simplified schematic diagram of each Port.

Addressing

For addressing see Figs 9, 10 and 11.



(a) PCF8574.
(b) PCF8574A.

Fig.9 PCF8574 and PCF8574A slave addresses.

Each bit of the PCF8574 I/O Port can be independently used as an input or output. Input data is transferred from the Port to the microcontroller by the READ mode (see Fig.11). Output data is transmitted to the Port by the WRITE mode (see Fig.10).

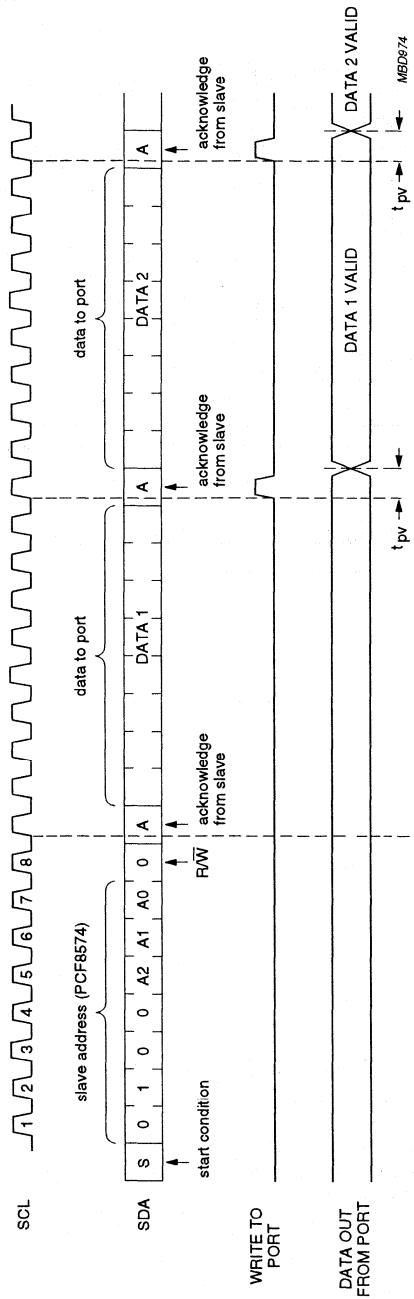
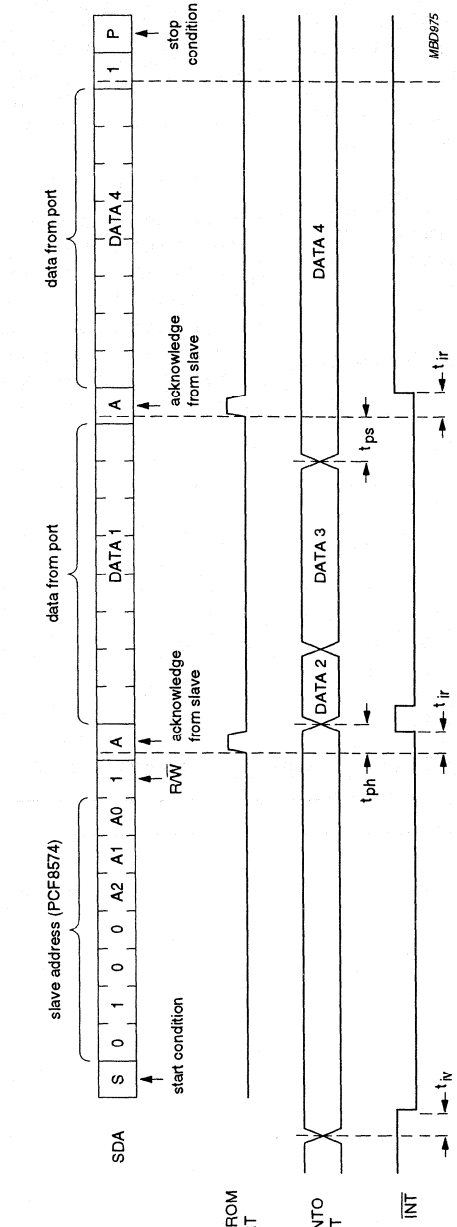


Fig.10 WRITE mode (output Port).



A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Fig.11 READ mode (input Port).

Interrupt (see Figs 12 and 13)

The PCF8574 provides an open drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcontroller. This gives these chips a type of master function which can initiate an action elsewhere in the system.

An interrupt is generated by any rising or falling edge of the Port inputs in the input mode. After time t_{iv} the signal $\overline{INT}$ is valid.

Resetting and reactivating the interrupt circuit is achieved when data on the Port is changed to the original setting or data is read from or written to the Port which has generated the interrupt.

Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH-to-LOW transition of the SCL signal.
- Interrupts which occur during the acknowledge clock pulse may be lost (or very short) due to the resetting of the interrupt during this pulse.

Each change of the Ports after the resettings will be detected and after the next rising clock edge, will be transmitted as $\overline{INT}$. Reading from or writing to another device does not affect the interrupt circuit.

Quasi-bidirectional I/O Ports (see Fig.14)

A quasi-bidirectional Port can be used as an input or output without the use of a control signal for data direction. At power-on the Ports are HIGH. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The Ports should be HIGH before being used as inputs.

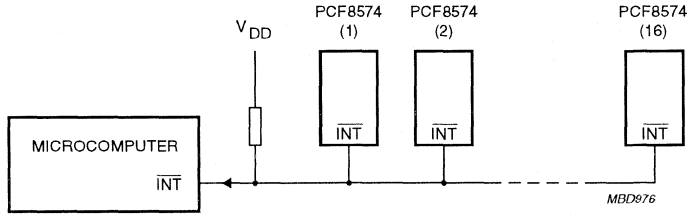


Fig.12 Application of multiple PCF8574s with interrupt.

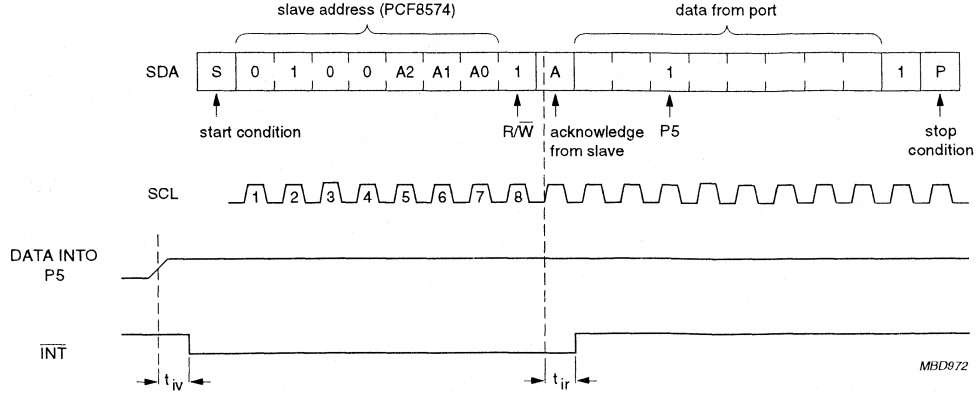


Fig.13 Interrupt generated by a change of input to Port P5.

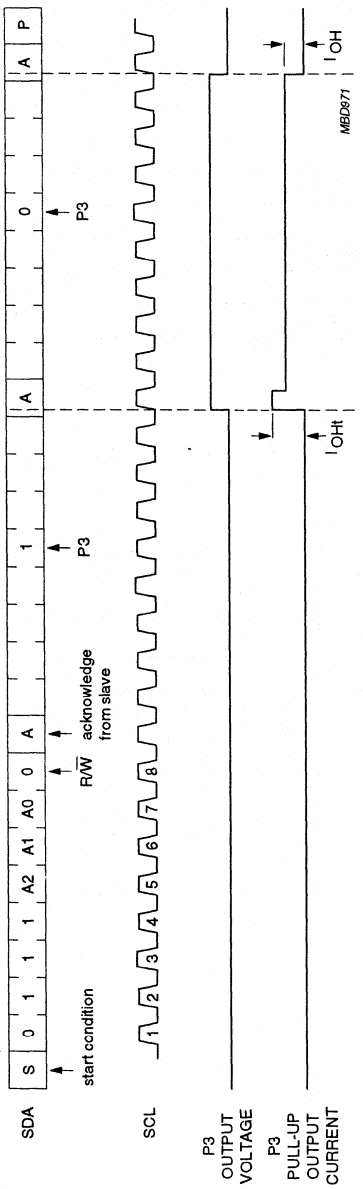


Fig.14 Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+7.0	V
V_I	input voltage	V_{SS} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	−	±20	mA
I_O	DC output current	−	±25	mA
I_{DD}	supply current	−	±100	mA
I_{SS}	supply current	−	±100	mA
P_{tot}	total power dissipation	−	400	mW
P_O	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−40	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.5	−	6.0	V
I_{DD}	supply current	operating mode; V_{DD} = 6 V; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 100 kHz	−	40	100	µA
I_{stb}	standby current	standby mode; V_{DD} = 6 V; no load; $V_I = V_{DD}$ or V_{SS}	−	2.5	10	µA
V_{POR}	power-on reset voltage	V_{DD} = 6 V; no load; $V_I = V_{DD}$ or V_{SS}; note 1	−	1.3	2.4	V
Input SCL; input/output SDA						
V_{IL}	LOW level input voltage		−0.5	−	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	V_{DD} + 0.5	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	−	−	mA
$\|I_L\|$	leakage current	$V_I = V_{DD}$ or V_{SS}	−	−	1	µA
C_I	input capacitance	$V_I = V_{SS}$	−	−	7	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I/O Ports						
V_{IL}	LOW level input voltage		−0.5	−	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	$V_{DD} + 0.5$	V
$I_{IHL(max)}$	maximum allowed input current through protection diode	$V_I \geq V_{DD}$ or $V_I \leq V_{SS}$	−	−	±400	μA
I_{OL}	LOW level output current	V_{OL} = 1 V; V_{DD} = 5 V	10	25	−	mA
I_{OH}	HIGH level output current	$V_{OH} = V_{SS}$	30	−	300	μA
I_{OHt}	transient pull-up current	HIGH during acknowledge (see Fig.14); $V_{OH} = V_{SS}$; V_{DD} = 2.5 V	−	−1	−	mA
C_I	input capacitance		−	−	10	pF
C_O	output capacitance		−	−	10	pF
Port timing (see Figs 10 and 11); **$C_L \leq$ 100 pF**						
t_{pv}	output data valid		−	−	4	μs
t_{su}	input data set-up time		0	−	−	μs
t_h	input data hold time		4	−	−	μs
Interrupt $\overline{INT}$ (see Fig.13)						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	1.6	−	−	mA
$\|I_L\|$	leakage current	$V_I = V_{DD}$ or V_{SS}	−	−	1	μA
TIMING; $C_L \leq$ 100 pF						
t_{iv}	input data valid time		−	−	4	μs
t_{ir}	reset delay time		−	−	4	μs
Select inputs A0 to A2						
V_{IL}	LOW level input voltage		−0.5	−	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	$V_{DD} + 0.5$	V
$\|I_{LI}\|$	input leakage current	pin at V_{DD} or V_{SS}	−	−	250	nA

Note

1. The power-on reset circuit resets the I²C-bus logic with $V_{DD} < V_{POR}$ and sets all Ports to logic 1 (with current source to V_{DD}).

I²C-BUS TIMING CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
I²C-BUS TIMING (see Fig.15; note 1)					
f_{SCL}	SCL clock frequency	–	–	100	kHz
t_{SW}	tolerable spike width on bus	–	–	100	ns
t_{BUF}	bus free time	4.7	–	–	µs
$t_{SU;STA}$	start condition set-up time	4.7	–	–	µs
$t_{HD;STA}$	start condition hold time	4.0	–	–	µs
t_{LOW}	SCL LOW time	4.7	–	–	µs
t_{HIGH}	SCL HIGH time	4.0	–	–	µs
t_r	SCL and SDA rise time	–	–	1.0	µs
t_f	SCL and SDA fall time	–	–	0.3	µs
$t_{SU;DAT}$	data set-up time	250	–	–	ns
$t_{HD;DAT}$	data hold time	0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid	–	–	3.4	µs
$t_{SU;STO}$	stop condition set-up time	4.0	–	–	µs

Note

1. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

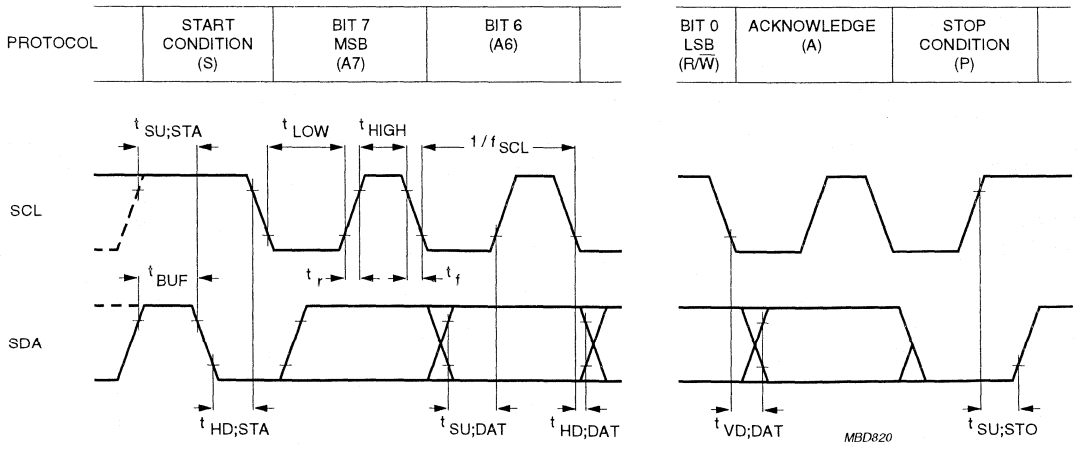


Fig.15 I²C-bus timing diagram.

Universal LCD driver for low multiplex rates PCF8576C

FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 6 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with 24-segment LCD driver PCF8566
- Optimized pinning for plane wiring in both and multiple PCF8576C applications
- Space-saving 56-lead plastic very small outline package (VSO56) or 64-lead low profile quad flat package (LQFP64)
- No external components
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

The PCF8576C is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576C is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I^2C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8576CT	VSO56	plastic very small outline package; 56 leads	SOT190-1
PCF8576CU	–	uncased chip in tray	–
PCF8576CU/10	FFC	chip-on-film frame carrier	–
PCF8576CH	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

BLOCK DIAGRAM

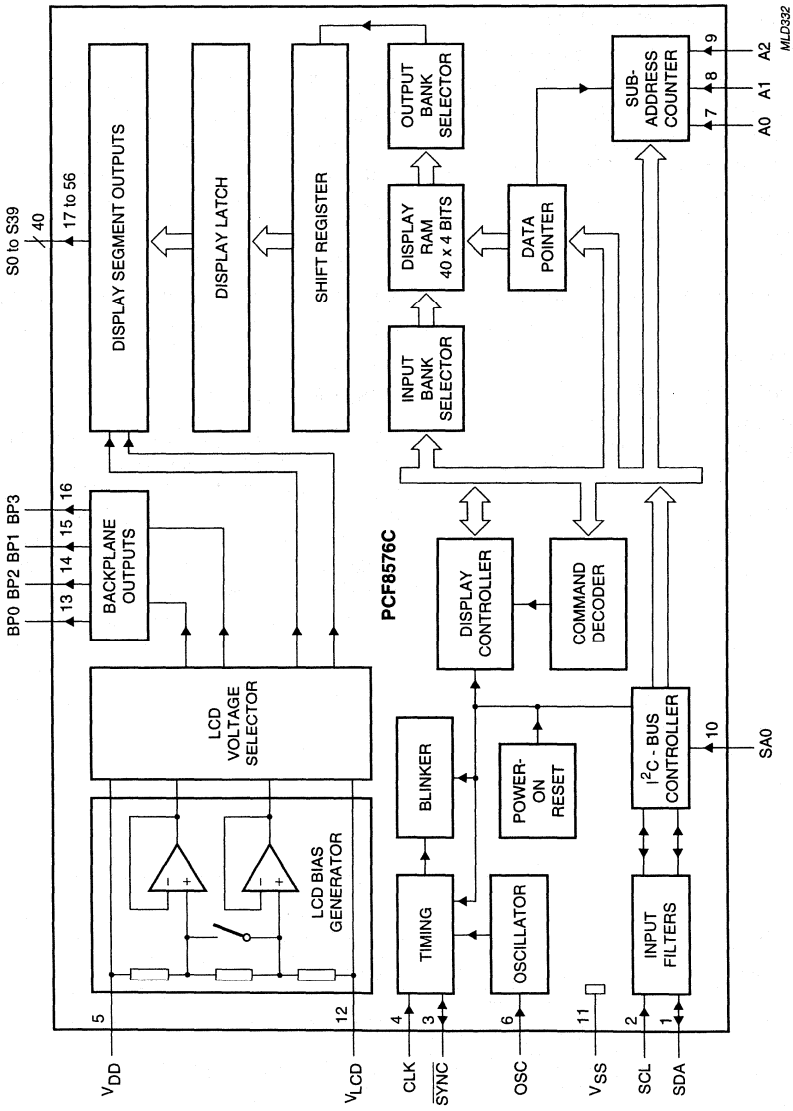


Fig.1 Block diagram; VSO56.

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT190	SOT314	
SDA	1	10	I^2C-bus serial data input/output
SCL	2	11	I^2C-bus serial clock input
$\overline{SYNC}$	3	12	cascade synchronization input/output
CLK	4	13	external clock input
V_{DD}	5	14	supply voltage
OSC	6	15	oscillator input
A0 to A2	7 to 9	16 to 18	I^2C-bus subaddress inputs
SA0	10	19	I^2C-bus slave address input; bit 0
V_{SS}	11	20	logic ground
V_{LCD}	12	21	LCD supply voltage
BP0, BP2, BP1, BP3	13 to 16	25 to 28	LCD backplane outputs
S0 to S39	17 to 56	29 to 32, 34 to 47, 49 to 64, 2 to 7	LCD segment outputs
n.c.	–	1, 8, 9, 22 to 24, 33 and 48	not connected

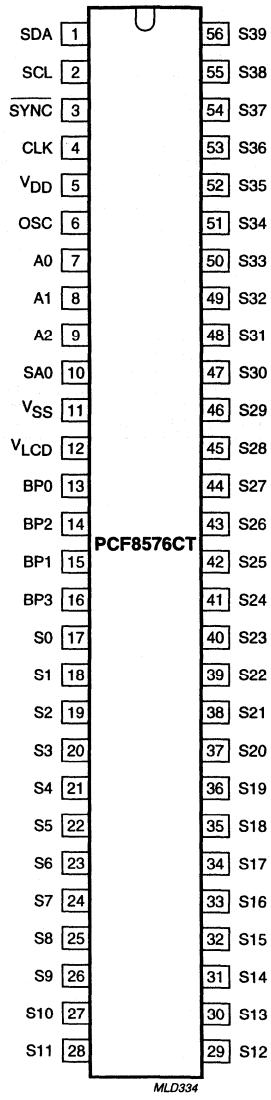


Fig.2 Pin configuration; VSO56.

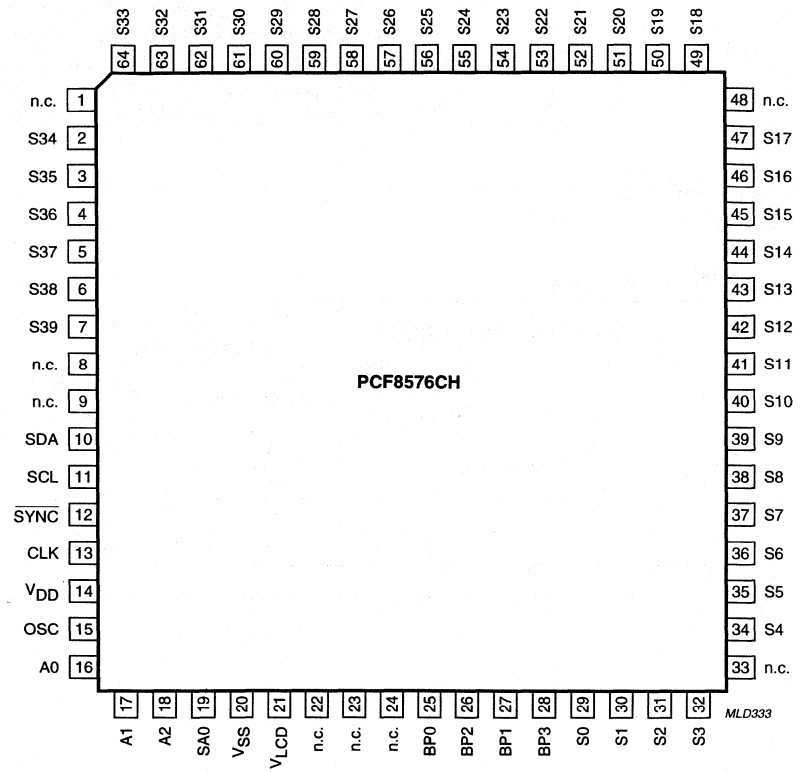


Fig.3 Pin configuration; LQFP64.

FUNCTIONAL DESCRIPTION

The PCF8576C is a versatile peripheral device designed to interface to any microprocessor/microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The display configurations possible with the PCF8576C depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig.4.

The host microprocessor/microcontroller maintains the 2-line I²C-bus communication channel with the PCF8576C. The internal oscillator is selected by tying OSC (pin 6) to V_{SS} (pin 11). The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and the LCD panel chosen for the application.

Table 1 Selection of display configurations

NUMBER OF		7-SEGMENTS NUMERIC		14-SEGMENTS ALPHANUMERIC		DOT MATRIX
BACKPLANES	SEGMENTS	DIGITS	INDICATOR SYMBOLS	CHARACTERS	INDICATOR SYMBOLS	
4	160	20	20	10	20	160 dots (4 × 40)
3	120	15	15	8	8	120 dots (3 × 40)
2	80	10	10	5	10	80 dots (2 × 40)
1	40	5	5	2	12	40 dots (1 × 40)

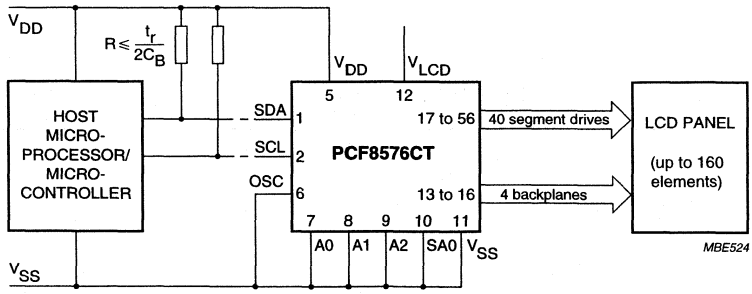


Fig.4 Typical system configuration.

Power-on reset

At power-on the PCF8576C resets to a starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with $\frac{1}{3}$bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C-bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C-bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of the three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of the circuit to provide a $\frac{1}{2}$bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector co-ordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} > 3V_{th}$ approximately.

Multiplex drive ratios of 1 : 3 and 1 : 4 with $\frac{1}{2}$bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1.732$ for 1 : 3 multiplex or $\frac{\sqrt{21}}{3} = 1.528$ for 1 : 4 multiplex).

The advantage of these modes is a reduction of the LCD full-scale voltage V_{op} as follows:

- 1 : 3 multiplex ($\frac{1}{2}$bias):

  $V_{op} = \sqrt{6} \times V_{off\langle rms\rangle} = 2.449\ V_{off(rms)}$

- 1 : 4 multiplex ($\frac{1}{2}$bias):

  $V_{op} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309\ V_{off(rms)}$

These compare with $V_{op} = 3\ V_{off(rms)}$ when $\frac{1}{3}$bias is used.

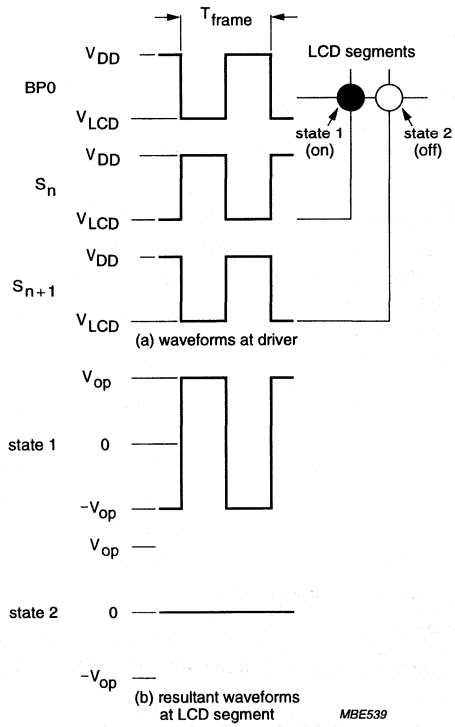
Table 2 Preferred LCD drive modes: summary of characteristics

LCD DRIVE MODE	NUMBER OF		LCD BIAS CONFIGURATION	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on(rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
	BACKPLANES	LEVELS				
static	1	2	static	0	1	∞
1 : 2	2	3	$\frac{1}{2}$	0.354	0.791	2.236
1 : 2	2	4	$\frac{1}{3}$	0.333	0.745	2.236
1 : 3	3	4	$\frac{1}{3}$	0.333	0.638	1.915
1 : 4	4	4	$\frac{1}{3}$	0.333	0.577	1.732

LCD drive mode waveforms

STATIC DRIVE MODE

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig.5.



$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = V_{op}$

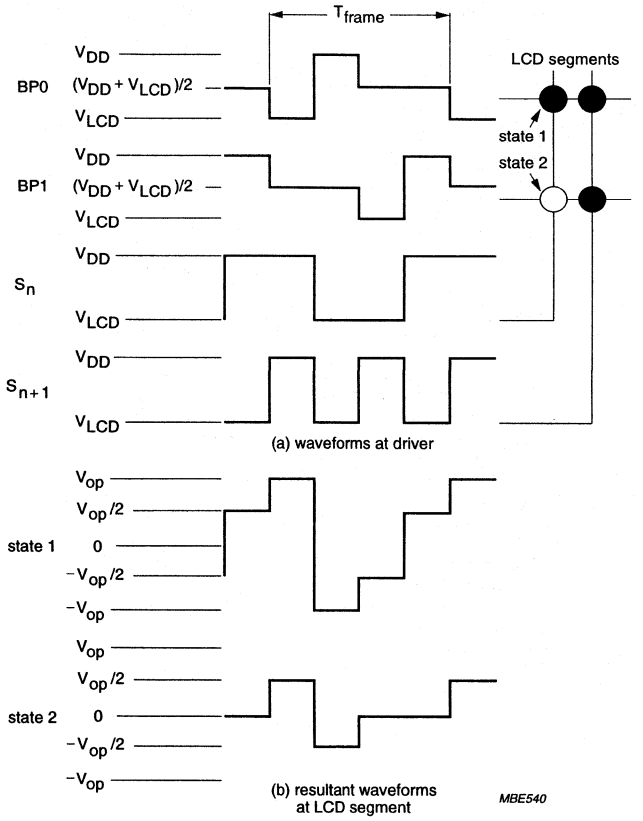
$V_{state2}(t) = V_{S_{n+1}}(t) - V_{BP0}(t)$

$V_{off(rms)} = 0\ V$

Fig.5 Static drive mode waveforms ($V_{op} = V_{DD} - V_{LCD}$).

1 : 2 MULTIPLEX DRIVE MODE

When two backplanes are provided in the LCD, the 1 : 2 multiplex mode applies. The PCF8576C allows use of ½bias or ⅓bias in this mode as shown in Figs 6 and 7.



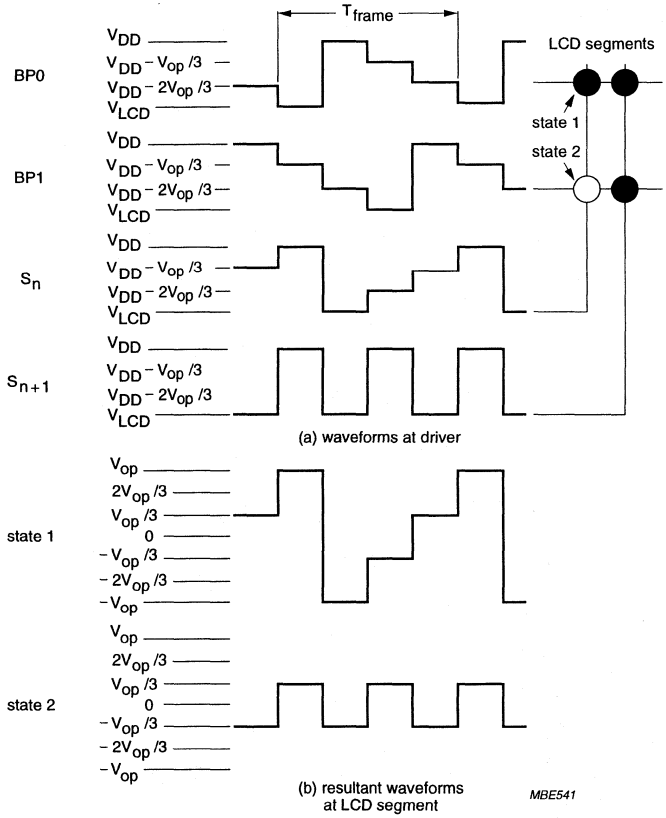
$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = 0.791 V_{op}$

$V_{state2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = 0.354 V_{op}$

Fig.6 Waveforms for the 1 : 2 multiplex drive mode with ½bias ($V_{op} = V_{DD} - V_{LCD}$).



$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = 0.745V_{op}$

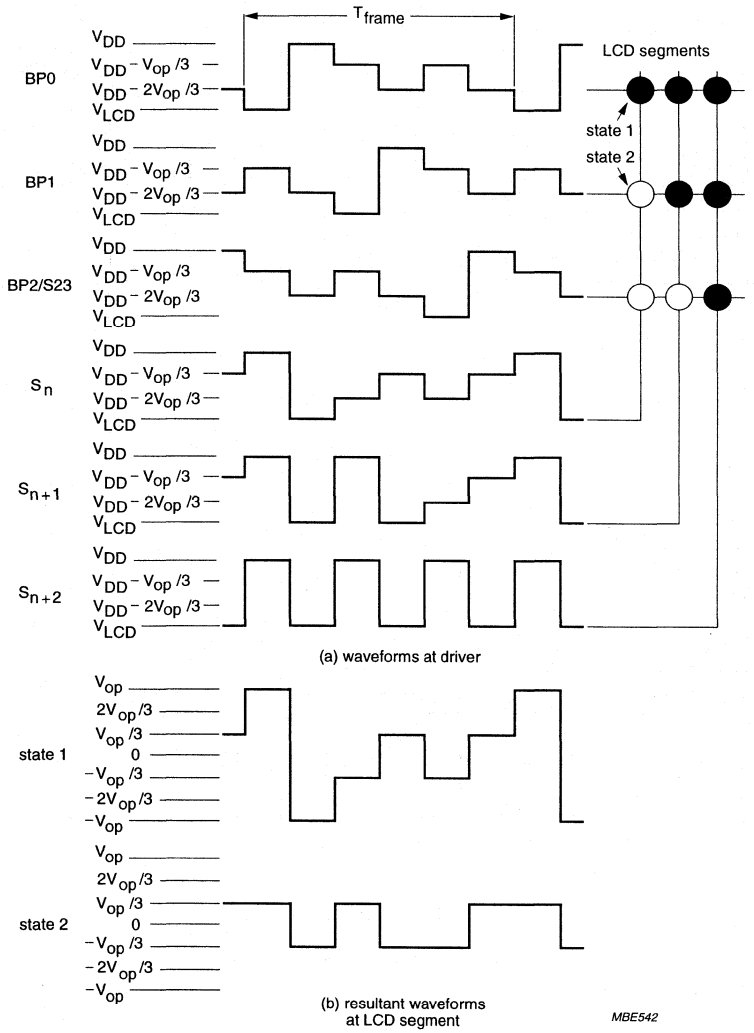
$V_{state2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = 0.333V_{op}$

Fig.7 Waveforms for the 1 : 2 multiplex drive mode with $\frac{1}{3}$bias ($V_{op} = V_{DD} - V_{LCD}$).

1 : 3 MULTIPLEX DRIVE MODE

When three backplanes are provided in the LCD, the 1 : 3 multiplex drive mode applies, as shown in Fig.8.



$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = 0.638V_{op}$

$V_{state2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = 0.333V_{op}$

Fig.8 Waveforms for the 1 : 3 multiplex drive mode ($V_{op} = V_{DD} - V_{LCD}$).

1 : 4 MULTIPLEX DRIVE MODE

When four backplanes are provided in the LCD, the 1 : 4 multiplex drive mode applies, as shown in Fig.9.

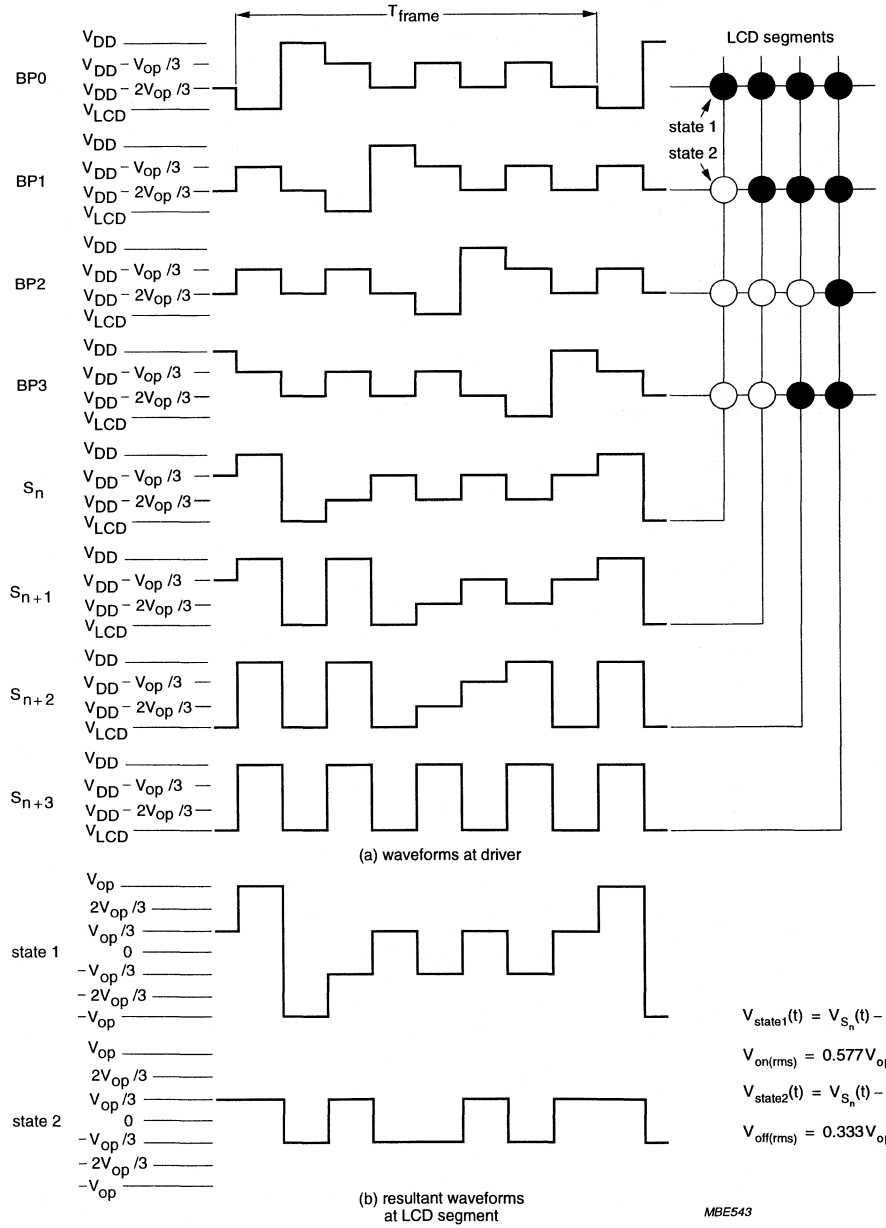


Fig.9 Waveforms for the 1 : 4 multiplex drive mode ($V_{op} = V_{DD} - V_{LCD}$).

Oscillator

INTERNAL CLOCK

The internal logic and the LCD drive signals of the PCF8576C are timed either by the built-in oscillator or from an external clock. When the internal oscillator is used, OSC (pin 6) should be connected to V_{SS} (pin 11). In this event, the output from CLK (pin 4) provides the clock signal for cascaded PCF8566s or PCF8576Cs in the system.

Note that the PCF8576C is backwards compatible with the PCF8576. Where resistor R_{osc} to V_{SS} is present, the internal oscillator is selected.

EXTERNAL CLOCK

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

The clock frequency (f_{clk}) determines the LCD frame frequency and the maximum rate for data reception from the I²C-bus. To allow I²C-bus transmissions at their maximum data rate of 100 kHz, f_{clk} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

Timing

The timing of the PCF8576C organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8576Cs in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (see Table 3). The frame frequency is set by the MODE SET commands when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I²C-bus.

When a device is unable to digest a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I²C-bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data is displayed.

Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 (pins 17 to 56) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data resident in the display latch. When less than 40 segment outputs are required the unused segment outputs should be left open-circuit.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open-circuit. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 40 × 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the on state of the corresponding LCD segment; similarly, a logic 0 indicates the off state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 40 segments operated with respect to backplane BP0 (see Fig.10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

When display data is transmitted to the PCF8576C the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig.11; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig.11, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses.

In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Table 3 LCD frame frequencies

PCF8576C MODE	FRAME FREQUENCY	NOMINAL FRAME FREQUENCY (Hz)
Normal mode	$\frac{f_{clk}}{2880}$	64
Power-saving mode	$\frac{f_{clk}}{480}$	64

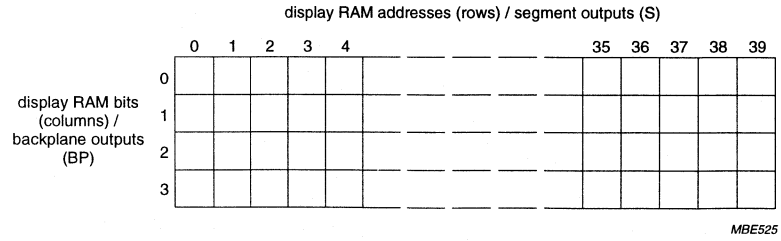


Fig.10 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig.11. The data pointer is automatically incremented in accordance with the chosen LCD configuration. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode) or by two (1 : 2 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF8576C occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1 : 3 multiplex mode).

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence.
In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 and 1 are selected and, in the static mode, bit 0 is selected.

The PCF8576C includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independent of the output bank selector.

Blinker

The display blinking capabilities of the PCF8576C are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads.

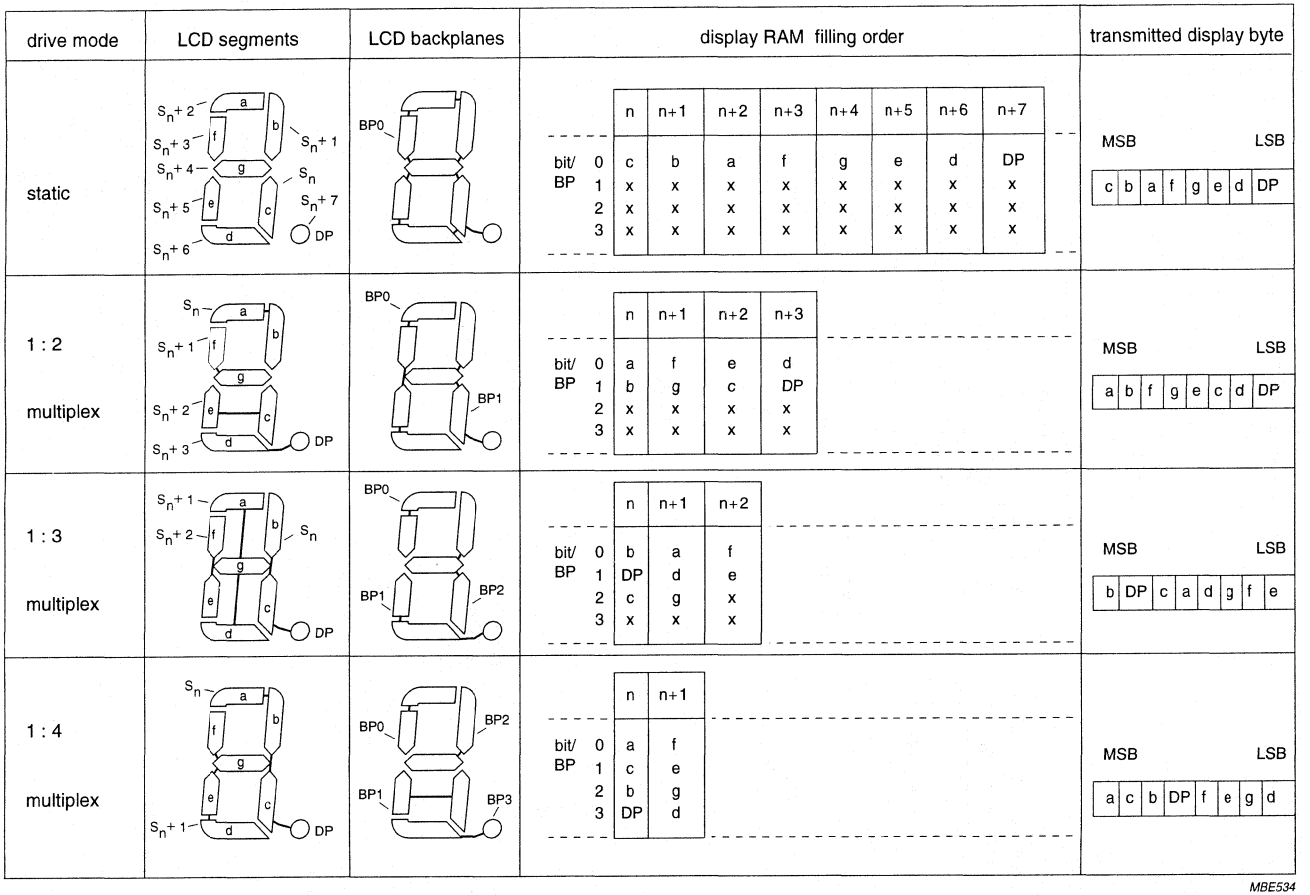
By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 4 Blinking frequencies

BLINKING MODE	NORMAL OPERATING MODE RATIO	POWER-SAVING MODE RATIO	NOMINAL BLINKING FREQUENCY
Off	–	–	blinking off
2 Hz	$\frac{f_{clk}}{92160}$	$\frac{f_{clk}}{15360}$	2 Hz
1 Hz	$\frac{f_{clk}}{184320}$	$\frac{f_{clk}}{30720}$	1 Hz
0.5 Hz	$\frac{f_{clk}}{368640}$	$\frac{f_{clk}}{61440}$	0.5 Hz



x = data bit unchanged.

Fig.11 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C-bus.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer (see Fig.12)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

Start and stop conditions (see Fig.13)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

System configuration (see Fig.14)

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

Acknowledge (see Fig.15)

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

PCF8576C I²C-bus controller

The PCF8576C acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF8576C are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device application, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} in accordance with a binary coding scheme such that no two devices with a common I²C-bus slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8576C is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576C forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C-bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C-bus protocol

Two I²C-bus slave addresses (0111000 and 0111001) are reserved for the PCF8576C. The least significant bit of the slave address that a PCF8576C will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8576C can be distinguished on the same I²C-bus which allows:

1. Up to 16 PCF8576Cs on the same I²C-bus for very large LCD applications.
2. The use of two types of LCD multiplex on the same I²C-bus.

The I²C-bus protocol is shown in Fig.16. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the two PCF8675C slave addresses available. All PCF8576Cs with the corresponding SA0 level acknowledge in parallel with the slave address but all PCF8576Cs with the alternative SA0 level ignore the whole I²C-bus transfer.

After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8576Cs.

The last command byte is tagged with a cleared most significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576Cs on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data is directed to the intended PCF8576C device. The acknowledgement after each byte is made only by the (A0, A1 and A2) addressed PCF8576C. After the last display byte, the I²C-bus master issues a STOP condition (P).

Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. All available commands carry a continuation bit C in their most significant bit position (Fig.17). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

The five commands available to the PCF8576C are in defined in Table 5.

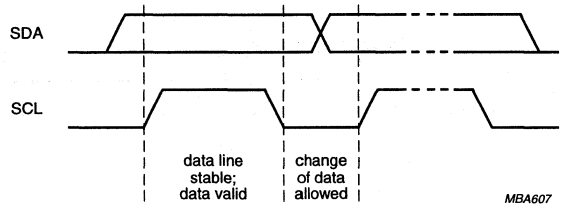


Fig.12 Bit transfer.

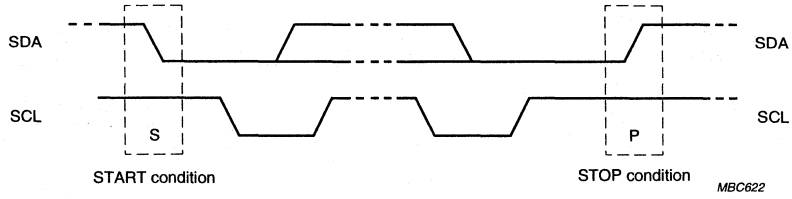


Fig.13 Definition of START and STOP conditions.

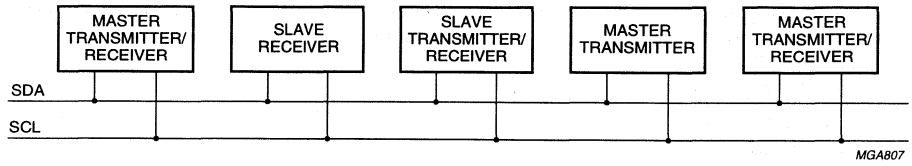


Fig.14 System configuration.

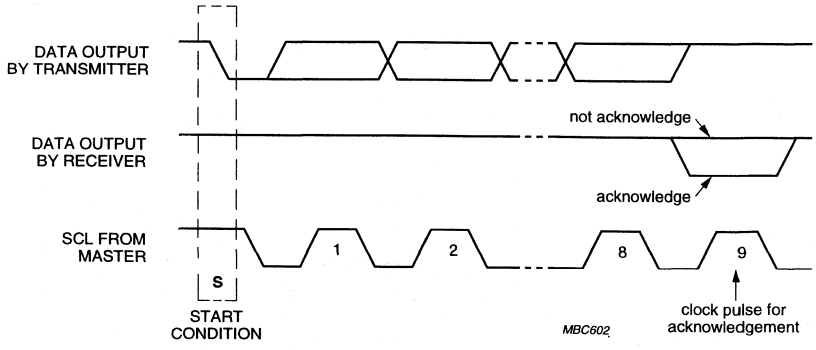


Fig.15 Acknowledgement on the I^2C-bus.

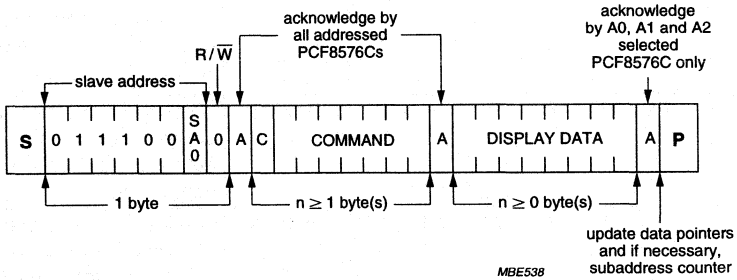
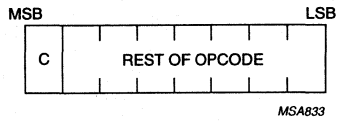


Fig.16 I²C-bus protocol.



C = 0; last command.
C = 1; commands continue.

Fig.17 General format of command byte.

Table 5 Definition of PCF8576C commands

COMMAND	OPCODE								OPTIONS	DESCRIPTION
MODE SET	C	1	0	LP	E	B	M1	M0	Table 6	Defines LCD drive mode.
									Table 7	Defines LCD bias configuration.
									Table 8	Defines display status. The possibility to disable the display allows implementation of blinking under external control.
									Table 9	Defines power dissipation mode.
LOAD DATA POINTER	C	0	P5	P4	P3	P2	P1	P0	Table 10	Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of forty display RAM addresses.
DEVICE SELECT	C	1	1	0	0	A2	A1	A0	Table 11	Three bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of eight hardware subaddresses.
BANK SELECT	C	1	1	1	1	0	I	O	Table 12	Defines input bank selection (storage of arriving display data).
									Table 13	Defines output bank selection (retrieval of LCD display data). The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes.
BLINK	C	1	1	1	0	A	BF1	BF0	Table 14	Defines the blinking frequency.
									Table 15	Selects the blinking mode; normal operation with frequency set by BF1, BF0 or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes.

Table 6 Mode set option 1

LCD DRIVE MODE		BITS	
DRIVE MODE	BACKPLANE	M1	M0
Static	1 BP	0	1
1 : 2	MUX (2 BP)	1	0
1 : 3	MUX (3 BP)	1	1
1 : 4	MUX (4 BP)	0	0

Table 7 Mode set option 2

LCD BIAS	BIT B
1/3 bias	0
1/2 bias	1

Table 8 Mode set option 3

DISPLAY STATUS	BIT E
Disabled (blank)	0
Enabled	1

Table 9 Mode set option 4

MODE	BIT LP
Normal mode	0
Power-saving mode	1

Table 10 Load data pointer option 1

DESCRIPTION	BITS					
6 bit binary value of 0 to 39	P5	P4	P3	P2	P1	P0

Table 11 Device select option 1

DESCRIPTION	BITS		
3 bit binary value of 0 to 7	A0	A1	A2

Table 12 Bank select option 1

STATIC	1 : 2 MUX	BIT I
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 13 Bank select option 2

STATIC	1 : 2 MUX	BIT O
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 14 Blink option 1

BLINK FREQUENCY	BITS	
	BF1	BF0
Off	0	0
2 Hz	0	1
1 Hz	1	0
0.5 Hz	1	1

Table 15 Blink option 2

BLINK MODE	BIT A
Normal blinking	0
Alternation blinking	1

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576C and co-ordinates their effects.The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8576Cs can be distinguished on the same I^2C-bus by using the 3-bit hardware subaddress (A0, A1 and A2) and the programmable I^2C-bus slave address (SA0). When cascaded PCF8576Cs are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8576Cs of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (Fig.18).

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF8576Cs. This synchronization is guaranteed after the power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8576Cs with differing SA0 levels are cascaded). $\overline{SYNC}$ is organized as an input/output pin; the output selection being realized as an open-drain driver with an internal pull-up resistor.
A PCF8576C asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8675C to assert $\overline{SYNC}$. The timing relationship between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF8576C are shown in Fig.19.

For single plane wiring of packaged PCF8576Cs and chip-on-glass cascading, see Chapter "Application information".

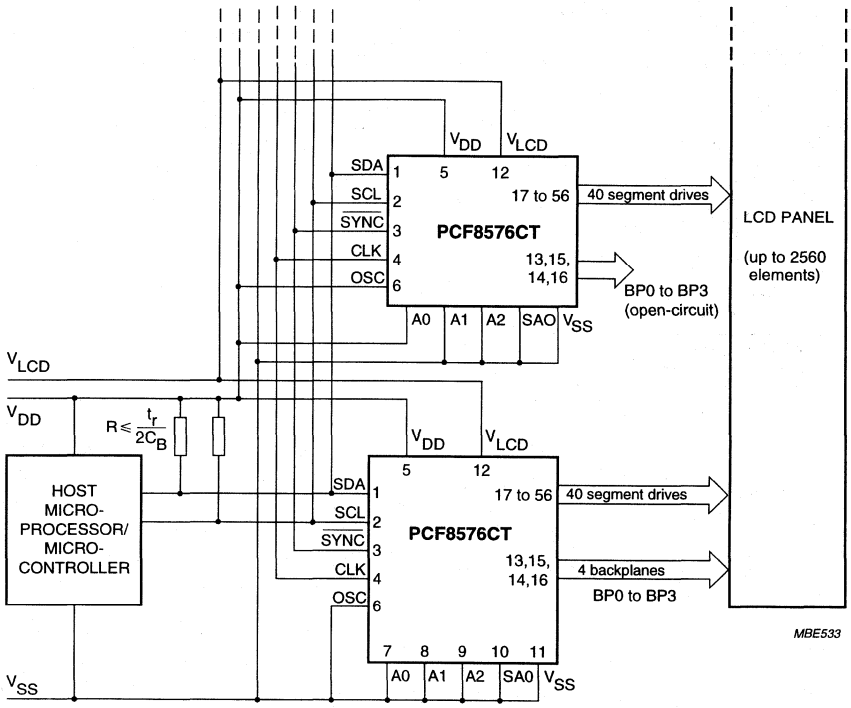
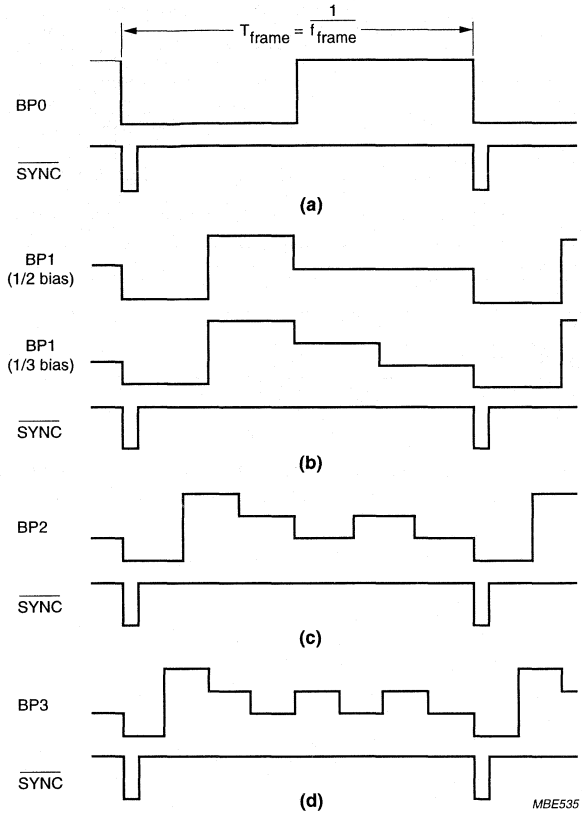


Fig.18 Cascaded PCF8576C configuration.



Excessive capacitive coupling between SCL or CLK and $\overline{SYNC}$ may cause erroneous synchronization. If this proves to be a problem, the capacitance of the $\overline{SYNC}$ line should be increased (e.g. by an external capacitor between $\overline{SYNC}$ and V_{DD}). Degradation of the positive edge of the $\overline{SYNC}$ pulse may be countered by an external pull-up resistor.

(a) static drive mode.

(b) 1 : 2 multiplex drive mode.

(c) 1 : 3 multiplex drive mode.

(d) 1 : 4 multiplex drive mode.

Fig.19 Synchronization of the cascade for the various PCF8576C drive modes.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+8.0	V
V_{LCD}	LCD supply voltage	V_{DD} − 8.0	V_{DD}	V
V_I	input voltage SDA, SCL, CLK, $\overline{SYNC}$, SA0, OSC, A0 to A2	V_{SS} − 0.5	V_{DD} + 0.5	V
V_O	output voltage S0 to S39, BP0 to BP3	V_{LCD} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	−20	+20	mA
I_O	DC output current	−25	+25	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	−50	+50	mA
P_{tot}	total power dissipation	−	400	mW
P_O	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

DC CHARACTERISTICS

V_{DD} = 2 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 2 V to V_{DD} − 6 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2	–	6	V
V_{LCD}	LCD supply voltage	note 1	V_{DD} − 6	–	V_{DD} − 2	V
I_{DD}	supply current	note 2				
	normal mode	f_{clk} = 200 kHz	–	–	120	μA
	power-saving mode	f_{clk} = 35 kHz; V_{DD} = 3.5 V; V_{LCD} = 0 V; A0, A1 and A2 tied to V_{SS}	–	–	60	μA
Logic						
V_{IL}	LOW level input voltage		V_{SS}	–	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD}	V
V_{OL}	LOW level input voltage	I_{OL} = 0 mA	–	–	0.05	V
V_{OH}	HIGH level input voltage	I_{OH} = 0 mA	V_{DD} − 0.05	–	–	V
I_{OL1}	LOW level output current CLK, $\overline{SYNC}$	V_{OL} = 1 V; V_{DD} = 5 V	1	–	–	mA
I_{OH1}	HIGH level output current CLK	V_{OH} = 4 V; V_{DD} = 5 V	−1	–	–	mA
I_{OL2}	LOW level output current SDA, SCL	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
I_{L1}	leakage current SA0, A0 to A2, CLK, SDA and SCL	V_I = V_{DD} or V_{SS}	−1	–	+1	μA
I_{L2}	leakage current OSC	V_I = V_{DD}	−1	–	+1	μA
I_{pd}	A0, A1, A2 and OSC pull-down current	V_I = 1 V; V_{DD} = 5 V	15	50	150	μA
$R_{\overline{SYNC}}$	pull-up resistor ($\overline{SYNC}$)		20	50	150	kΩ
V_{POR}	power-on reset voltage level	note 3	–	1.0	1.6	V
t_{SW}	tolerable spike width on bus		–	–	100	ns
C_I	input capacitance	note 4	–	–	7	pF
LCD outputs						
V_{BP}	DC voltage component BP0 to BP3	C_{BP} = 35 nF	−20	–	+20	mV
V_S	DC voltage component S0 to S39	C_S = 5 nF	−20	–	+20	mV
R_{BP}	output resistance BP0 to BP3	note 5; V_{LCD} = V_{DD} − 5 V	–	–	5	kΩ
R_S	output resistance S0 to S39	note 5; V_{LCD} = V_{DD} − 5 V	–	–	7.5	kΩ

Notes

1. $V_{LCD} \leq V_{DD} - 3$ V for 1/3 bias.
2. LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I^2C-bus inactive.
3. Resets all logic when $V_{DD} < V_{POR}$.
4. Periodically sampled, not 100% tested.
5. Outputs measured one at a time.

AC CHARACTERISTICS

V_{DD} = 2 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 2 V to V_{DD} − 6 V; T_{amb} = −40 to + 85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clk}	oscillator frequency					
	normal mode	V_{DD} = 5 V; note 1	125	200	315	kHz
	power-saving mode	V_{DD} = 3.5 V	21	31	48	kHz
t_{clkH}	CLK HIGH time		1	–	–	µs
t_{clkL}	CLK LOW time		1	–	–	µs
t_{PSYNC}	$\overline{SYNC}$ propagation delay time		–	–	400	ns
$t_{\overline{SYNC}L}$	$\overline{SYNC}$ LOW time		1	–	–	µs
t_{PLCD}	driver delays with test loads	V_{LCD} = V_{DD} − 5 V	–	–	30	µs
Timing characteristics: I²C-bus; note 2						
t_{BUF}	bus free time		4.7	–	–	µs
$t_{HD;STA}$	START condition hold time		4.0	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	–	–	µs

Notes

1. At f_{clk} < 125 kHz, I²C-bus maximum transmission speed is derated.
2. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

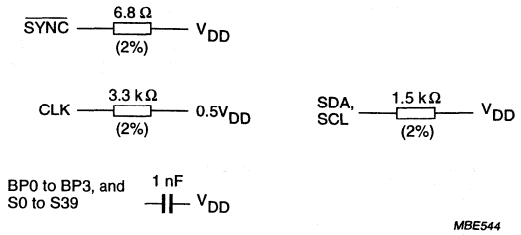


Fig.20 Test loads.

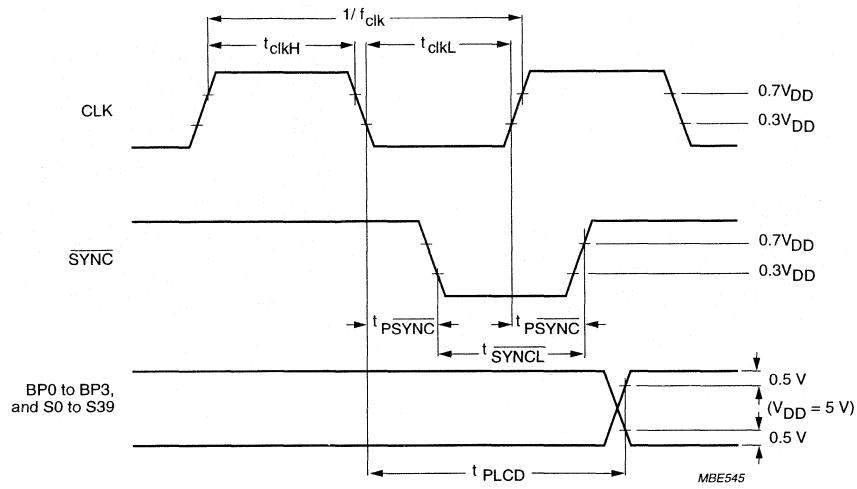


Fig.21 Driver timing waveforms.

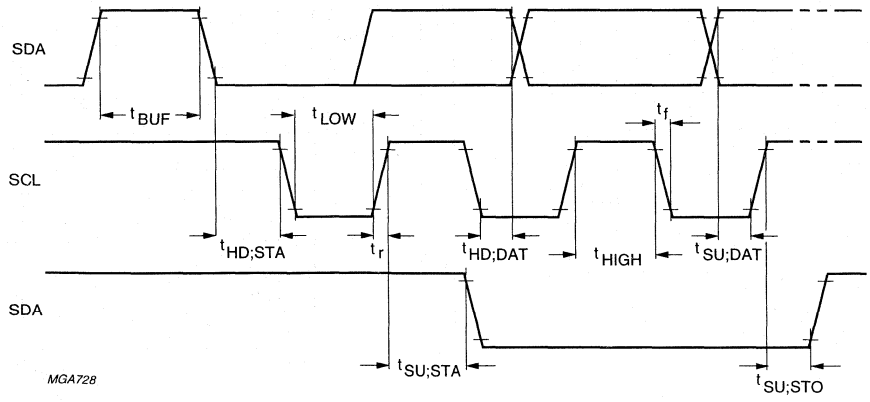
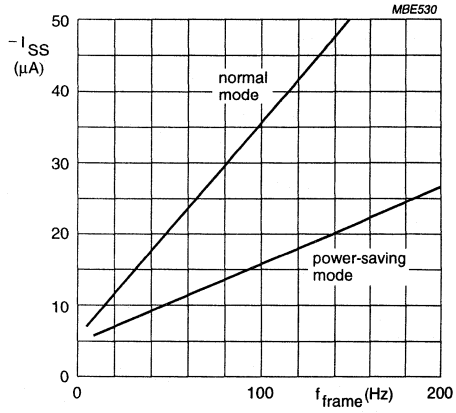


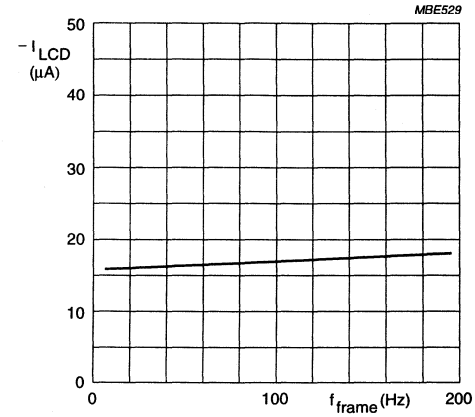
Fig.22 I²C-bus timing waveforms.

Typical supply current characteristics



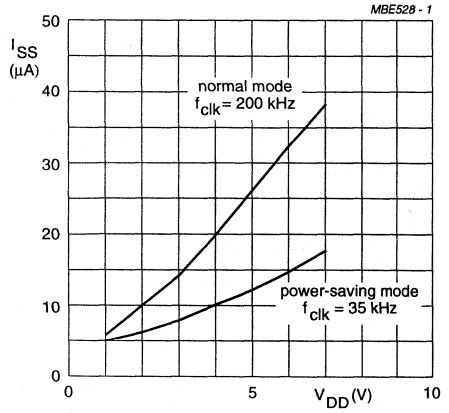
V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

Fig.23 $-I_{SS}$ as a function of f_{frame}.



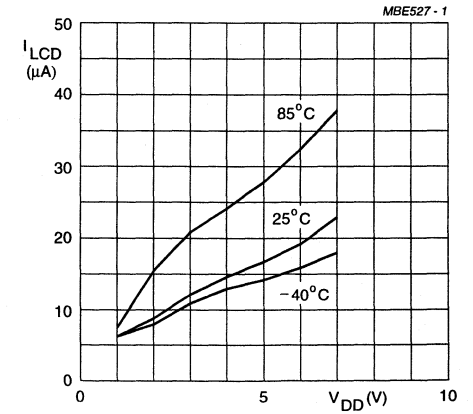
V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

Fig.24 $-I_{LCD}$ as a function of f_{frame}.



V_{LCD} = 0 V; external clock; T_{amb} = 25 °C.

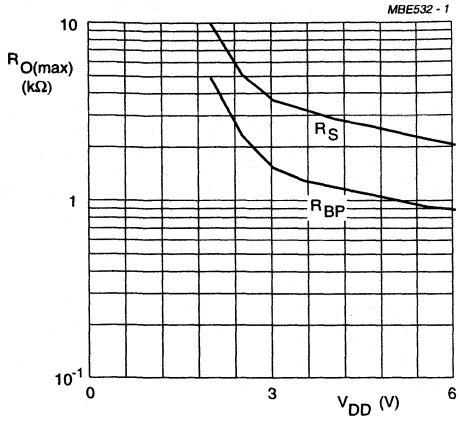
Fig.25 I_{SS} as a function of V_{DD}.



V_{LCD} = 0 V; external clock; f_{clk} = nominal frequency.

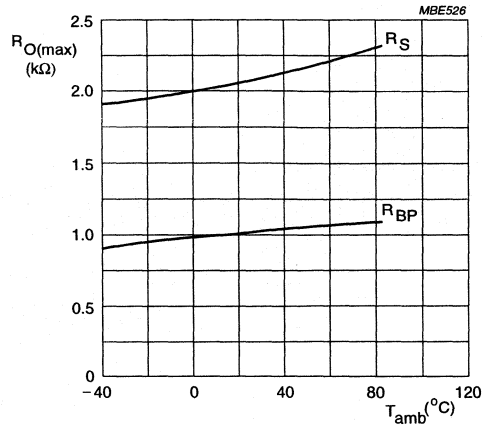
Fig.26 I_{LCD} as a function of V_{DD}.

Typical characteristics of LC D outputs



V_{LCD} = 0 V; T_{amb} = 25 °C.

Fig.27 $R_{O(max)}$ as a function of V_{DD}.



V_{DD} = 5 V; V_{LCD} = 0 V.

Fig.28 $R_{O(max)}$ as a function of T_{amb}.

APPLICATION INFORMATION

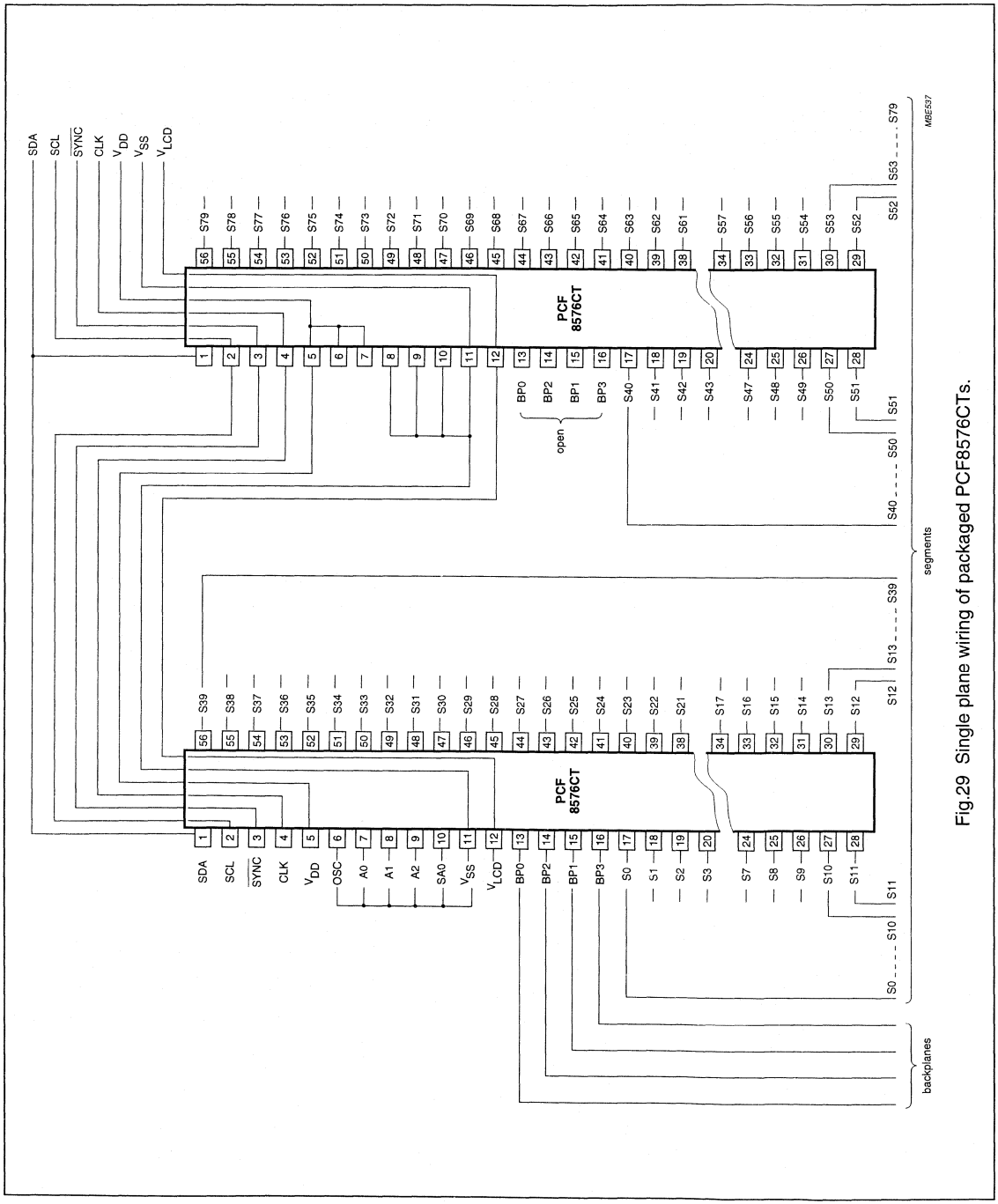


Fig.29 Single plane wiring of packaged PCF8576CTs.

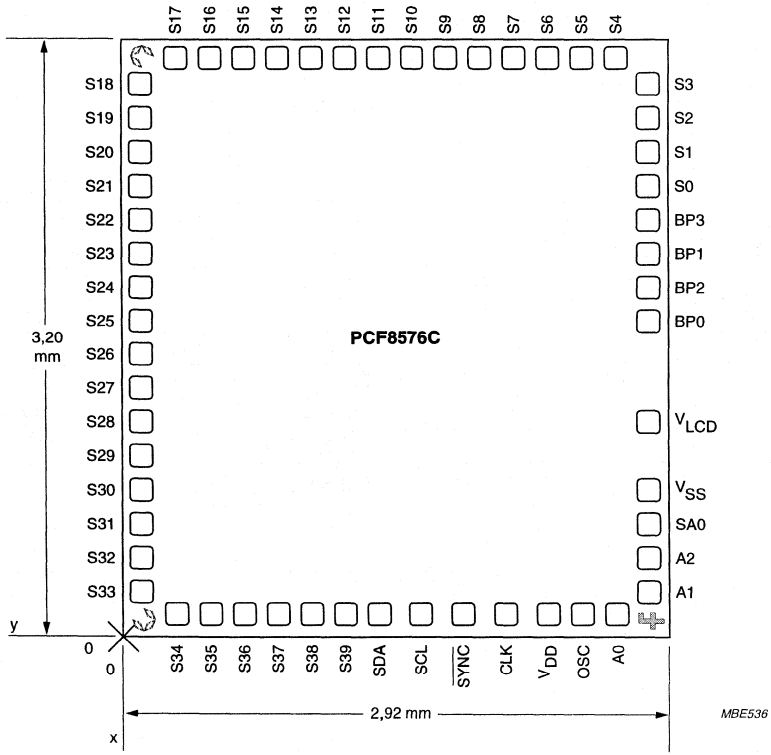
Chip-on-glass cascadability in single plane

In chip-on-glass technology, where driver devices are bonded directly onto glass of the LCD, it is important that the devices may be cascaded without the crossing of conductors, but the paths of conductors can be continued on the glass under the chip. All of this is facilitated by the PCF8576C bonding pad layout (Fig.30). Pads needing bus interconnection between all PCF8576Cs are the cascade are V_{DD}, V_{SS}, V_{LCD}, CLK, SCL, SDA and $\overline{SYNC}$. These lines may be led to the corresponding pads of the next PCF8576C through the wide opening between V_{LCD} pad and the backplane output pads.

The only bussed line that does not require a second opening to lead through to the next PCF8576C is V_{LCD}, being the cascade centre. The placing of V_{LCD} adjacent to V_{SS} allows the two supplies to be tied together.

When an external clocking source is to be used, OSC of all devices should be tied to V_{DD}. The pads OSC, A0, A1, A2 and SA0 have been placed between V_{SS} and V_{DD} to facilitate wiring of oscillator, hardware subaddress and slave address.

BONDING PAD LOCATIONS



Chip dimensions: approximately 2.92 × 3.20 mm.
Pad area: 0.0121 mm².
Bonding pad dimensions: 110 × 110 µm.

Fig.30 Bonding pad locations.

Table 16 Bonding pad locations (dimensions in μm)

All x/y coordinates are referenced to left-hand bottom corner of chip, see Fig.30.

SYMBOL	PAD	x	y
SDA	1	−74	−1380
SCL	2	148	−1380
$\overline{SYNC}$	3	355	−1380
CLK	4	534	−1380
V_{DD}	5	742	−1380
OSC	6	913	−1380
A0	7	1087	−1380
A1	8	1290	−1284
A2	9	1290	−1116
SA0	10	1290	−945
V_{SS}	11	1290	−751
V_{LCD}	12	1290	−485
BP0	13	1290	125
BP1	14	1290	285
BP2	15	1290	458
BP3	16	1290	618
S0	17	1290	791
S1	18	1290	951
S2	19	1290	1124
S3	20	1290	1284
S4	21	1074	1380
S5	22	914	1380
S6	23	741	1380
S7	24	581	1380
S8	25	408	1380
S9	26	248	1380
S10	27	75	1380
S11	28	−85	1380
S12	29	−258	1380
S13	30	−418	1380
S14	31	−591	1380
S15	32	−751	1380
S16	33	−924	1380
S17	34	−1084	1380
S18	35	−1290	1243
S19	36	−1290	1083
S20	37	−1290	910
S21	38	−1290	750
S22	39	−1290	577
S23	40	−1290	417
S24	41	−1290	244
S25	42	−1290	84
S26	43	−1290	−89
S27	44	−1290	−249
S28	45	−1290	−422
S29	46	−1290	−582
S30	47	−1290	−755
S31	48	−1290	−915
S32	49	−1290	−1088
S33	50	−1290	−1248
S34	51	−1083	−1380
S35	52	−923	−1380
S36	53	−750	−1380
S37	54	−590	−1380
S38	55	−417	−1380
S39	56	−257	−1380
Alignment marks			
C1	−	−1290	1385
C2	−	−1295	−1385
F	−	1305	−1405

LCD direct/duplex driver with I²C-bus interface

PCF8577C

FEATURES

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2.5 to 6 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- Display memory switching in direct drive mode
- May be used as I²C-bus output expander
- System expansion up to 256 segments
- Power-on reset blanks display.

GENERAL DESCRIPTION

The PCF8577C is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex configuration.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. I²C-bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware subaddressing and display memory switching (direct drive mode).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8577CP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF8577CT	VSO40	plastic very small outline package; 40 leads	SOT158A
PCF8577CT	–	V6040 in blister tape	–
PCF8577CU/10	–	chip on film-frame-carrier (FFC)	–

BLOCK DIAGRAM

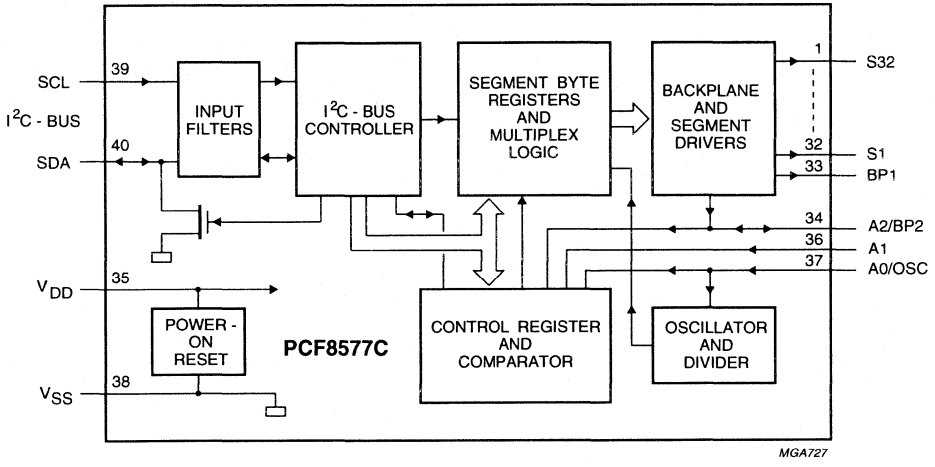


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
S32 to S1	1 to 32	segments outputs
BP1	33	cascade sync input/backplane output
A2/BP2	34	hardware address line and cascade sync input/backplane output
V_{DD}	35	positive supply voltage
A1	36	hardware address line input
A0/OSC	37	hardware address line and oscillator pin input
V_{SS}	38	negative supply voltage
SCL	39	I²C-bus clock line input
SDA	40	I²C-bus data line input/output

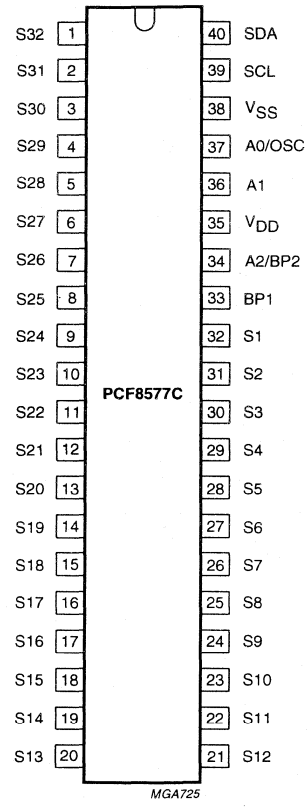


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Hardware subaddress A0, A1, A2

The hardware subaddress lines A0, A1 and A2 are used to program the device subaddress for each PCF8577C connected to the I²C-bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pin-out requirements.

1. Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as HIGH (logic 1) when connected to V_{DD}.
2. Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V_{SS} or V_{DD} respectively.
3. In the direct drive mode the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to V_{DD}.
4. In the duplex drive mode the second backplane signal BP2 is required and the A2 signal is undefined. In this mode device selection is made exclusively from lines A0 and A1.

Oscillator A0/OSC

The PCF8577C has a single-pin built-in oscillator which provides the modulation for the LCD segment driver outputs. One external resistor and one external capacitor are connected to the A0/OSC pin to form the oscillator (see Figs 15 and 16). For correct start-up of the oscillator after power on, the resistor and capacitor must be connected to the same V_{SS}/V_{DD} as the chip. In an expanded system containing more than one PCF8577C the backplane signals are usually common to all devices and only one oscillator is required. The devices which are not used for the oscillator are put into the cascade mode by connecting the A0/OSC pin to either V_{DD} or V_{SS} depending on the required state for A0. In the cascade mode each PCF8577C is synchronized from the backplane signal(s).

User-accessible registers

There are nine user-accessible 1-byte registers. The first is a control register which is used to control the loading of data into the segment byte registers and to select display options. The other eight are segment byte registers, split into two banks of storage, which store the segment data. The set of even numbered segment byte registers is called BANK A. Odd numbered segment byte registers are called BANK B.

There is one slave address for the PCF8577C (see Fig.6). All addressed devices load the second byte into the control register and each device maintains an identical copy of the control byte in the control register at all times (see I²C-bus protocol Fig.7), i.e. all addressed devices respond to control commands sent on the I²C-bus.

The control register is shown in more detail in Fig.3. The least-significant bits select which device and which segment byte register is loaded next. This part of the register is therefore called the Segment Byte Vector (SBV).

The upper three bits of the SBV (V5 to V3) are compared with the hardware subaddress input signals A2, A1 and A0. If they are the same then the device is enabled for loading, if not the device ignores incoming data but remains active.

The three least-significant bits of the SBV (V2 to V0) address one of the segment byte registers within the enabled chip for loading segment data.

The control register also has two display control bits. These bits are named MODE and BANK. The MODE bit selects whether the display outputs are configured for direct or duplex drive displays. The BANK bit allows the user to display BANK A or BANK B.

Auto-incremented loading

After each segment byte is loaded the SBV is incremented automatically. Thus auto-incremented loading occurs if more than one segment byte is received in a data transfer.

Since the SBV addresses both device and segment registers in all addressed chips, auto-incremented loading may proceed across device boundaries provided that the hardware subaddresses are arranged contiguously.

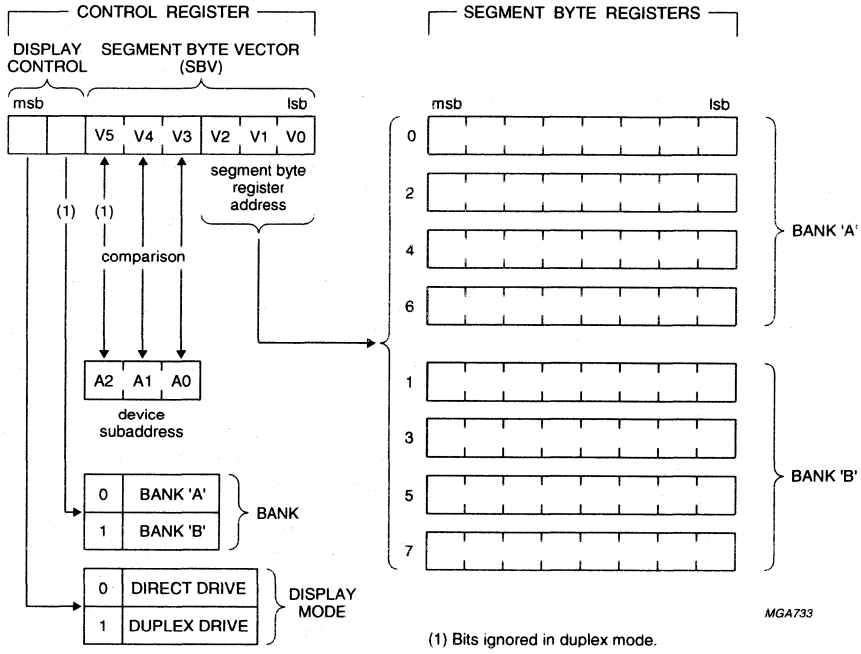
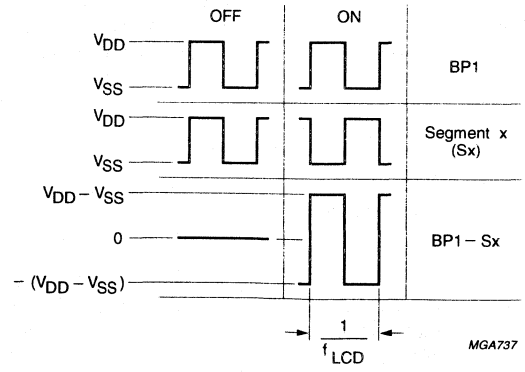


Fig.3 PCF8577C register organization.



$V_{on(rms)} = V_{DD} - V_{SS}$; $V_{off(rms)} = 0$.

Fig.4 Direct drive mode display output waveforms.

Direct drive mode

The PCF8577C is set to the direct drive mode by loading the MODE control bit with logic 0. In this mode only four bytes are required to store the data for the 32 segment drivers. Setting the BANK bit to logic 0 selects even bytes (BANK A), setting the BANK bit to logic 1 selects odd bytes (BANK B).

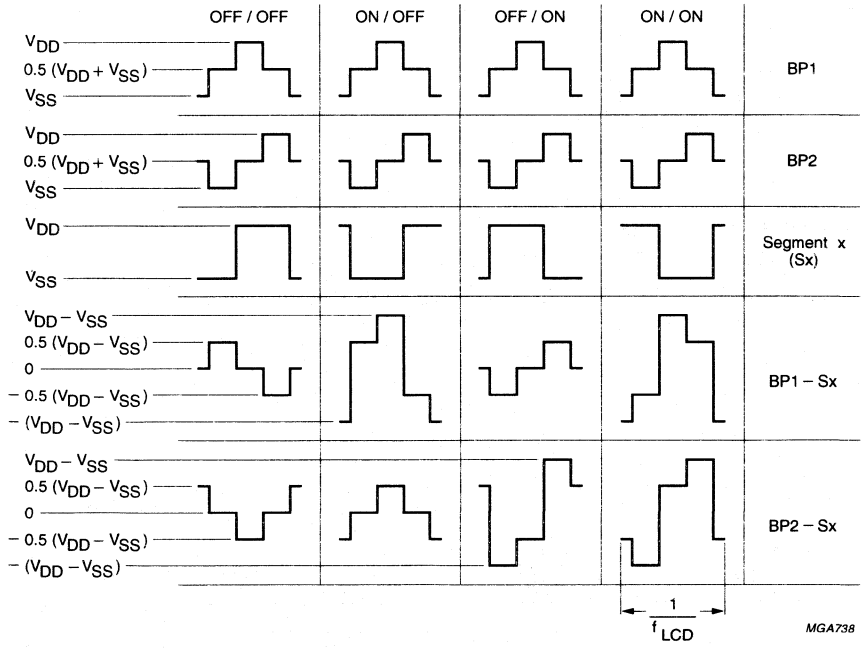
In the direct drive mode the SBV is auto-incremented by two after the loading of each segment byte register. This means that auto-incremented loading of BANK A or BANK B is possible. Either bank may be completely or partially loaded irrespective of which bank is being displayed. Direct drive output waveforms are shown in Fig.4.

Duplex mode

The PCF8577C is set to the duplex mode by loading the MODE bit with logic 1. In this mode a second backplane signal (BP2) is needed and pin A2/BP2 is used for this; therefore A2 and its equivalent SBV bit V5 are undefined. The SBV auto-increments by one between loaded bytes.

All of the segment bytes are required to store data for the 32 segment drivers and the BANK bit is ignored.

Duplex mode output waveforms are shown in Fig.5.



$V_{on(rms)} = 0.791\ (V_{DD} - V_{SS})$; $V_{off(rms)} = 0.354\ (V_{DD} - V_{SS})$.

$\frac{V_{on\,(rms)}}{V_{off\,(rms)}} = 2.236$

Fig.5 Duplex mode display output waveforms.

Power-on reset

At power-on reset the PCF8577C resets to a defined starting condition as follows:

1. Both backplane outputs are set to V_{SS} in master mode; to 3-state in cascade mode.
2. All segment outputs are set to V_{SS}.
3. The segment byte registers and control register are cleared.
4. The I²C-bus interface is initialized.

Slave address

The PCF8577C slave address is shown in Fig.6.

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

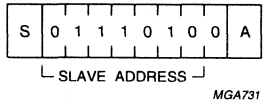


Fig.6 PCF8577C slave address.

I²C-bus protocol

The PCF8577C I²C-bus protocol is shown in Fig.7.

The PCF8577C is a slave receiver and has a fixed slave address (see Fig.6). All PCF8577Cs with the same slave address acknowledge the slave address in parallel. The second byte is always the control byte and is loaded into the control register of each PCF8577C connected to the I²C-bus. All addressed devices acknowledge the control byte. Subsequent data bytes are loaded into the segment registers of the selected device. Any number of data bytes may be loaded in one transfer and in an expanded system rollover of the SBV from 111 111 to 000 000 is allowed. If a stop (P) condition is given after the control byte acknowledge the segment data will remain unchanged. This allows the BANK bit to be toggled without changing the segment register contents. During loading of segment data only the selected PCF8577C gives an acknowledge. Loading is terminated by generating a stop (P) condition.

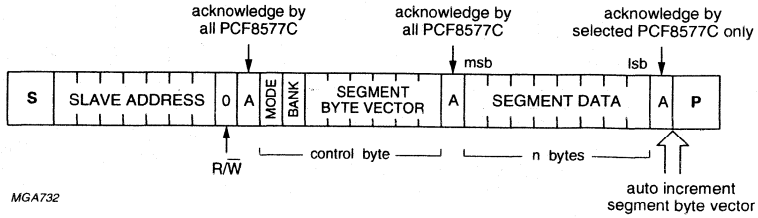


Fig.7 I²C-bus protocol.

Display memory mapping

The mapping between the eight segment registers and the segment outputs S1 to S32 is given in Tables 1 and 2.

Since only one register bit per segment is needed in the direct drive mode, the BANK bit allows swapping of display information. If BANK is set to logic 0 even bytes (BANK A) are displayed; if BANK is set to logic 1 odd bytes (BANK B) are displayed. BP1 is always used for the backplane output in the direct drive mode. In duplex mode even bytes (BANK A) correspond to backplane 1 (BP1) and odd bytes (BANK B) correspond to backplane 2 (BP2).

Table 1 Segment byte-segment driver mapping in direct drive mode

MODE	BANK	V 2	V 1	V 0	SEGMENT/ BIT/ REGISTER	MSB 7	6	5	4	3	2	1	LSB 0	BACK-PLANE
0	0	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	1	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	0	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	1	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	0	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	1	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	0	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
0	1	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP1

Mapping example: bit 0 of register 7 controls the LCD segment S25 if BANK bit is a logic 1.

Table 2 Segment byte-segment driver mapping in duplex mode

MODE	BANK[1]	V 2	V 1	V 0	SEGMENT/ BIT/ REGISTER	MSB 7	6	5	4	3	2	1	LSB 0	BACK-PLANE
1	x	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
1	x	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP2
1	x	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
1	x	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP2
1	x	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
1	x	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP2
1	x	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
1	x	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP2

Note

1. Where x = don't care.

Mapping example: bit 7 of register 5 controls the LCD segment S24/BP2.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the I²C-bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

Start and stop conditions

Both data and clock lines remain HIGH when the I²C-bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the I²C-bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

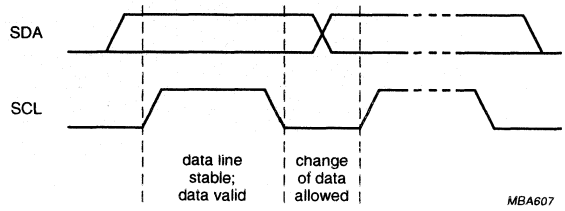


Fig.8 Bit transfer.

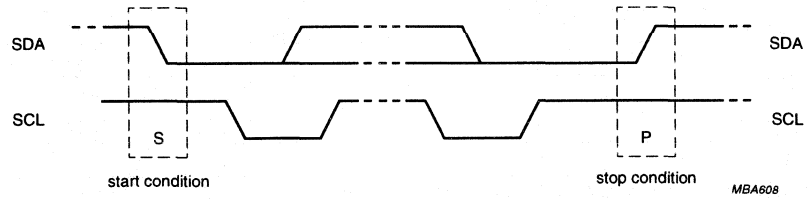


Fig.9 Definition of the start and stop conditions.

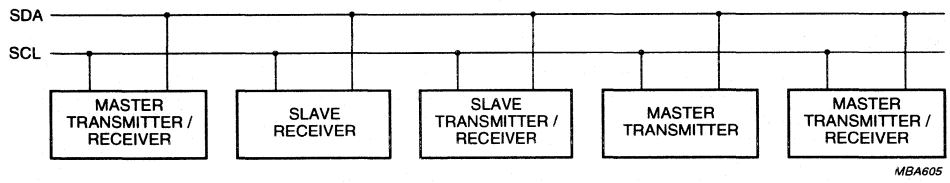


Fig.10 System configuration.

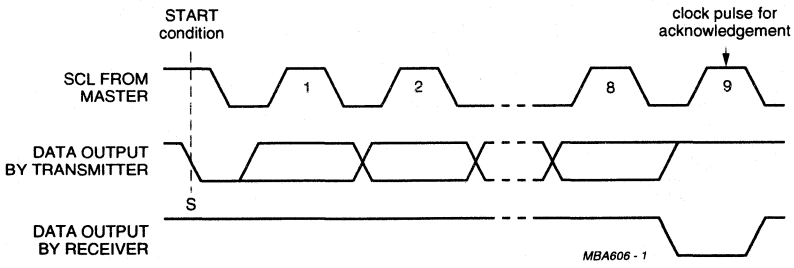


Fig.11 Acknowledgement on the I²C-bus.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+8.0	V
V_I	input voltage on pin		−0.5	V_{DD} + 0.5	V
I_{DD}; I_{SS}	V_{DD} or V_{SS} current		−50	+50	mA
I_I	DC input current		−20	+20	mA
I_O	DC output current		−25	+25	mA
P_{tot}	power dissipation per package	note 1	−	500	mW
P_O	power dissipation per output		−	100	mW
T_{stg}	storage temperature		−65	+150	°C

Note

1. Reduce by 7.7 mW/K when $T_{amb} > 60$ °C.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices.

DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to 85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.5	−	6	V
I_{DD}	supply current for non-specified inputs at V_{DD} or V_{SS}	no load; f_{SCL} = 100 kHz; R_{osc} = 1 MΩ; C_{osc} = 680 pF		50	125	µA
		no load; f_{SCL} = 0; R_{osc} = 1 MΩ; C_{osc} = 680 pF	−	25	75	µA
		no load; f_{SCL} = 0; R_{osc} = 1 MΩ; C_{osc} = 680 pF; V_{DD} = 5 V; T_{amb} = 25 °C	−	25	40	µA
		no load; f_{SCL} = 0; direct mode; A0/OSC = V_{DD}; V_{DD} = 5 V; T_{amb} = 25 °C	−	10	20	µA
V_{POR}	power-on reset level	note 2	−	1.1	2.0	V
Input A0						
V_{IL1}	LOW level input voltage		0	−	0.05	V
V_{IH1}	HIGH level input voltage		V_{DD} − 0.05	−	V_{DD}	V
Input A1						
V_{IL2}	LOW level input voltage		0	−	0.3V_{DD}	V
V_{IH2}	HIGH level input voltage		0.7V_{DD}	−	V_{DD}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
Input A2						
V_{IL3}	LOW level input voltage		0	–	0.10	V
V_{IH3}	HIGH level input voltage		V_{DD} – 0.10	–	V_{DD}	V
Input SCL; SDA						
V_{IL4}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH4}	HIGH level input voltage		$0.7V_{DD}$	–	6	V
C_I	input capacitance	note 3	–	–	7	pF
Output SDA						
I_{OL}	LOW level output current	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
A1; SCL; SDA						
I_{L1}	leakage current	$V_I = V_{DD}$ or V_{SS}	–1	–	+1	µA
A2/BP2; BP1						
I_{L2}	leakage current	$V_I = V_{DD}$ or V_{SS}	–5	–	+5	µA
A2/BP2						
I_{pd}	pull-down current	$V_I = V_{DD}$	–5	–1.5	–	µA
A0/OSC						
I_{L3}	leakage current	$V_I = V_{DD}$	–1	–	–	µA
Oscillator						
I_{OSC}	start-up current	$V_I = V_{SS}$	–	1.2	5	µA
LCD outputs						
V_{BP}	DC component of LCD driver		–	±20	–	mV
I_{OL1}	LOW level segment output current	V_{DD} = 5 V; V_{OL} = 0.8 V; note 4	0.3	–	–	mA
I_{OH1}	HIGH level segment output current	V_{DD} = 5 V; $V_{OH} = V_{DD}$ – 0.8 V; note 4	–	–	–0.3	mA
R_{BP}	backplane output resistance (BP1; BP2)	$V_O = V_{SS}$ or V_{DD} or $(V_{SS} + V_{DD})/2$; note 5	–	0.4	5	kΩ

Notes

1. Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.
2. Resets all logic when $V_{DD} < V_{POR}$.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. Outputs measured one at a time; V_{DD} = 5 V; I_{load} = 100 µA.

AC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; T_{amb} = −40 to 85 °C; unless otherwise specified. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
f_{LCD}	display frequency	C_{osc} = 680 pF; R_{osc} = 1 MΩ	65	90	120	Hz
t_{BS}	driver delays with test loads	V_{DD} = 5 V	–	20	100	µs
I²C-bus						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SW}	tolerable spike width on I²C-bus	T_{amb} = 25 °C	–	–	100	ns
t_{BUF}	I²C-bus free time		4.7	–	–	µs
$t_{SU;STA}$	start condition set-up time		4.0	–	–	µs
$t_{HD;STA}$	start condition hold time		4.0	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1.0	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	stop condition set-up time		4.0	–	–	µs

Note

1. Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.

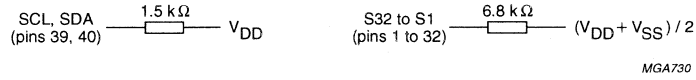


Fig.12 Test loads.

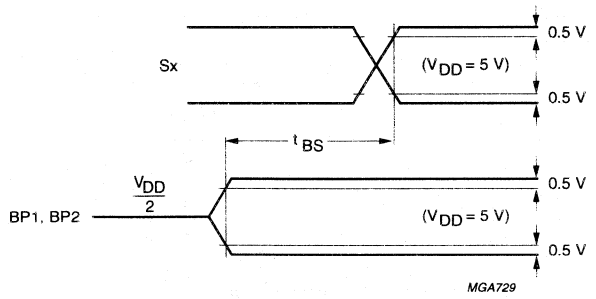


Fig.13 Driver timing waveforms.

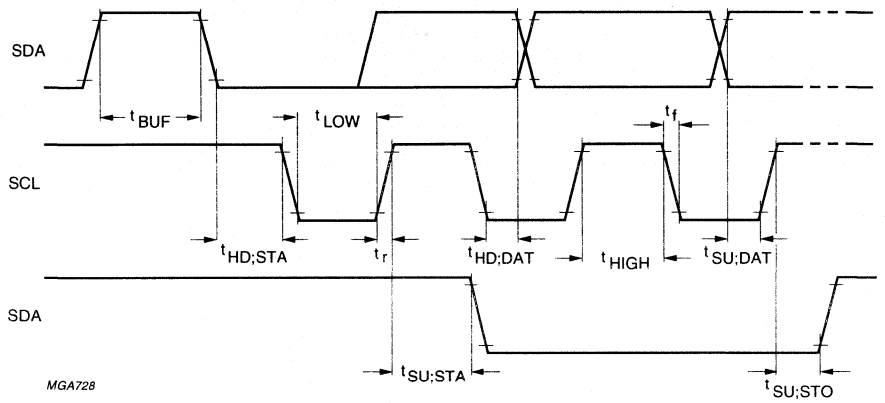


Fig.14 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

APPLICATION INFORMATION

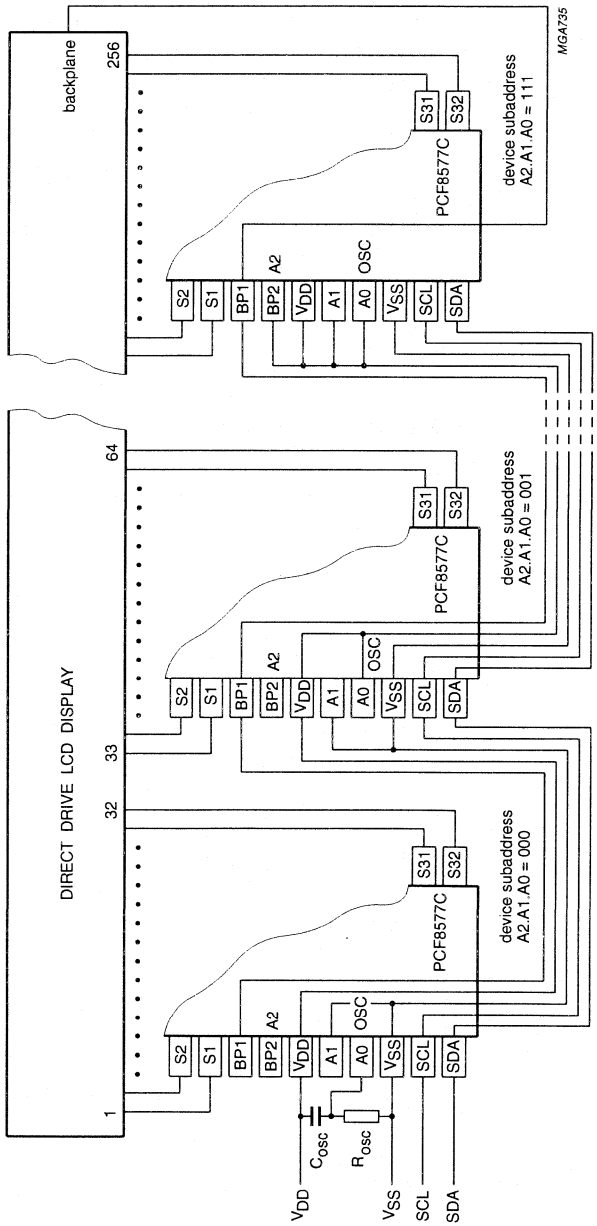


Fig.15 Direct display driver; expansion to 256 segments using eight PCF8577Cs.

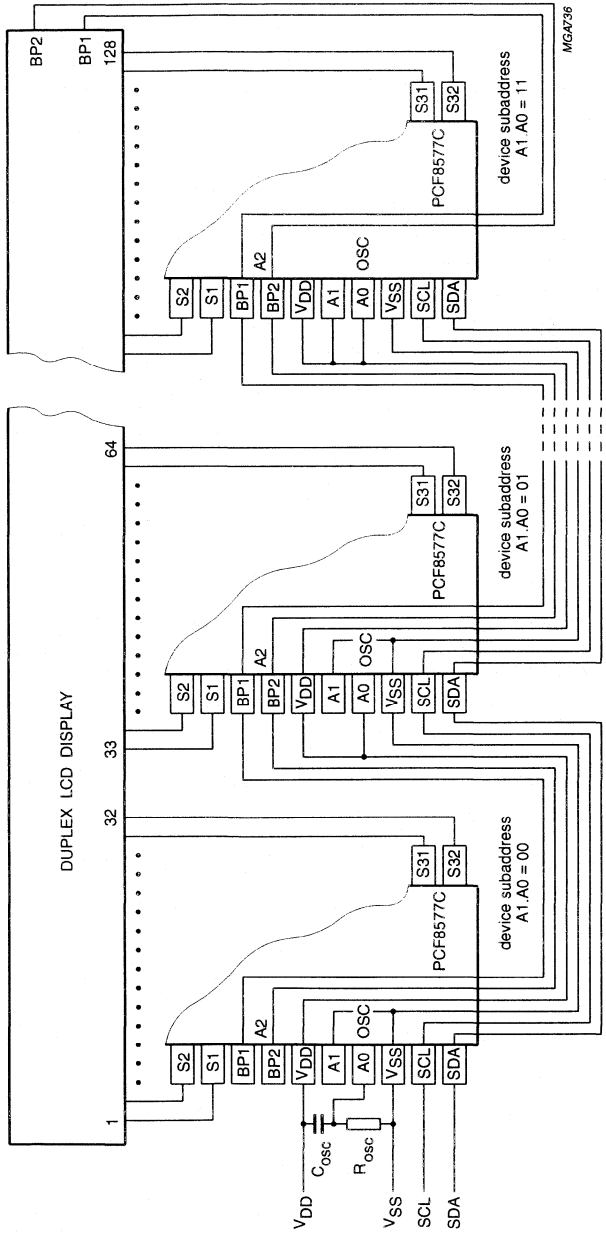
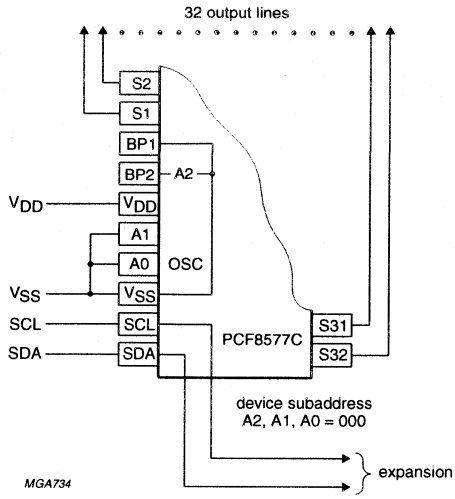


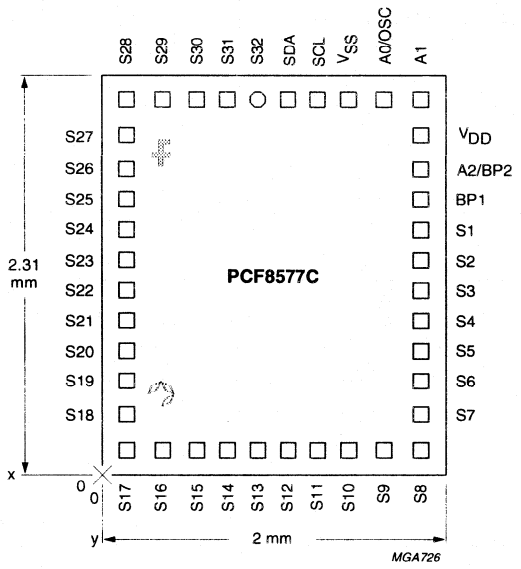
Fig.16 Duplex display; expansion to 2 × 128 segments using four PCF8577Cs.



MODE bit must always be set to logic 0 (direct drive).
BANK switching is permitted.
BP1 must always be connected to V_{SS} and A0/OSC must be connected to either V_{DD} or V_{SS} (no LCD modulation).

Fig.17 Use of PCF8577C as a 32-bit output expander in I²C-bus application.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area = 4.62 mm².
Thickness = 381 ±25 µm.
n-substrate (back) connected to V_{DD}.
Bonding pad dimensions = 110 µm × 110 µm.

Fig.18 Bonding pad locations.

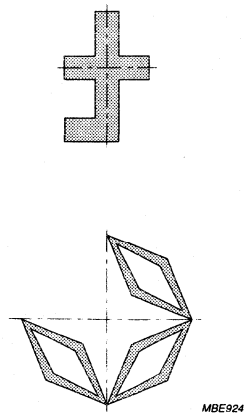


Fig.19 Reference marks.

Table 3 Bonding pad locations (dimensions in μm)

All x and y co-ordinates are referenced to bottom left corner, see Fig.18.

SIGNAL	PAD POSITION CENTERED	
	x	y
S32	−86	941
S31	−257	941
S30	−428	941
S29	−599	941
S28	−836	941
S27	−836	769
S26	−836	598
S25	−836	427
S24	−836	256
S23	−836	85
S22	−836	−86
S21	−836	−257
S20	−836	−428
S19	−836	−599
S18	−836	−770
S17	−836	−941
S16	−599	−941
S15	−428	−941
S14	−257	−941
S13	−86	−941
S12	85	−941
S11	256	−941

SIGNAL	PAD POSITION CENTERED	
	x	y
S10	427	−941
S9	598	−941
S8	836	−941
S7	836	−770
S6	836	−599
S5	836	−428
S4	836	−257
S3	836	−86
S2	836	85
S1	836	256
BP1	836	427
A2/BP2	836	598
V_{DD}	836	769
A1	836	941
A0/OSC	598	941
V_{SS}	427	941
SCL	256	941
SDA	85	941
Recpats		
C	−586	−699
F	−580	663

LCD row/column driver for dot matrix graphic displays

PCF8578

FEATURES

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (40960 dots possible)
- 40 driver outputs, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

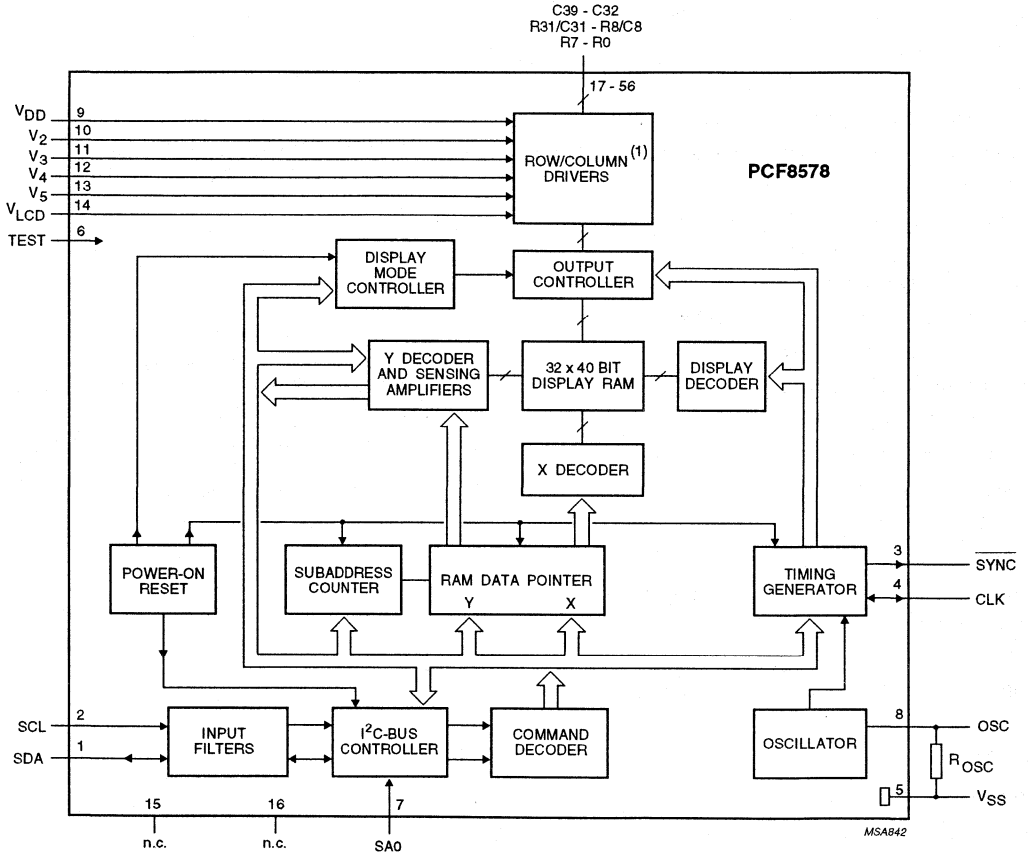
GENERAL DESCRIPTION

The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs, of which 24 are programmable, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8578T	56	VSO56	plastic	SOT190
PCF8578U7	–	chip with bumps on-tape	–	–

BLOCK DIAGRAM



(1) LCD voltage levels, all other blocks operate at logic levels.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus serial data line
SCL	2	I²C-bus serial clock line
$\overline{SYNC}$	3	cascade synchronization output
CLK	4	external clock input/output
V_{SS}	5	ground (logic)
TEST	6	test pin (connect to V_{SS})
SA0	7	I²C-bus slave address input (bit 0)
OSC	8	oscillator input
V_{DD}	9	positive supply voltage
V_2 to V_5	10 to 13	LCD bias voltage inputs
V_{LCD}	14	LCD supply voltage
n.c.	15, 16	not connected
C39 to C32	17 to 24	LCD column driver outputs
R31/C31 to R8/C8	25 to 48	LCD row/column driver outputs
R7 to R0	49 to 56	LCD row driver outputs

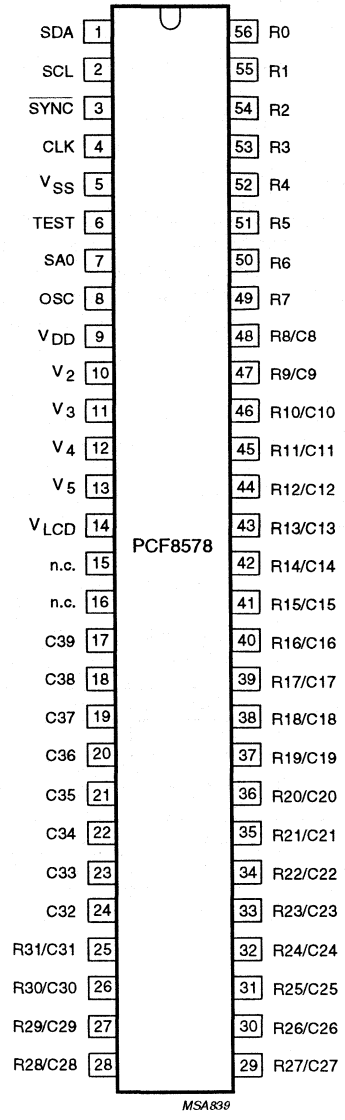


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The PCF8578 row/column driver is designed for use in one of three ways:

- Stand-alone row/column driver for small displays (mixed mode)
- Row/column driver with cascaded PCF8579s (mixed mode)
- Row driver with cascaded PCF8579s (mixed mode).

Mixed mode

In mixed mode, the device functions as both a row and column driver. It can be used in small stand-alone applications, or for larger displays with up to 15 PCF8579s (31 PCF8579s when two slave addresses are used). See Table 1 for common display configurations.

Row mode

In row mode, the device functions as a row driver with up to 32 row outputs and provides the clock and synchronization signals for the PCF8579. Up to 16 PCF8579s can normally be cascaded (32 when two slave addresses are used).

Timing signals are derived from the on-chip oscillator, whose frequency is determined by the value of the resistor connected between OSC and V_{SS}.

Commands sent on the I^2C-bus from the host microprocessor set the mode (row or mixed), configuration (multiplex rate and number of rows and columns) and control the operation of the device. The device may have one of two slave addresses. The only difference between these slave addresses is the least significant bit, which is set by the logic level applied to SA0. The PCF8578 and PCF8579 also have subaddresses. The subaddress of the PCF8578 is only defined in mixed mode and is fixed at 0. The RAM may only be accessed in mixed mode and data is loaded as described for the PCF8579.

Bias levels may be generated by an external potential divider with appropriate decoupling capacitors. For large displays, bias sources with high drive capability should be used. A typical mixed mode system operating with up to 15 PCF8579s is shown in Fig.4 (a stand-alone system would be identical but without the PCF8579s).

Table 1 Possible displays configurations.

APPLICATION	MULTIPLEX RATE	MIXED MODE		ROW MODE		TYPICAL APPLICATIONS
		ROWS	COLUMNS	ROWS	COLUMNS	
Stand alone	1 : 8	8	32	–	–	small digital or alphanumerical displays
	1 : 16	16	24	–	–	
	1 : 24	24	16	–	–	
	1 : 32	32	8	–	–	
With PCF8579	1 : 8	8[1]	632[1]	8 x 4[2]	640[2]	alphanumeric displays and dot matrix graphic displays
	1 : 16	16[1]	624[1]	16 x 2[2]	640[2]	
	1 : 24	24[1]	616[1]	24[2]	640[2]	
	1 : 32	32[1]	608[1]	24[2]	640[2]	

Notes

1. Using 15 PCF8579s.
2. Using 16 PCF8579s.

Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the LCD threshold voltage (V_{th}). V_{th} is typically defined as the RMS voltage at which the LCD exhibits 10% contrast. Table 2 shows the optimum voltage bias levels for the PCF8578 as functions of V_{op} ($V_{op} = V_{DD} - V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{op} is obtained by equating $V_{off(rms)}$ with V_{th}.

Table 2 Optimum LCD voltages.

PARAMETER	MULTIPLEX RATE			
	1 : 8	1 : 16	1 : 24	1 : 32
$\frac{V_2}{V_{op}}$	0.739	0.800	0.830	0.850
$\frac{V_3}{V_{op}}$	0.522	0.600	0.661	0.700
$\frac{V_4}{V_{op}}$	0.478	0.400	0.339	0.300
$\frac{V_5}{V_{op}}$	0.261	0.200	0.170	0.150
$\frac{V_{off(rms)}}{V_{op}}$	0.297	0.245	0.214	0.193
$\frac{V_{on(rms)}}{V_{op}}$	0.430	0.316	0.263	0.230
$D = \frac{V_{on(rms)}}{V_{off(rms)}}$	1.447	1.291	1.230	1.196
$\frac{V_{op}}{V_{th}}$	3.370	4.080	4.680	5.190

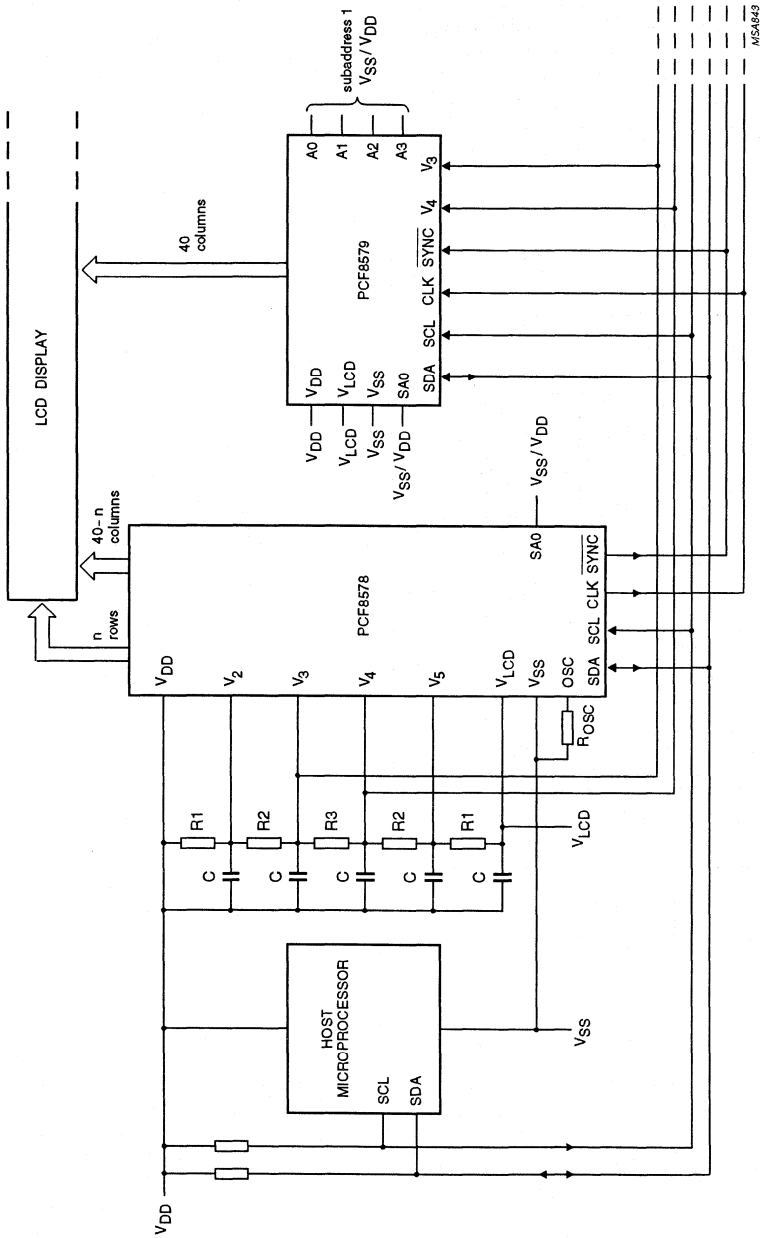


Fig.3 Typical mixed mode configuration.

Table 3 Multiplex rate for Fig.3.

RESISTORS	MULTIPLEX RATE (n)	
	n = 8	n = 16, 24, 32
R1	R	R
R2	$(\sqrt{n-2})$ R	R
R3	$(3-\sqrt{n})$ R	$(\sqrt{n-3})$ R

Power-on reset

At power-on the PCF8578 resets to a defined starting condition as follows:

1. Display blank
2. 1 : 32 multiplex rate, row mode
3. Start bank, 0 selected
4. Data pointer is set to X, Y address 0, 0
5. Character mode
6. Subaddress counter is set to 0
7. I^2C-bus interface is initialized.

Data transfers on the I^2C-bus should be avoided for 1 ms following power-on, to allow completion of the reset action.

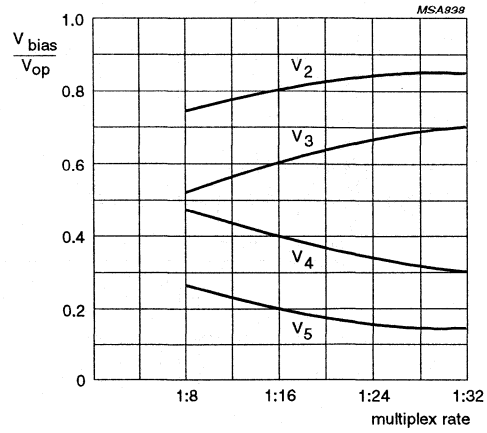


Fig.4 LCD bias voltages as a function of the multiplex rate.

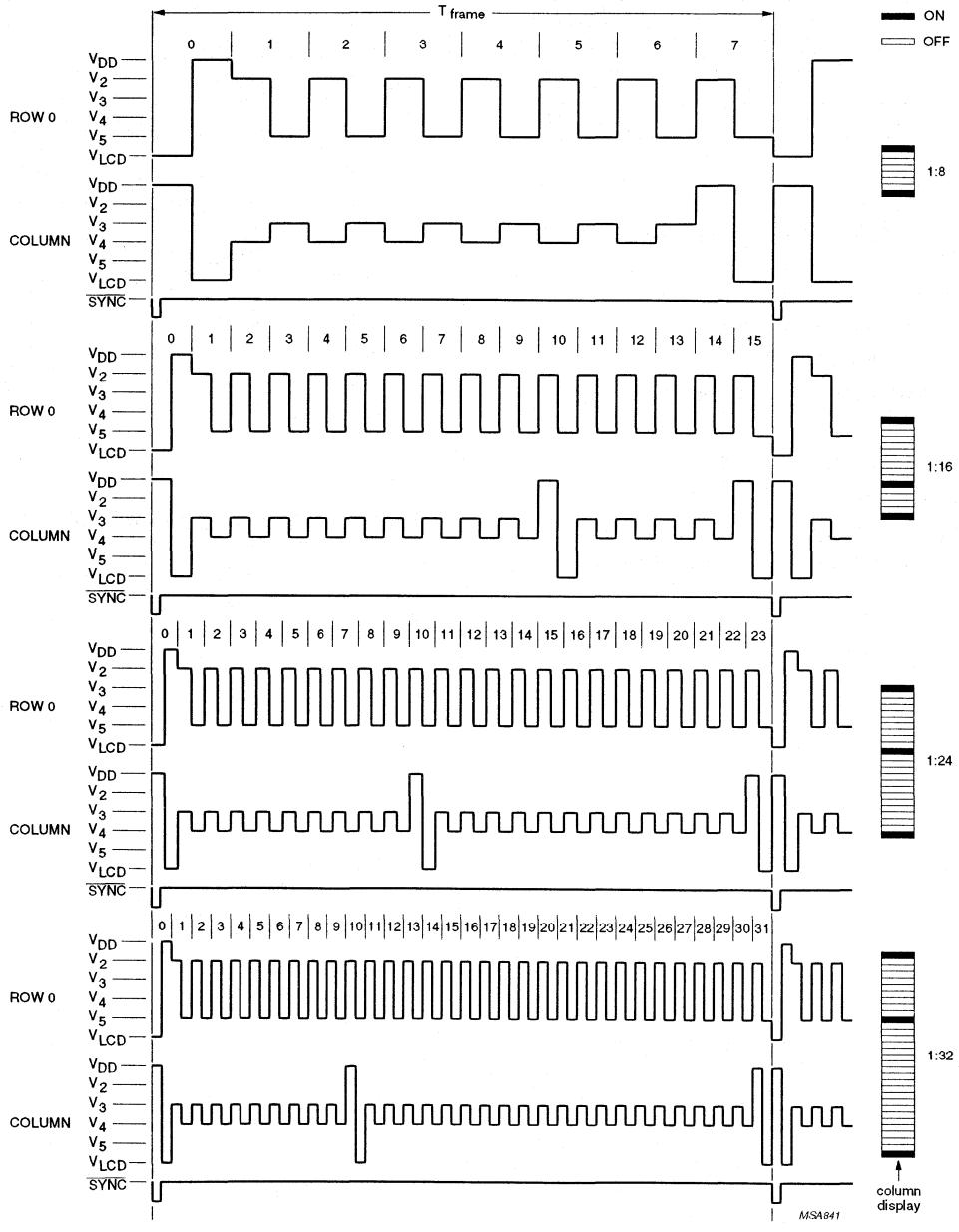
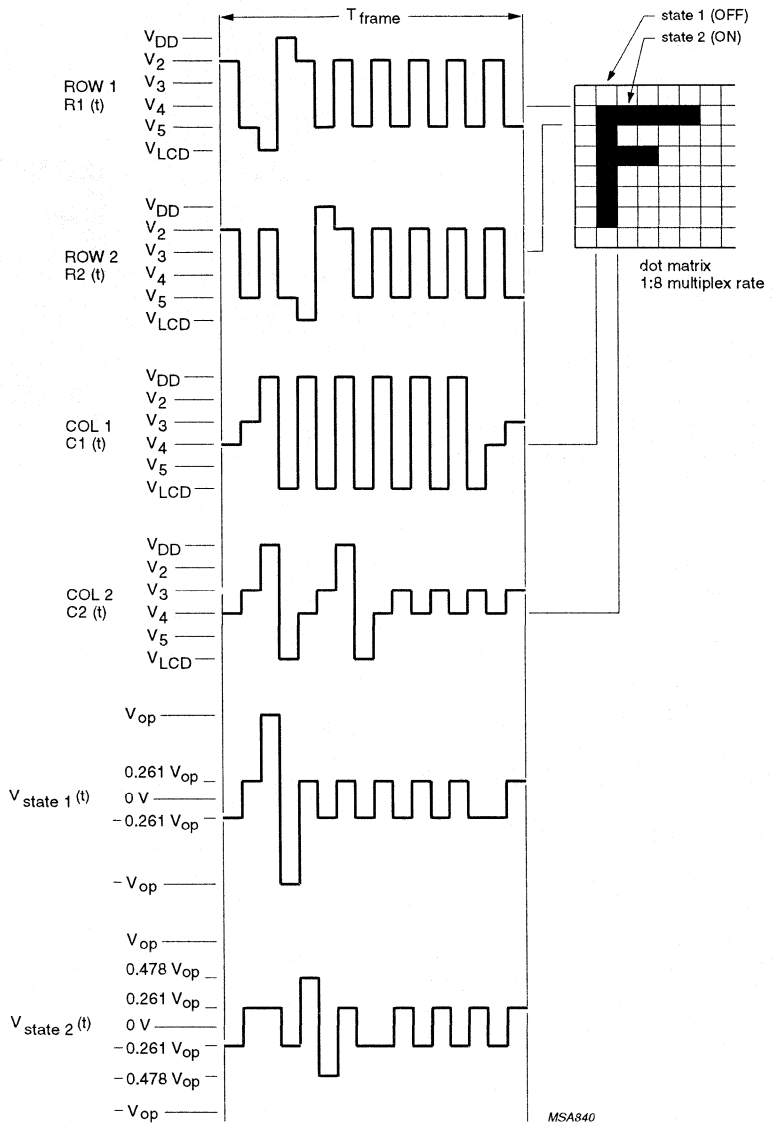


Fig.5 LCD row/column waveforms.



$V_{state\,1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{8} + \frac{\sqrt{8}-1}{8\,(\sqrt{8}+1)}} = 0.430$$

$V_{state\,2}(t) = C2(t) - R2(t)$:

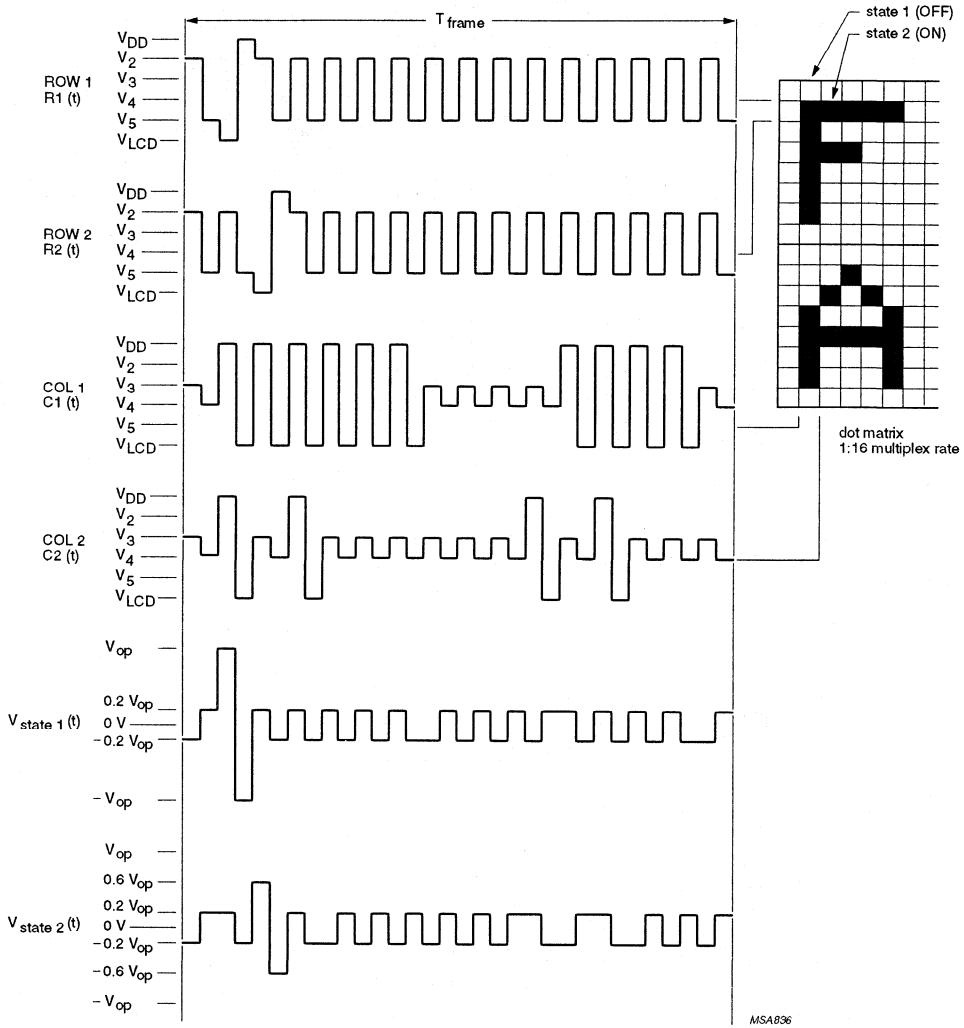
$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{8}-1)}{\sqrt{8}\,(\sqrt{8}+1)^2}} = 0.297$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n\,(\sqrt{n}+1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{n}-1)}{\sqrt{n}\,(\sqrt{n}+1)^2}}$$

Fig.6 LCD drive mode waveforms for 1 : 8 multiplex rate.



$V_{state\,1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{16} + \frac{\sqrt{16}-1}{16(\sqrt{16}+1)}} = 0.316$$

$V_{state\,2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{16}-1)}{\sqrt{16}(\sqrt{16}+1)^2}} = 0.254$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$$

Fig.7 LCD drive mode waveforms for 1 : 16 multiplex rate.

Internal clock

The clock signal for the system may be generated by the internal oscillator and prescaler. The frequency is determined by the value of the resistor R_{OSC}, see Fig.8. For normal use a value of 330 kΩ is recommended. The clock signal, for cascaded PCF8579s, is output at CLK and has a frequency $\frac{1}{6}$ (multiplex rate 1 : 8, 1 : 16 and 1 : 32) or $\frac{1}{8}$ (multiplex rate 1 : 24) of the oscillator frequency.

External clock

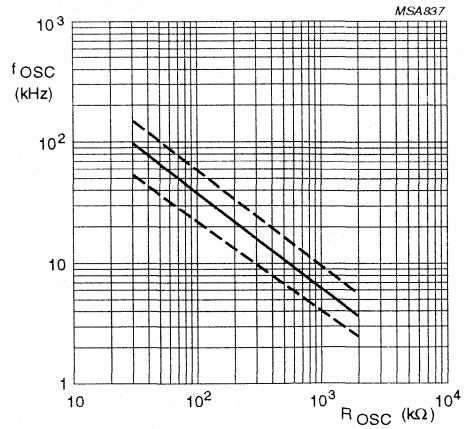
If an external clock is used, OSC must be connected to V_{DD} and the external clock signal to CLK. Table 4 summarizes the nominal CLK and $\overline{SYNC}$ frequencies.

Timing generator

The timing generator of the PCF8578 organizes the internal data flow of the device and generates the LCD frame synchronization pulse $\overline{SYNC}$, whose period is an integer multiple of the clock period. In cascaded applications, this signal maintains the correct timing relationship between the PCF8578 and PCF8579s in the system.

Row/column drivers

Outputs R0 to R7 and C32 to C39 are fixed as row and column drivers repectively. The remaining 24 outputs R8/C8 to R31/C31 are programmable and may be configured (in blocks of 8) to be either row or column drivers. The row select signal is produced sequentially at each output from R0 up to the number defined by the multiplex rate (see Table 1). In mixed mode the remaining outputs are configured as columns. In row mode all programmable outputs (R8/C8 to R31/C31) are defined as row drivers and the outputs C32 to C39 should be left open-circuit.



To avoid capacitive coupling, which could adversely affect oscillator stability, R_{OSC} should be placed as closely as possible to the OSC pin. If this proves to be a problem, a filtering capacitor may be connected in parallel to R_{OSC}.

Fig.8 Oscillator frequency as a function of R_{OSC}.

Using a 1 : 16 multiplex rate, two sets of row outputs are driven, thus facilitating split-screen configurations, i.e. a row select pulse appears simultaneously at R0 and R16/C16, R1 and R17/C17 etc. Similarly, using a multiplex rate of 1 : 8, four sets of row outputs are driven simultaneously. Driver outputs must be connected directly to the LCD. Unused outputs should be left open-circuit. In 1 : 8 R0 to R7 are rows; in 1 : 16 R0 to R15/C15 are rows; in 1 : 24 R0 to R23/C23 are rows; in 1 : 32 R0 to R31/C31 are rows.

Table 4 Signal frequencies required for nominal 64 Hz frame frequency; note 1.

OSCILLATOR FREQUENCY f_{OSC}[2] (Hz)	FRAME FREQUENCY $f_{\overline{SYNC}}$ (Hz)	MULTIPLEX RATE (n)	DIVISION RATIO	CLOCK FREQUENCY f_{CLK} (Hz)
12288	64	1 : 8, 1 : 16, 1 : 32	6	2048
12288	64	1 : 24	8	1536

Notes

1. A clock signal must always be present, otherwise the LCD may be frozen in a DC state.
2. R_{OSC} = 330 kΩ.

Display mode controller

The configuration of the outputs (row or column) and the selection of the appropriate driver waveforms are controlled by the display mode controller.

Display RAM

The PCF8578 contains a 32 x 40 bit static RAM which stores the display data. The RAM is divided into 4 banks of 40 bytes (4 x 8 x 40 bits). During RAM access, data is transferred to/from the RAM via the I²C-bus. The first eight columns of data (0 to 7) cannot be displayed but are available for general data storage and provide compatibility with the PCF8579. There is a direct correspondence between X-address and column output number.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows an individual data byte or a series of data bytes to be written into, or read from, the display RAM, controlled by commands sent on the I²C-bus.

Subaddress counter

The storage and retrieval of display data is dependent on the content of the subaddress counter. Storage takes place only when the contents of the subaddress counter agree with the hardware subaddress. The hardware subaddress of the PCF8578, valid in mixed mode only, is fixed at 0000.

I²C-bus controller

The I²C-bus controller detects the I²C-bus protocol, slave address, commands and display data bytes. It performs the conversion of the data input (serial-to-parallel) and the data output (parallel-to-serial). The PCF8578 acts as an I²C-bus slave transmitter/receiver in mixed mode, and as a slave receiver in row mode. A slave device cannot control bus communication.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

RAM access

RAM operations are only possible when the PCF8578 is in mixed mode.

In this event its hardware subaddress is internally fixed at 0000 and the hardware subaddresses of any PCF8579 used in conjunction with the PCF8578 must start at 0001.

There are three RAM ACCESS modes:

- Character
- Half-graphic
- Full-graphic.

These modes are specified by bits G1 to G0 of the RAM ACCESS command. The RAM ACCESS command controls the order in which data is written to or read from the RAM (see Fig.9).

To store RAM data, the user specifies the location into which the first byte will be loaded (see Fig.10):

- Device subaddress (specified by the DEVICE SELECT command)
- RAM X-address (specified by the LOAD X-ADDRESS command)
- RAM bank (specified by bits Y1 and Y0 of the RAM ACCESS command).

Subsequent data bytes will be written or read according to the chosen RAM ACCESS mode.
Device subaddresses are automatically incremented between devices until the last device is reached. If the last device has subaddress 15, further display data transfers will lead to a wrap-around of the subaddress to 0.

Display control

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD via the column outputs. The number of rows scanned depends on the multiplex rate set by bits M1 and M0 of the SET MODE command.

The display status (all dots on/off and normal/inverse video) is set by bits E1 and E0 of the SET MODE command. For bank switching, the RAM bank corresponding to the top of the display is set by bits B1 and B0 of the SET START BANK command. This is shown in Fig.11. This feature is useful when scrolling in alphanumeric applications.

TEST pin

The TEST pin must be connected to V_{SS}.

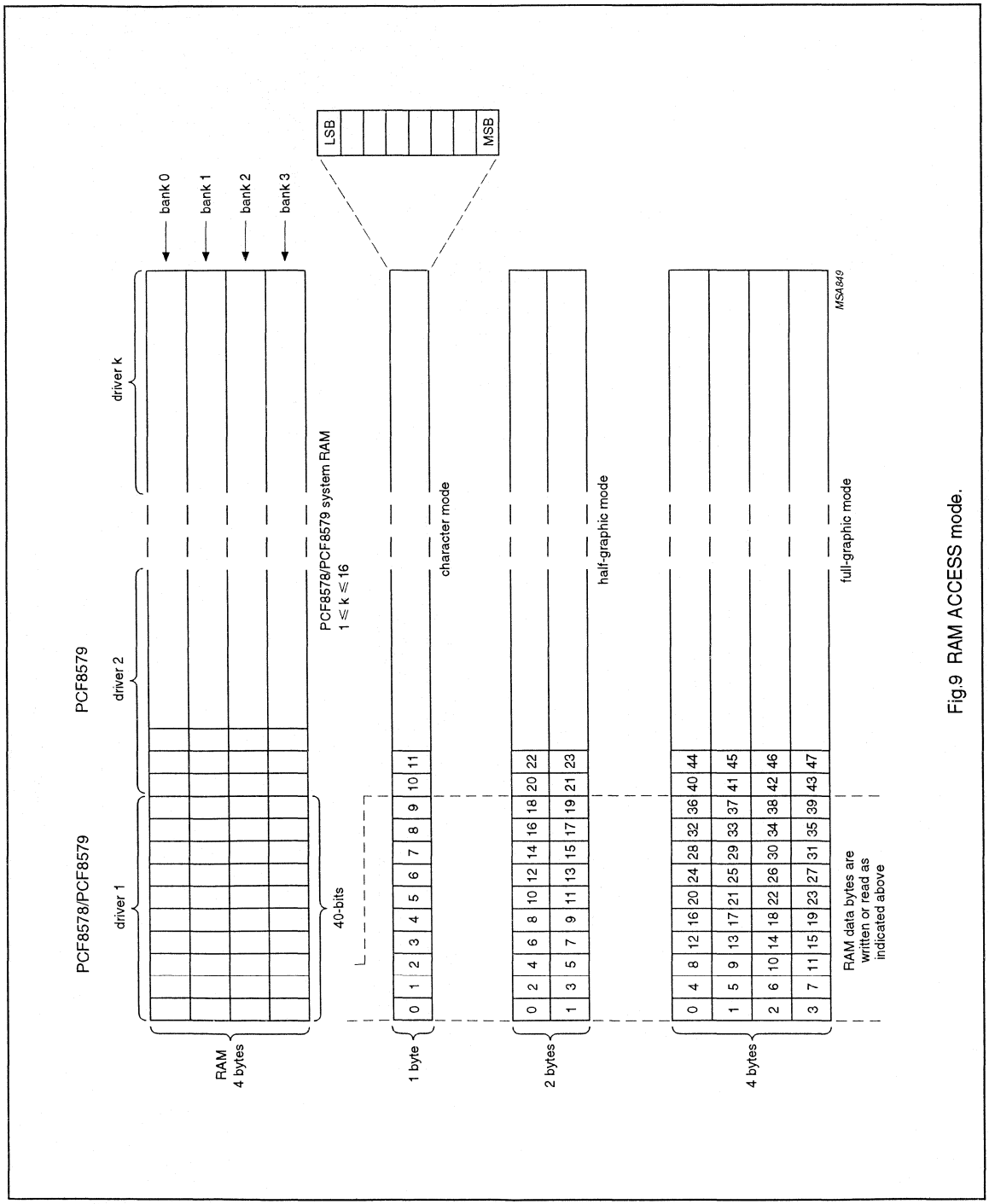


Fig.9 RAM ACCESS mode.

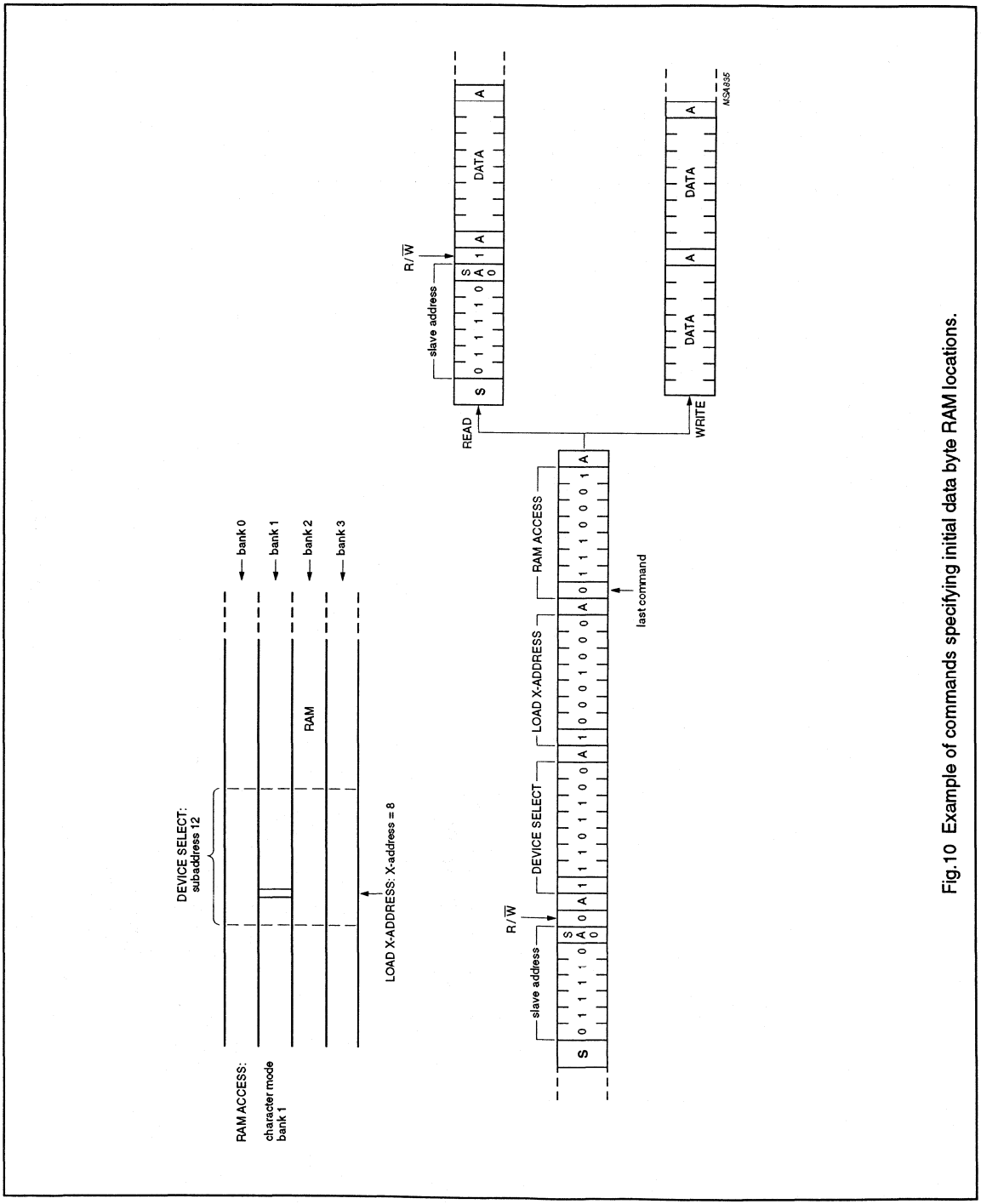


Fig.10 Example of commands specifying initial data byte RAM locations.

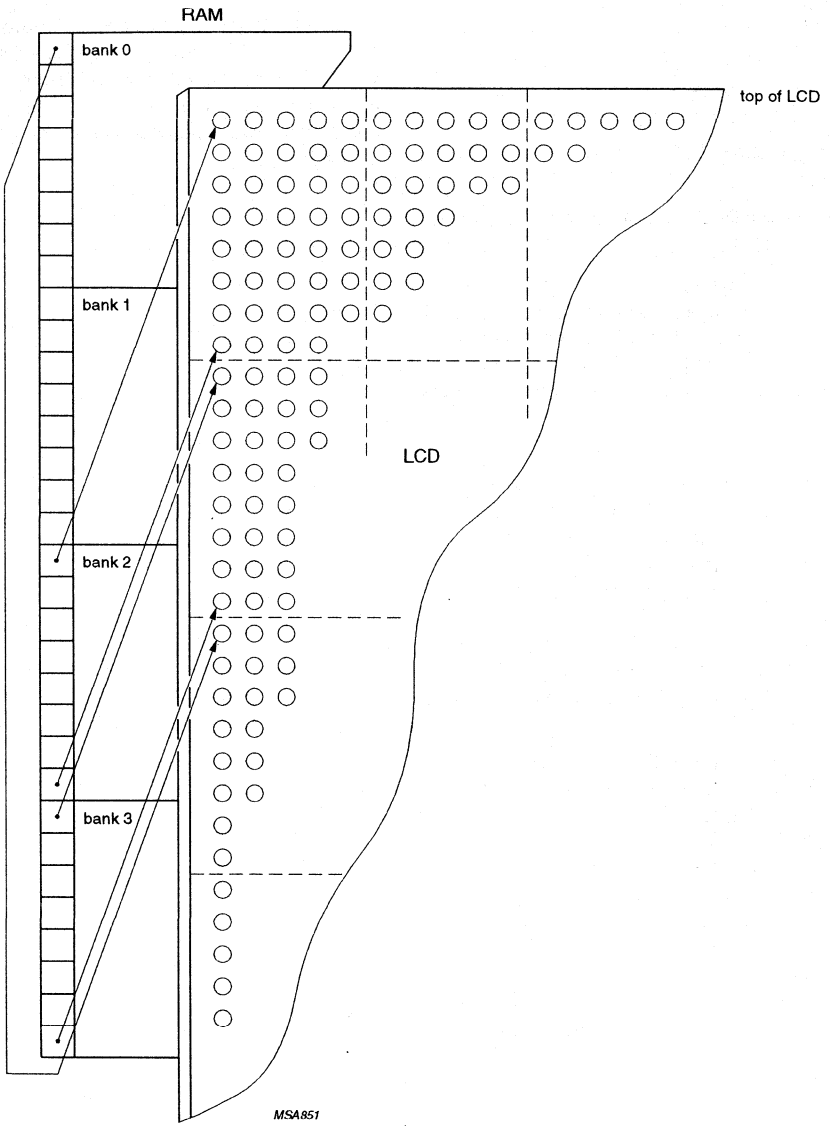


Fig.11 Relationship between display and SET START BANK; 1 : 32 multiplex rate and start bank = 2.

I²C-BUS PROTOCOL

Two 7-bit slave addresses (0111100 and 0111101) are reserved for both the PCF8578 and PCF8579. The least-significant bit of the slave address is set by connecting input SA0 to either 0 (V_{SS}) or 1 (V_{DD}). Therefore, two types of PCF8578 or PCF8579 can be distinguished on the same I²C-bus which allows:

1. One PCF8578 to operate with up to 32 PCF8579s on the same I²C-bus for very large applications.
2. The use of two types of LCD multiplex schemes on the same I²C-bus.

In most applications the PCF8578 will have the same slave address as the PCF8579.

The I²C-bus protocol is shown in Fig.12.
All communications are initiated with a start condition (S) from the I²C-bus master, which is followed by the desired slave address and read/write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

In WRITE mode (indicated by setting the read/write bit LOW) one or more commands follow the slave address acknowledgement. The commands are also acknowledged by all addressed devices on the bus. The last command must clear the continuation bit C. After the last command a series of data bytes may follow. The acknowledgement after each byte is made only by the (A0, A1, A2 and A3) addressed PCF8579 or PCF8578 with its implicit subaddress 0. After the last data byte has been acknowledged, the I²C-bus master issues a stop condition (P).

In READ mode, indicated by setting the read/write bit HIGH, data bytes may be read from the RAM following the slave address acknowledgement. After this acknowledgement the master transmitter becomes a master receiver and the PCF8578 becomes a slave transmitter. The master receiver must acknowledge the reception of each byte in turn. The master receiver must signal an end of data to the slave transmitter, by not generating an acknowledge on the last byte clocked out of the slave. The slave transmitter then leaves the data line HIGH, enabling the master to generate a stop condition (P).

Display bytes are written into, or read from, the RAM at the address specified by the data pointer and subaddress counter. Both the data pointer and subaddress counter are automatically incremented, enabling a stream of data to be transferred either to, or from, the intended devices.

In multiple device applications, the hardware subaddress pins of the PCF8579s (A0 to A3) are connected to V_{SS} or V_{DD} to represent the desired hardware subaddress code. If two or more devices share the same slave address, then each device **must** be allocated a unique hardware subaddress.

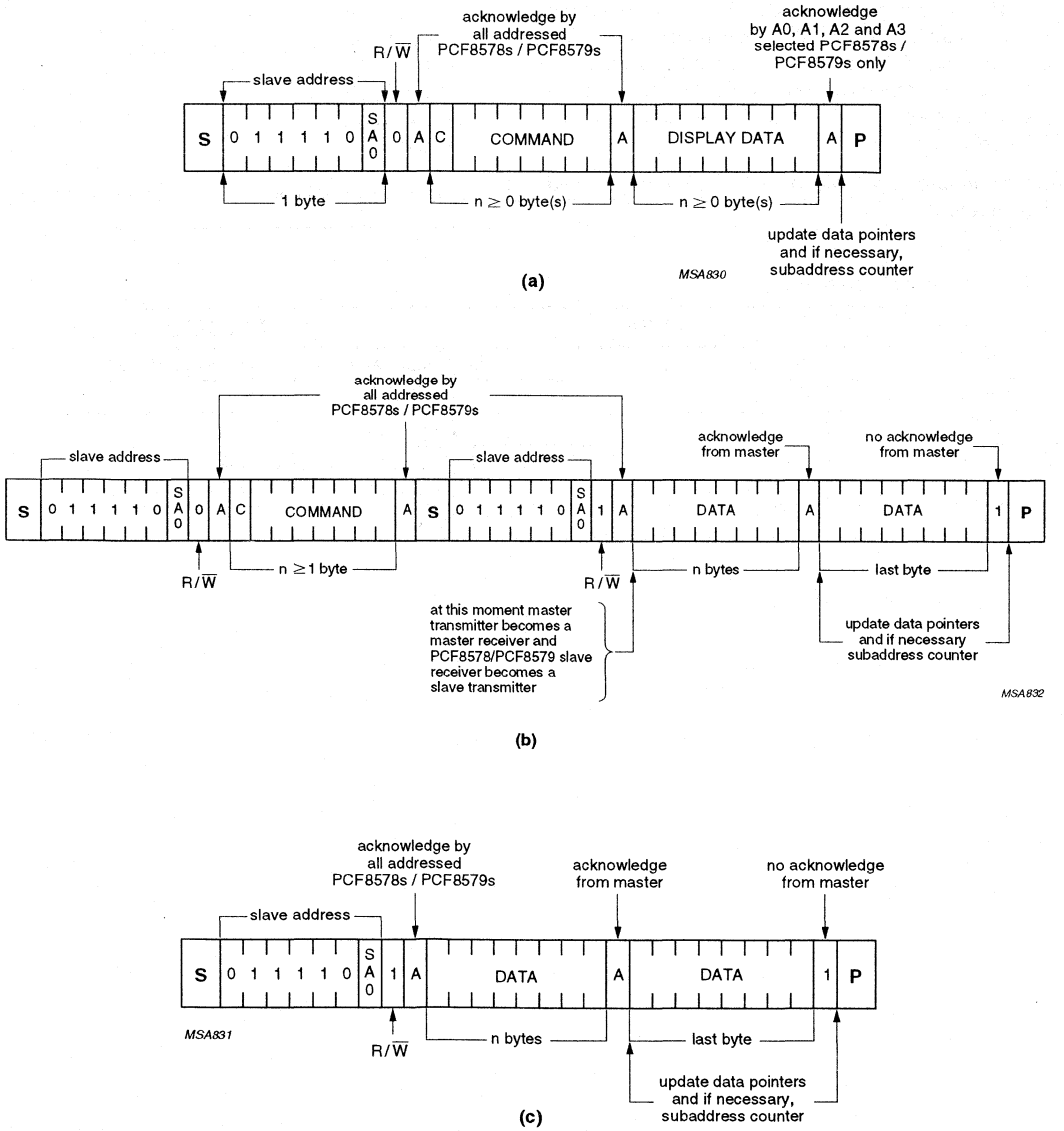
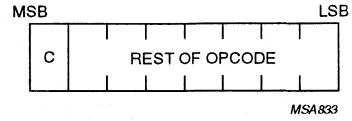


Fig.12 (a) Master transmits to slave receiver (WRITE mode); (b) Master reads after sending command string (WRITE commands; READ data); (c) Master reads slave immediately after sending slave address (READ mode).

Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. The most-significant bit of a command is the continuation bit C (see Fig.13). When this bit is set, it indicates that the next byte to be transferred will also be a command. If the bit is reset, it indicates the conclusion of the command transfer. Further bytes will be regarded as display data. Commands are transferred in WRITE mode only.

The five commands available to the PCF8578 are defined in Tables 5 and 6.



C = 0; last command.
C = 1; commands continue.

Fig.13 General information of command byte.

Table 5 Summary of commands.

COMMAND	OPCODE(1)								DESCRIPTION
SET MODE	C	1	0	D	D	D	D	D	multiplex rate, display status, system type
SET START BANK	C	1	1	1	1	1	D	D	defines bank at top of LCD
DEVICE SELECT	C	1	1	0	D	D	D	D	defines device subaddress
RAM ACCESS	C	1	1	1	D	D	D	D	graphic mode, bank select (D D D D ≥ 12 is not allowed; see SET START BANK opcode)
LOAD X-ADDRESS	C	0	D	D	D	D	D	D	0 to 39

Note

1. C = command continuation bit.
   D = may be a logic 1 or 0.

Table 6 Definition of PCF8578/PCF8579 commands.

COMMAND	OPCODE								OPTIONS	DESCRIPTION
SET MODE	C	1	0	T	E1	E0	M1	M0	see Table 7	defines LCD drive mode
									see Table 8	defines display status
									see Table 9	defines system type
SET START BANK	C	1	1	1	1	1	B1	B0	see Table 10	defines pointer to RAM bank corresponding to the top of the LCD; useful for scrolling, pseudo-motion and background preparation of new display
DEVICE SELECT	C	1	1	0	A3	A2	A1	A0	see Table 11	four bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of sixteen hardware subaddresses
RAM ACCESS	C	1	1	1	G1	G0	Y1	Y0	see Table 12	defines the auto-increment behaviour of the address for RAM access
									see Table 13	two bits of immediate data, bits Y0 to Y1, are transferred to the X-address pointer to define one of forty display RAM columns
LOAD X-ADDRESS	C	0	X5	X4	X3	X2	X1	X0	see Table 14	six bits of immediate data, bits X0 to X5, are transferred to the X-address pointer to define one of forty display RAM columns

Table 7 Set mode option 1.

LCD DRIVE MODE		BITS	
		M1	M0
1 : 8	MUX (8 rows)	0	1
1 : 16	MUX (16 rows)	1	0
1 : 24	MUX (24 rows)	1	1
1 : 32	MUX (32 rows)	0	0

Table 8 Set mode option 2.

DISPLAY STATUS	BITS	
	E1	E0
Blank	0	0
Normal	0	1
All segments on	1	0
Inverse video	1	1

Table 9 Set mode option 3.

SYSTEM TYPE	BIT T
PCF8578 row only	0
PCF8578 mixed mode	1

Table 10 Set start bank option 1.

START BANK POINTER	BITS	
	B1	B0
Bank 0	0	0
Bank 1	0	1
Bank 2	1	0
Bank 3	1	1

Table 11 Device select option 1.

DESCRIPTION	BITS			
Decimal value 0 to 15	A3	A2	A1	A0

Table 12 RAM access option 1.

RAM ACCESS MODE	BITS	
	G1	G0
Character	0	0
Half-graphic	0	1
Full-graphic	1	0
Not allowed (note 1)	1	1

Note

1. See opcode for SET START BANK in Table 6.

Table 13 Device select option 1.

DESCRIPTION	BITS	
Decimal value 0 to 3	Y1	Y0

Table 14 Device select option 1.

DESCRIPTION	BITS					
Decimal value 0 to 39	X5	X4	X3	X2	X1	X0

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL) which must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this moment will be interpreted as control signals.

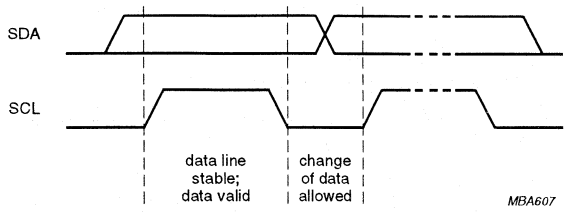


Fig.14 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

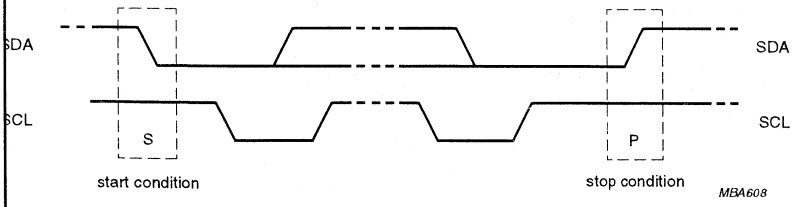


Fig.15 Definition of start and stop condition.

System configuration

A device transmitting a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message flow is the 'master' and the devices which are controlled by the master are the 'slaves'.

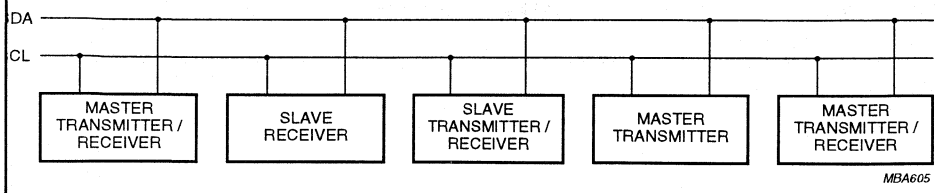
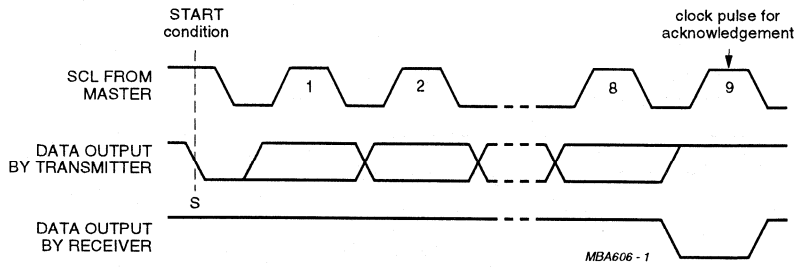


Fig.16 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal the end of a data transmission to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.



The general characteristics and detailed specification of the I²C-bus are available on request.

Fig.17 Acknowledgment on the I²C-bus.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+8.0	V
V_{LCD}	LCD supply voltage	V_{DD} − 11	V_{DD}	V
V_{I1}	input voltage SDA, SCL, CLK, TEST, SA0 and OSC	V_{SS} − 0.5	V_{DD} + 0.5	V
V_{I2}	input voltage V_2 to V_5	V_{LCD} − 0.5	V_{DD} + 0.5	V
V_{O1}	output voltage $\overline{SYNC}$ and CLK	V_{SS} − 0.5	V_{DD} + 0.5	V
V_{O2}	output voltage R0 to R7, R8/C8 to R31/C31 and C32 to C39	V_{LCD} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	−50	+50	mA
P_{tot}	power dissipation per package	−	400	mW
P_o	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices.

DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.5	–	6.0	V
V_{LCD}	LCD supply voltage		V_{DD} − 9	–	V_{DD} − 3.5	V
I_{DD1}	supply current external clock	f_{CLK} = 2 kHz; note 1	–	6	15	μA
I_{DD2}	supply current internal clock	R_{OSC} = 330 kΩ	–	20	50	μA
V_{POR}	power-on reset level	note 2	0.8	1.3	1.8	V
Logic						
V_{IL}	LOW level input voltage		V_{SS}	–	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD}	V
I_{OL1}	LOW level output current at $\overline{SYNC}$ and CLK	V_{OL} = 1 V; V_{DD} = 5 V	1	–	–	mA
I_{OH1}	HIGH level output current at $\overline{SYNC}$ and CLK	V_{OH} = 4 V; V_{DD} = 5 V	–	–	−1	mA
I_{OL2}	LOW level output current at SDA	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
I_{L1}	leakage current at SDA, SCL, $\overline{SYNC}$, CLK, TEST and SA0	V_I = V_{DD} or V_{SS}	–	–	+1	mA
I_{L2}	leakage current at OSC	V_I = V_{DD}	–	–	+1	μA
C_I	input capacitance at SCL and SDA	note 3	–	–	5	pF
LCD outputs						
I_{L3}	leakage current at V_2 to V_5	V_I = V_{DD} or V_{LCD}	−2	–	+2	μA
V_{DC}	DC component of LCD drivers R0 to R7, R8/C8 to R31/C31 and C32 to C39		–	±20	–	mV
R_{ROW}	output resistance R0 to R7 and R8/C8 to R31/C31	row mode; note 4	–	1.5	3	kΩ
R_{COL}	output resistance R8/C8 to R31/C31 and C32 to C39	column mode; note 4	–	3	6	kΩ

Notes

1. Outputs are open; inputs at V_{DD} or V_{SS}; I²C-bus inactive; external clock with 50% duty factor.
2. Resets all logic when V_{DD} < V_{POR}.
3. Periodically sampled; not 100% tested.
4. Resistance measured between output terminal (R0 to R7, R8/C8 to R31/C31 and C32 to C39) and bias input (V_2 to V_5, V_{DD} and V_{LCD}) when the specified current flows through one output under the following conditions (see Table 2):
   - V_{op} = V_{DD} − V_{LCD} = 9 V;
   - row mode, R0 to R7 and R8/C8 to R31/C31: $V_2 - V_{LCD} \geq 6.65$ V; $V_5 - V_{LCD} \leq 2.35$ V; I_{LOAD} = 150 μA;
   - column mode, R8/C8 to R31/C31 and C32 to C39: $V_3 - V_{LCD} \geq 4.70$ V; $V_4 - V_{LCD} \leq 4.30$ V; I_{LOAD} = 100 μA.

AC CHARACTERISTICS

All timing values are referenced to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{CLK1}	clock frequency at multiplex rates of 1 : 8, 1 : 16 and 1 : 32	R_{OSC} = 330 kΩ; V_{DD} = 6 V	1.2	2.1	3.3	kHz
f_{CLK2}	clock frequency at multiplex rates of 1 : 24	R_{OSC} = 330 kΩ; V_{DD} = 6 V	0.9	1.6	2.5	kHz
t_{PSYNC}	$\overline{SYNC}$ propagation delay		–	–	500	ns
t_{PLCD}	driver delays	V_{DD} − V_{LCD} = 9 V; with test loads	–	–	100	µs
I²C-bus						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SW}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	start condition set-up time	repeated start codes only	4.7	–	–	µs
$t_{HD;STA}$	start condition hold time		4.0	4.0	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	stop condition set-up time		4.0	–	–	µs

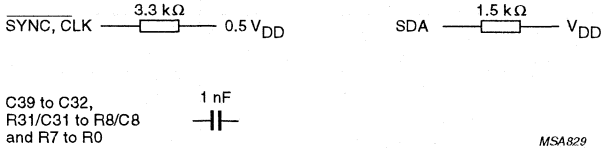


Fig.18 AC test loads.

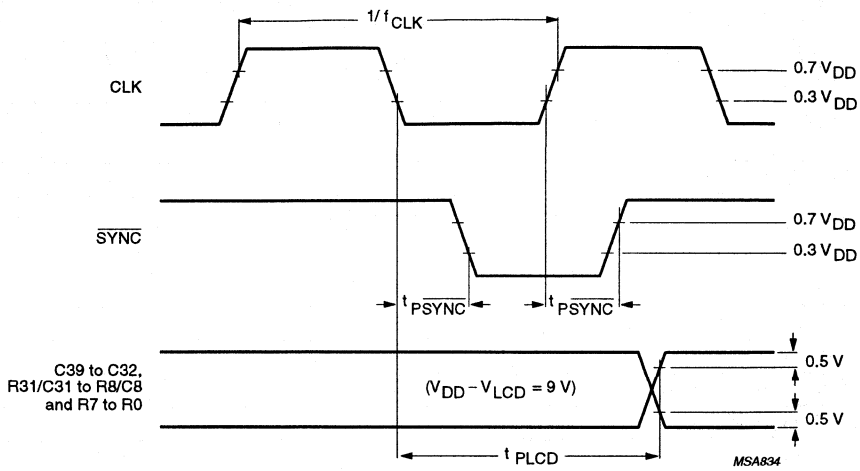


Fig.19 Driver timing waveforms.

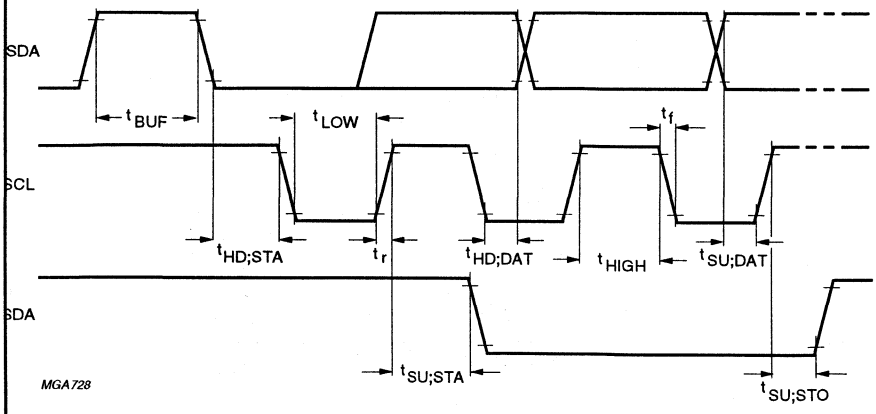


Fig.20 I²C-bus timing waveforms.

APPLICATION INFORMATION

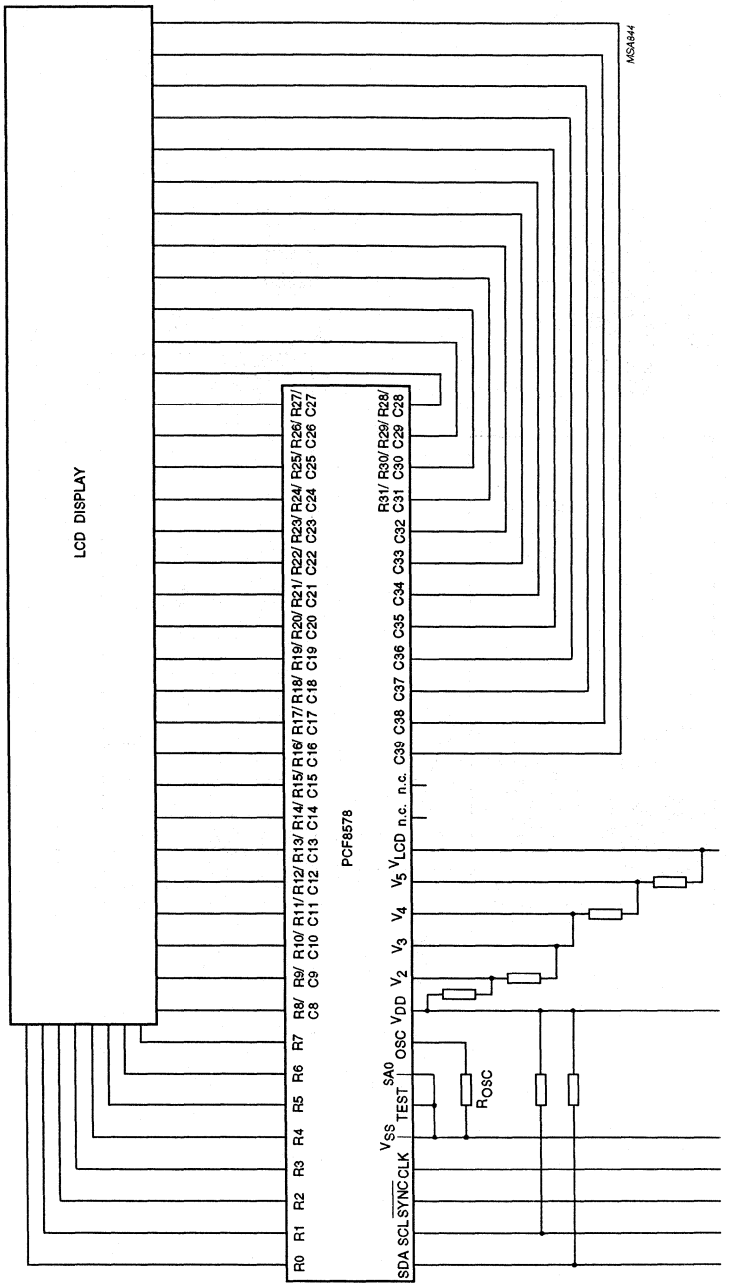


Fig.21 Stand-alone application using 8 rows and 32 columns.

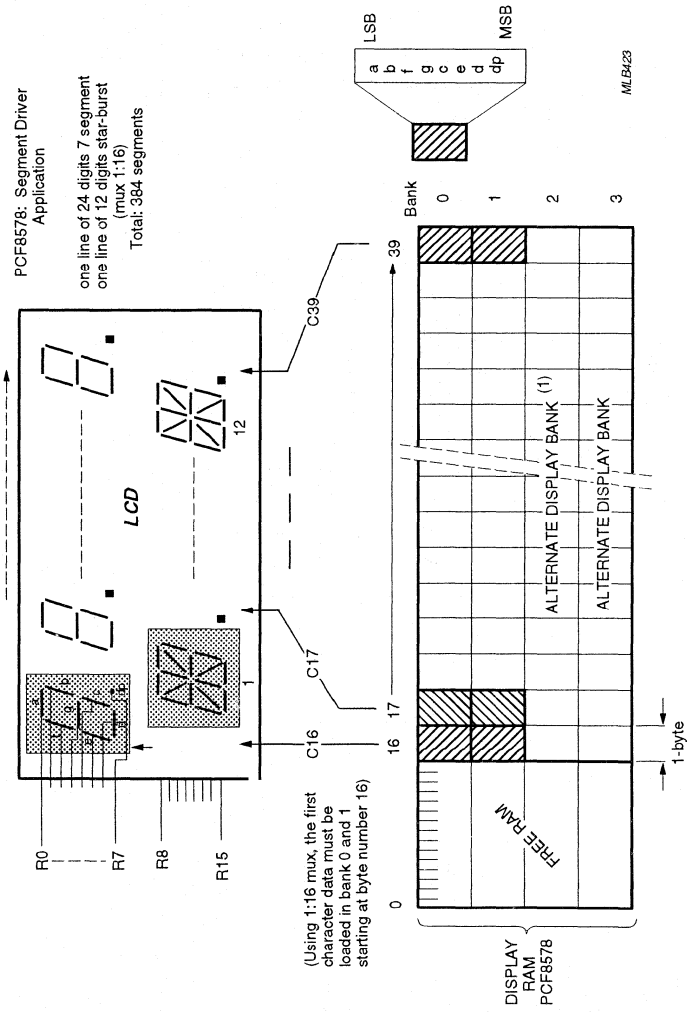


Fig.22 Segment driver application for up to 384 segments.

(1) Can be used for creating blinking characters.

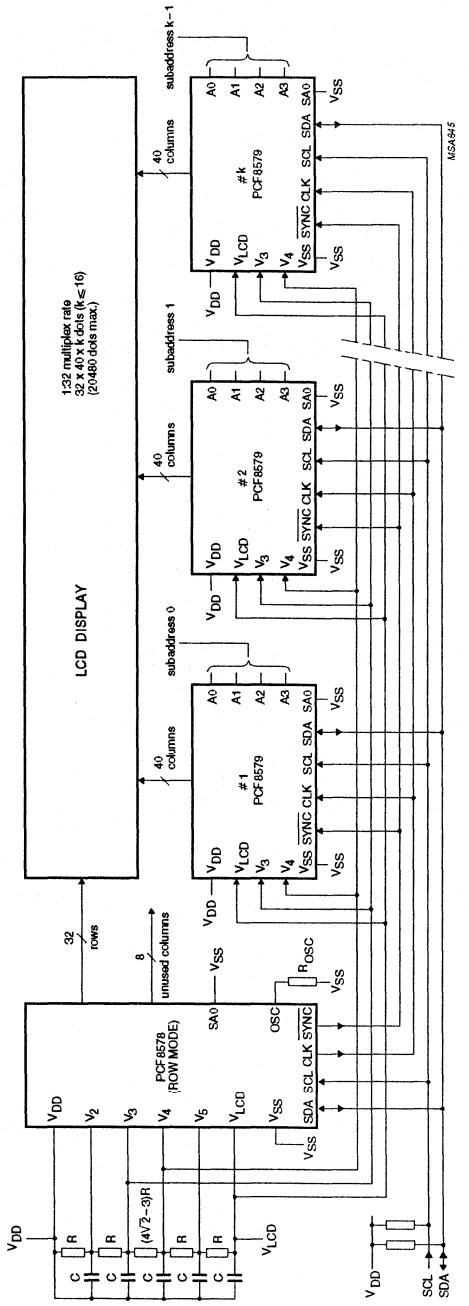


Fig.23 Typical LCD driver system with 1 : 32 multiplex rate.

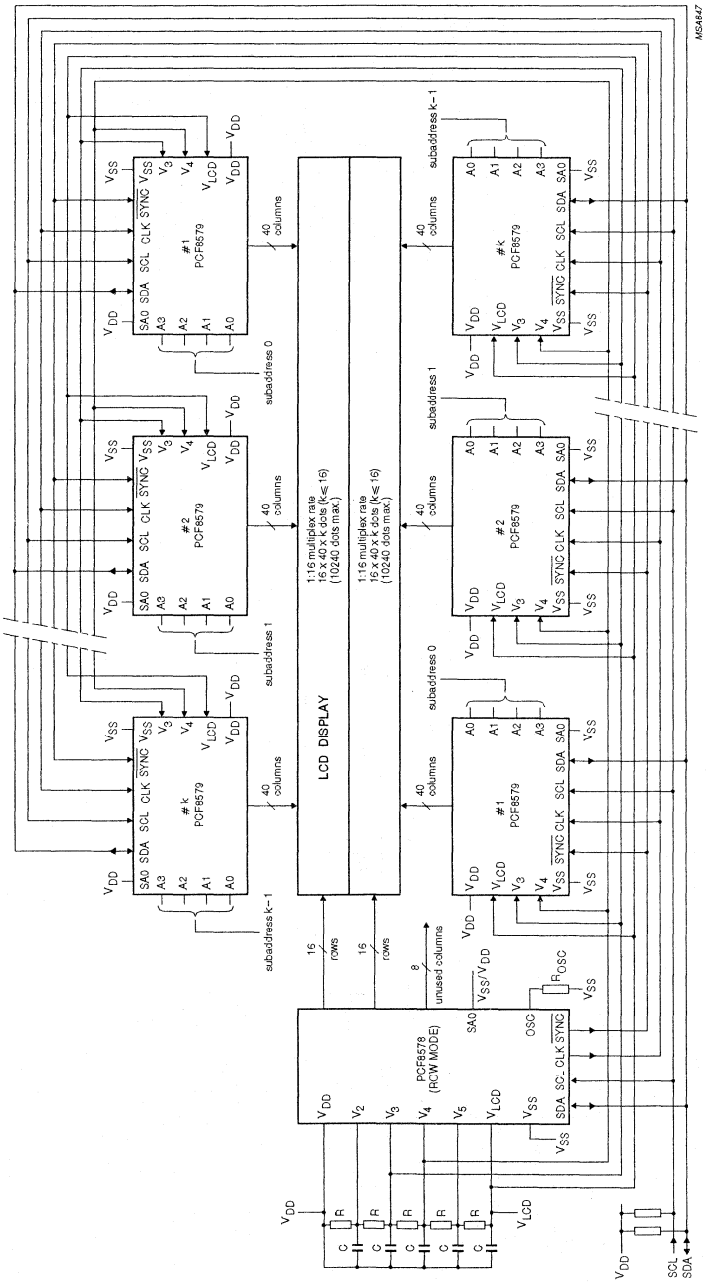


Fig.24 Split screen application with 1 : 16 multiplex rate for improved contrast.

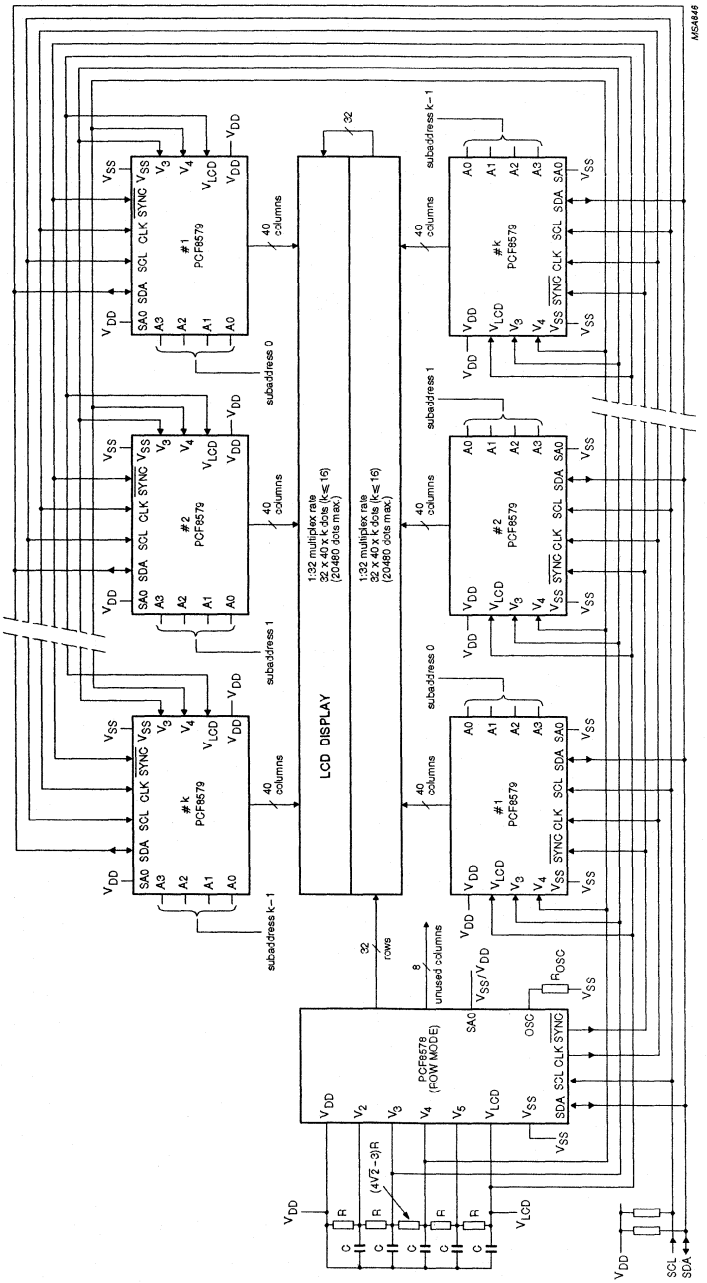


Fig.25 Split screen application with 1 : 32 multiplex rate.

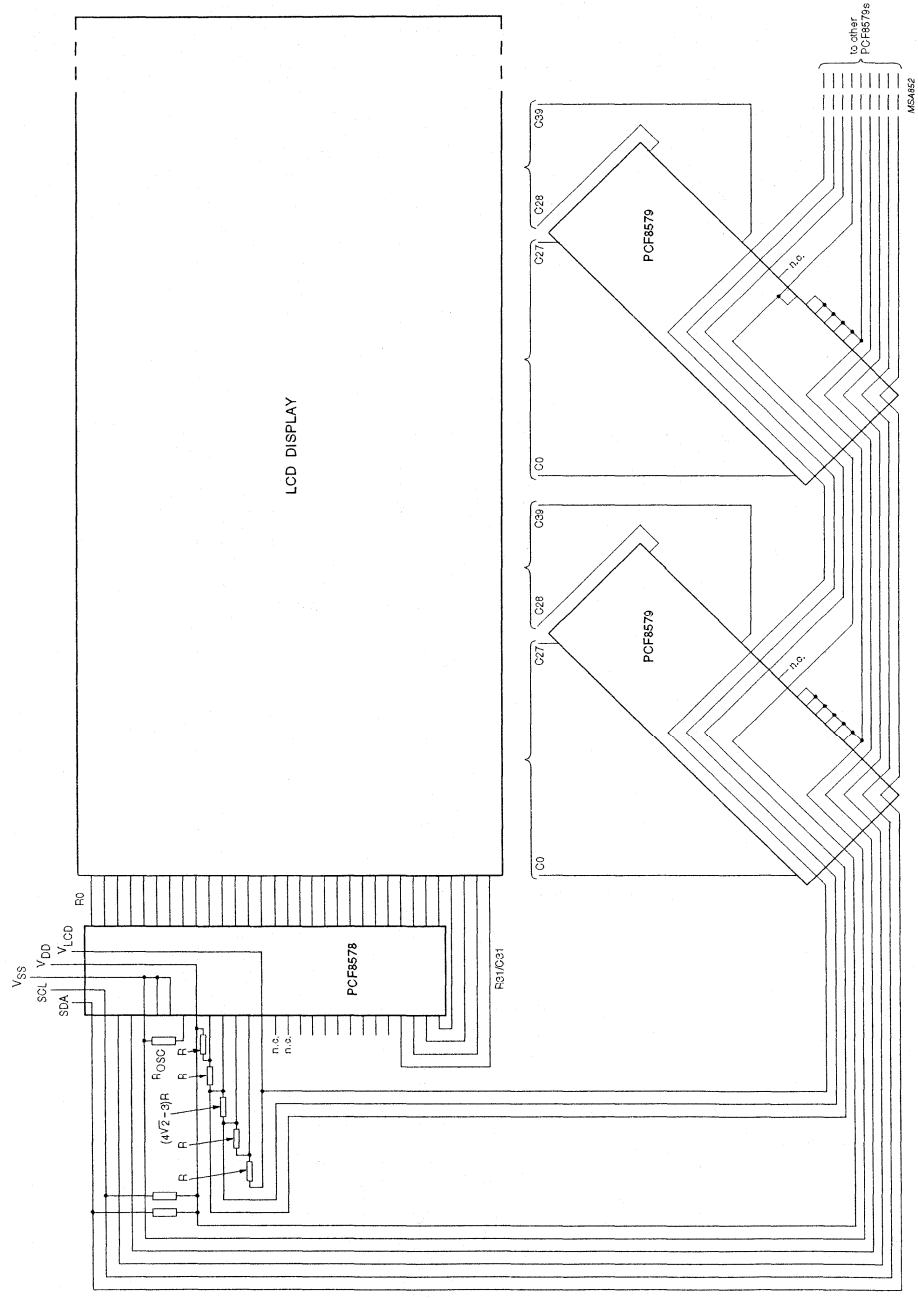
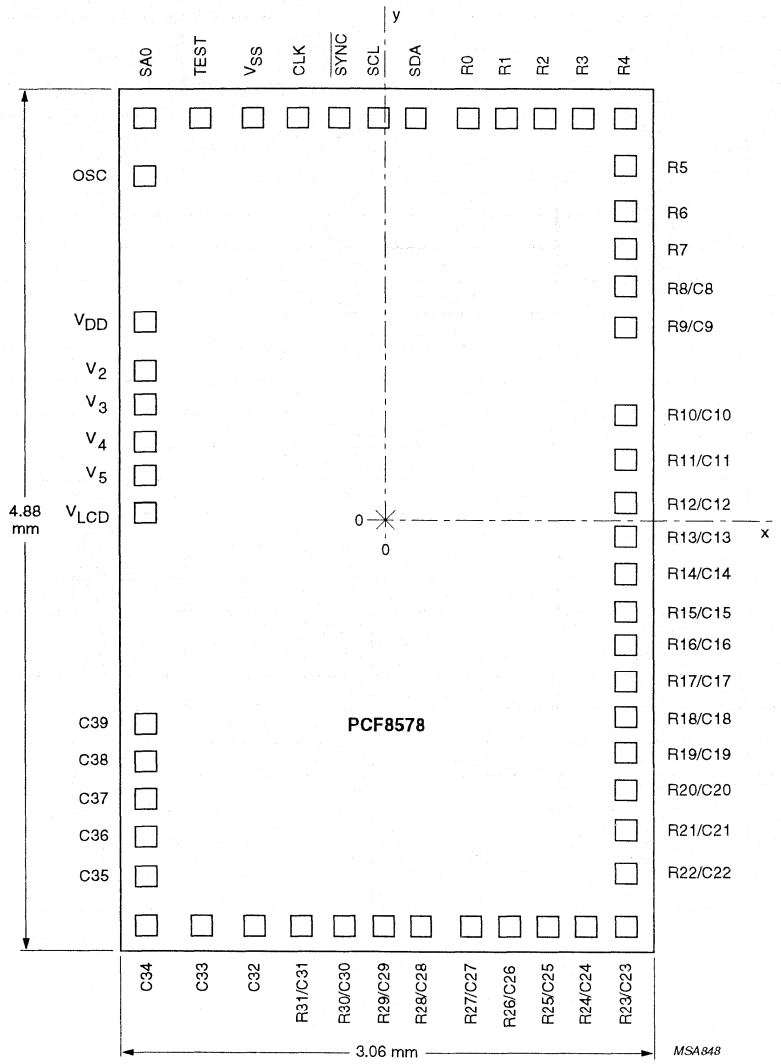


Fig.26 Example of single plane wiring, single screen with 1 : 32 multiplex rate (PCF8578 in row driver mode).

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



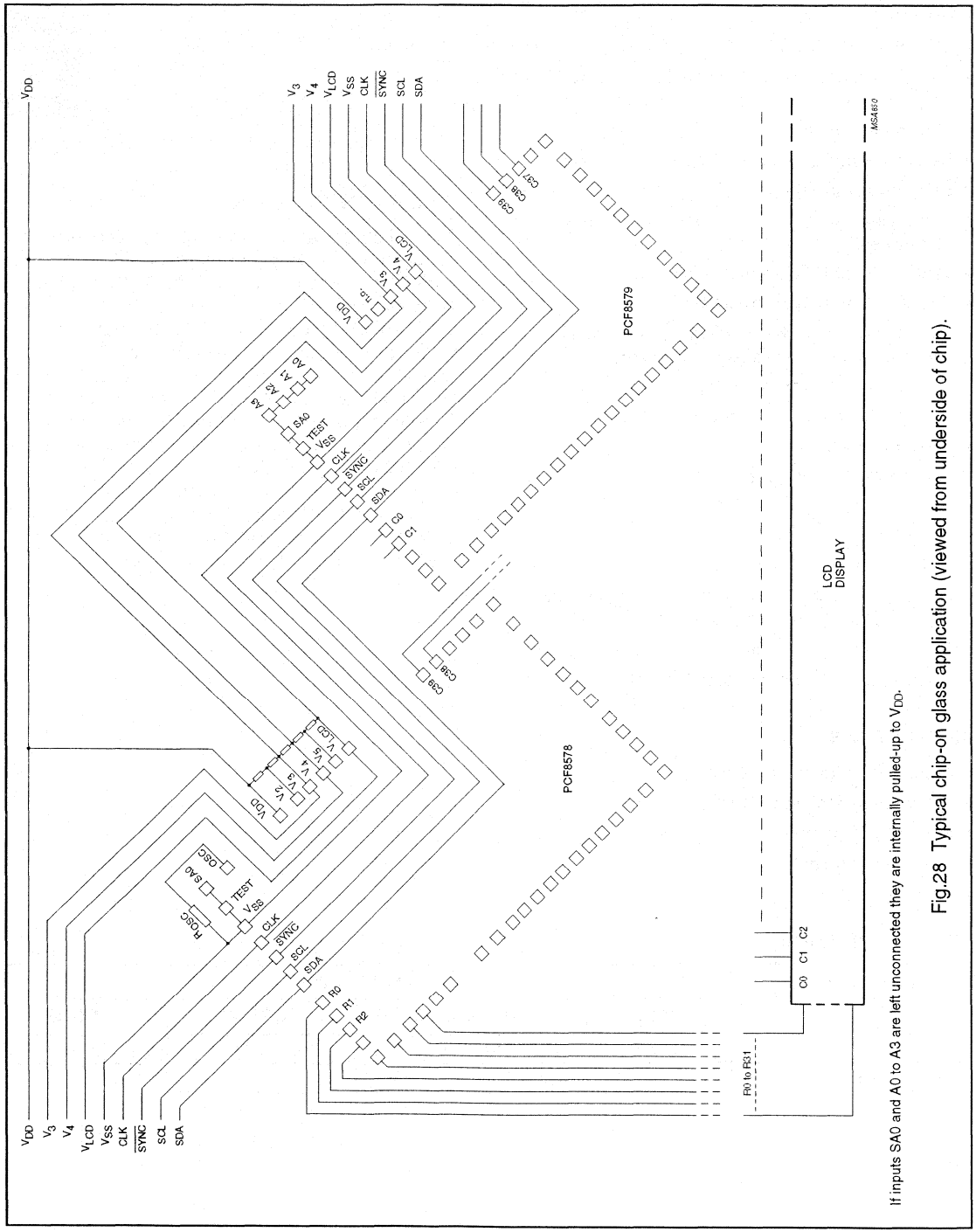
Chip area: 14.93 mm^2.
Bonding pad dimensions: 120 μm × 120 μm.

Fig.27 Bonding pad locations.

Table 15 Bonding pad locations (dimensions in μm).

All x/y coordinates are referenced to centre of chip, see Fig.27.

PAD	x	y	PAD	x	y
SDA	174	2241	R27/C27	468	−2241
SCL	−30	2241	R26/C26	672	−2241
$\overline{SYNC}$	−234	2241	R25/C25	876	−2241
CLK	−468	2241	R24/C24	1080	−2241
V_{SS}	726	2241	R23/C23	1308	−2241
TEST	−1014	2241	R22/C22	1308	−1977
SA0	−1308	2241	R21/C21	1308	−1731
OSC	−1308	1917	R20/C20	1308	−1515
V_{DD}	−1308	1113	R19/C19	1308	−1305
V_2	−1308	873	R18/C18	1308	−1101
V_3	−1308	663	R17/C17	1308	−897
V_4	−1308	459	R16/C16	1308	−693
V_5	−1308	255	R15/C15	1308	−489
V_{LCD}	−1308	51	R14/C14	1308	−285
n.c.	−	−	R13/C13	1308	−81
n.c.	−	−	R12/C12	1308	123
C39	−1308	−1149	R11/C11	1308	351
C38	−1308	−1353	R10/C10	1308	603
C37	−1308	−1557	R9/C9	1308	1101
C36	−1308	−1773	R8/C8	1308	1305
C35	−1308	−1995	R7	1308	1515
C34	−1308	−2241	R6	1308	1731
C33	−1014	−2241	R5	1308	1977
C32	−726	−2241	R4	1308	2241
R31/C31	−468	−2241	R3	1080	2241
R30/C30	−234	−2241	R2	876	2241
R29/C29	−30	−2241	R1	672	2241
R28/C28	174	−2241	R0	468	2241



If inputs SA0 and A0 to A3 are left unconnected they are internally pulled-up to V_{DD}.

Fig.28 Typical chip-on glass application (viewed from underside of chip).

CHIP-ON GLASS INFORMATION

LCD column driver for dot matrix graphic displays

PCF8579

FEATURES

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40960 dots
- 40 column outputs
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8578)
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8578)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

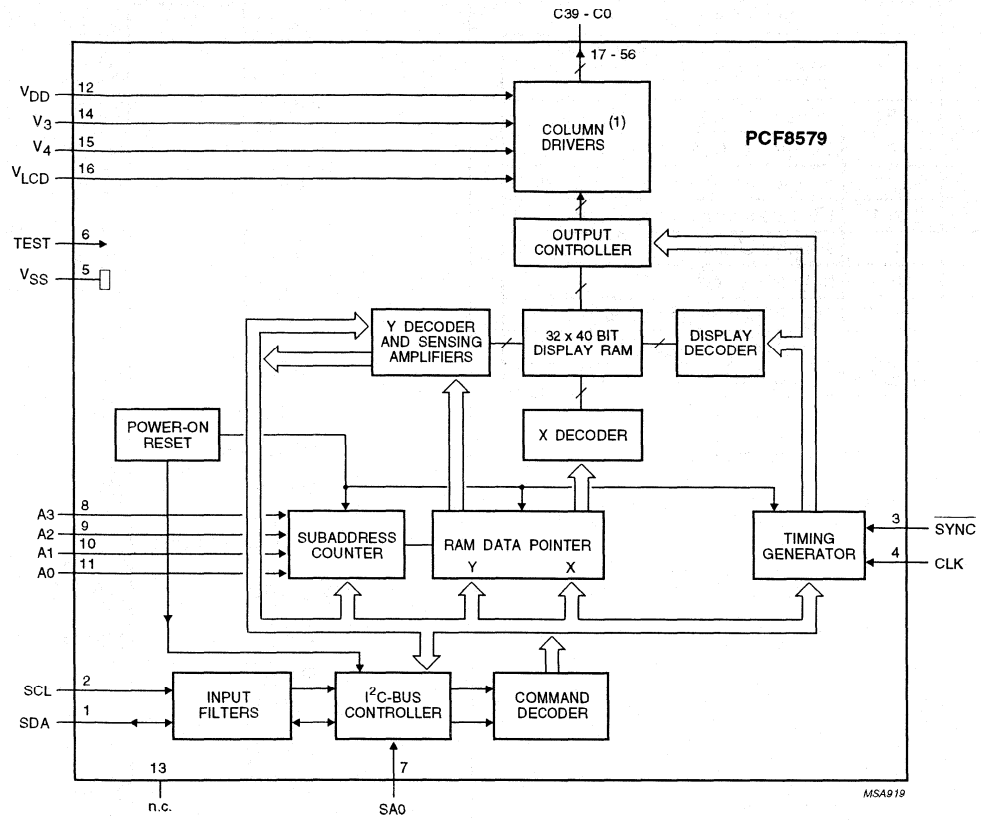
GENERAL DESCRIPTION

The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs and can drive 32 × 40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I²C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8579T	56	VSO56	plastic	SOT190
PCF8579U7	–	chip with bumps on-tape	–	–

BLOCK DIAGRAM



(1) LCD voltage levels, all other blocks operate at logic levels.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus serial data line
SCL	2	I²C-bus serial clock line
$\overline{SYNC}$	3	cascade synchronization input
CLK	4	external clock input
V_{SS}	5	ground (logic)
TEST	6	test pin (connect to V_{SS})
SA0	7	I²C-bus slave address input (bit 0)
A3 to A0	8 to 11	I²C-bus subaddress inputs
V_{DD}	12	supply voltage
n.c.	13(1)	not connected
V_3, V_4	14, 15	LCD bias voltage inputs
V_{LCD}	16	LCD supply voltage
C39 to C0	17 to 56	LCD column driver outputs

Note

1. Do not connect, this pin is reserved.

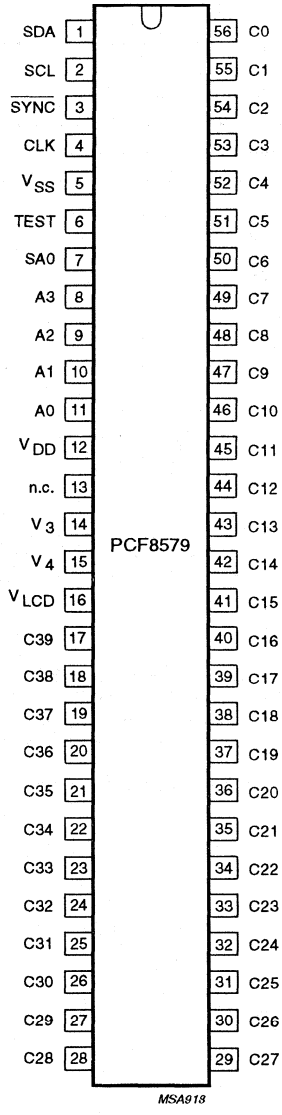


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The PCF8579 column driver is designed for use with the PCF8578. Together they form a general purpose LCD dot matrix chip set.

Typically up to 16 PCF8579s may be used with one PCF8578. Each of the PCF8579s is identified by a unique 4-bit hardware subaddress, set by pins A0 to A3. The PCF8578 can operate with up to 32 PCF8579s when using two I^2C-bus slave addresses. The two slave addresses are set by the logic level on input SA0.

Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the LCD threshold voltage (V_{th}). V_{th} is typically defined as the RMS voltage at which the LCD exhibits 10% contrast. Table 1 shows the optimum voltage bias levels for the PCF8578/PCF8579 chip set as functions of V_{op} ($V_{op} = V_{DD} - V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{op} is obtained by equating $V_{off(rms)}$ with V_{th}.

Table 1 Optimum LCD bias voltages.

PARAMETER	MULTIPLEX RATE			
	1 : 8	1 : 16	1 : 24	1 : 32
$\frac{V_2}{V_{op}}$	0.739	0.800	0.830	0.850
$\frac{V_3}{V_{op}}$	0.522	0.600	0.661	0.700
$\frac{V_4}{V_{op}}$	0.478	0.400	0.339	0.300
$\frac{V_5}{V_{op}}$	0.261	0.200	0.170	0.150
$\frac{V_{off(rms)}}{V_{op}}$	0.297	0.245	0.214	0.193
$\frac{V_{on(rms)}}{V_{op}}$	0.430	0.316	0.263	0.230
$D = \frac{V_{on(rms)}}{V_{off(rms)}}$	1.447	1.291	1.230	1.196
$\frac{V_{op}}{V_{th}}$	3.370	4.080	4.680	5.190

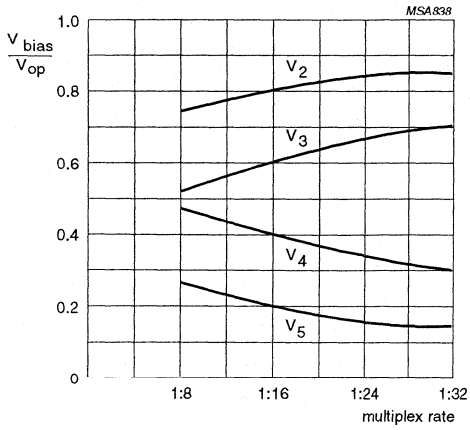


Fig.3 LCD bias voltages as a function of the multiplex rate.

Power-on reset

At power-on the PCF8579 resets to a defined starting condition as follows:

1. Display blank (in conjunction with PCF8578).
2. 1 : 32 multiplex rate.
3. Start bank, 0 selected.
4. Data pointer is set to X, Y address 0, 0.
5. Character mode.
6. Subaddress counter is set to 0.
7. I^2C-bus is initialized.

Data transfers on the I^2C-bus should be avoided for 1 ms following power-on, to allow completion of the reset action.

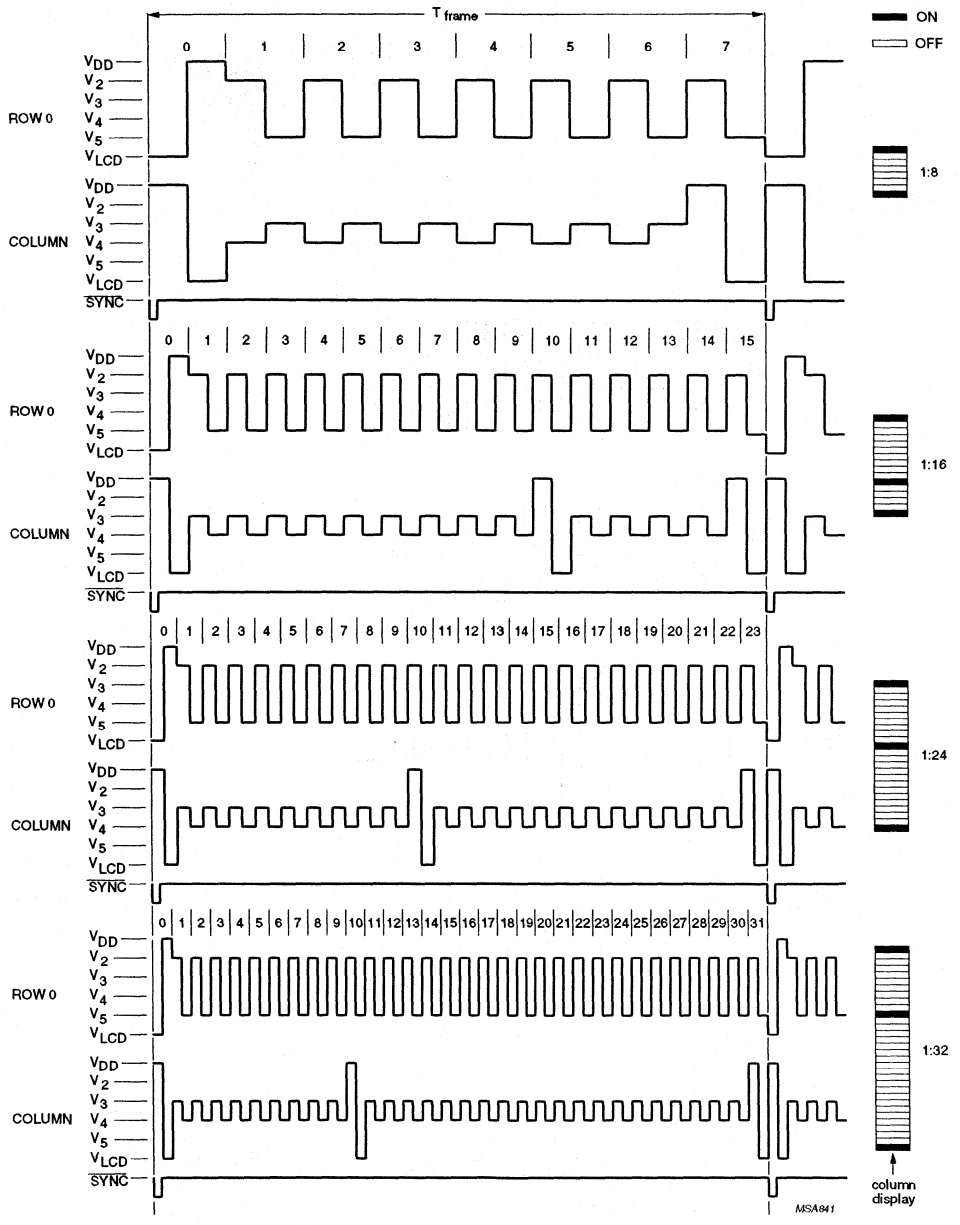
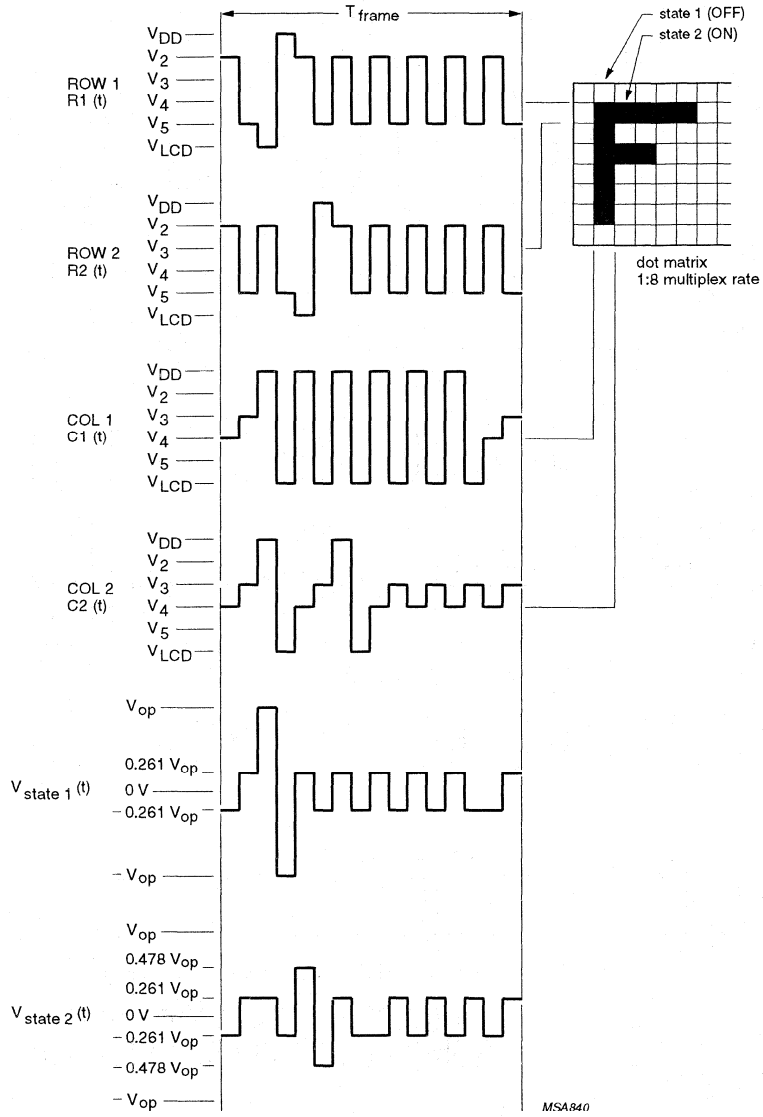


Fig.4 LCD row/column waveforms.



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{8} + \frac{\sqrt{8}-1}{8(\sqrt{8}+1)}} = 0.430$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

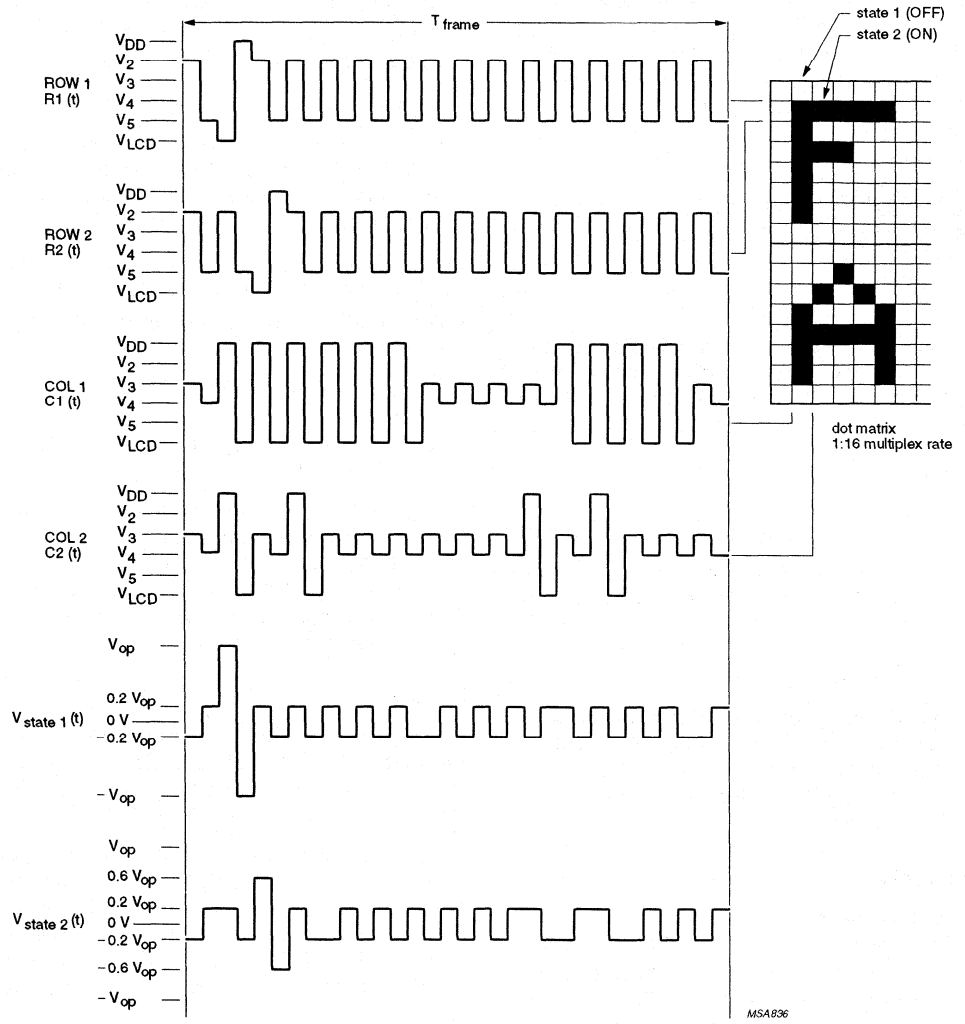
$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{8}-1)}{\sqrt{8}(\sqrt{8}+1)^2}} = 0.297$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$$

Fig.5 LCD drive mode waveforms for 1 : 8 multiplex rate.



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{16} + \frac{\sqrt{16}-1}{16(\sqrt{16}+1)}} = 0.316$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{16}-1)}{\sqrt{16}(\sqrt{16}+1)^2}} = 0.254$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$$

Fig.6 LCD drive mode waveforms for 1 : 16 multiplex rate.

Timing generator

The timing generator of the PCF8579 organizes the internal data flow from the RAM to the display drivers. An external synchronization pulse $\overline{SYNC}$ is received from the PCF8578. This signal maintains the correct timing relationship between cascaded devices.

Column drivers

Outputs C0 to C39 are column drivers which must be connected to the LCD. Unused outputs should be left open-circuit.

Display RAM

The PCF8579 contains a 32 × 40 bit static RAM which stores the display data. The RAM is divided into 4 banks of 40 bytes (4 × 8 × 40 bits). During RAM access, data is transferred to/from the RAM via the I²C-bus.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows an individual data byte or a series of data bytes to be written into, or read from, the display RAM, controlled by commands sent on the I²C-bus.

Subaddress counter

The storage and retrieval of display data is dependent on the content of the subaddress counter. Storage and retrieval take place only when the contents of the subaddress counter agree with the hardware subaddress at pins A0, A1, A2 and A3.

I²C-bus controller

The I²C-bus controller detects the I²C-bus protocol, slave address, commands and display data bytes. It performs the conversion of the data input (serial-to-parallel) and the data output (parallel-to-serial). The PCF8579 acts as an I²C-bus slave transmitter/receiver. Device selection depends on the I²C-bus slave address, the hardware subaddress and the commands transmitted.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

RAM access

There are three RAM ACCESS modes:

- Character
- Half-graphic
- Full-graphic.

These modes are specified by bits G1 and G0 of the RAM ACCESS command. The RAM ACCESS command controls the order in which data is written to or read from the RAM (see Fig.7).

To store RAM data, the user specifies the location into which the first byte will be loaded (see Fig.8):

- Device subaddress (specified by the DEVICE SELECT command)
- RAM X-address (specified by the LOAD X-ADDRESS command)
- RAM bank (specified by bits Y1 and Y0 of the RAM ACCESS command).

Subsequent data bytes will be written or read according to the chosen RAM access mode. Device subaddresses are automatically incremented between devices until the last device is reached. If the last device has subaddress 15, further display data transfers will lead to a wrap-around of the subaddress to 0.

Display control

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD via the column outputs. The number of rows scanned depends on the multiplex rate set by bits M1 and M0 of the SET MODE command.

The display status (all dots on/off and normal/inverse video) is set by bits E1 and E0 of the SET MODE command. For bank switching, the RAM bank corresponding to the top of the display is set by bits B1 and B0 of the SET START BANK command. This is shown in Fig.9 This feature is useful when scrolling in alphanumeric applications.

TEST pin

The TEST pin must be connected to V_{SS}.

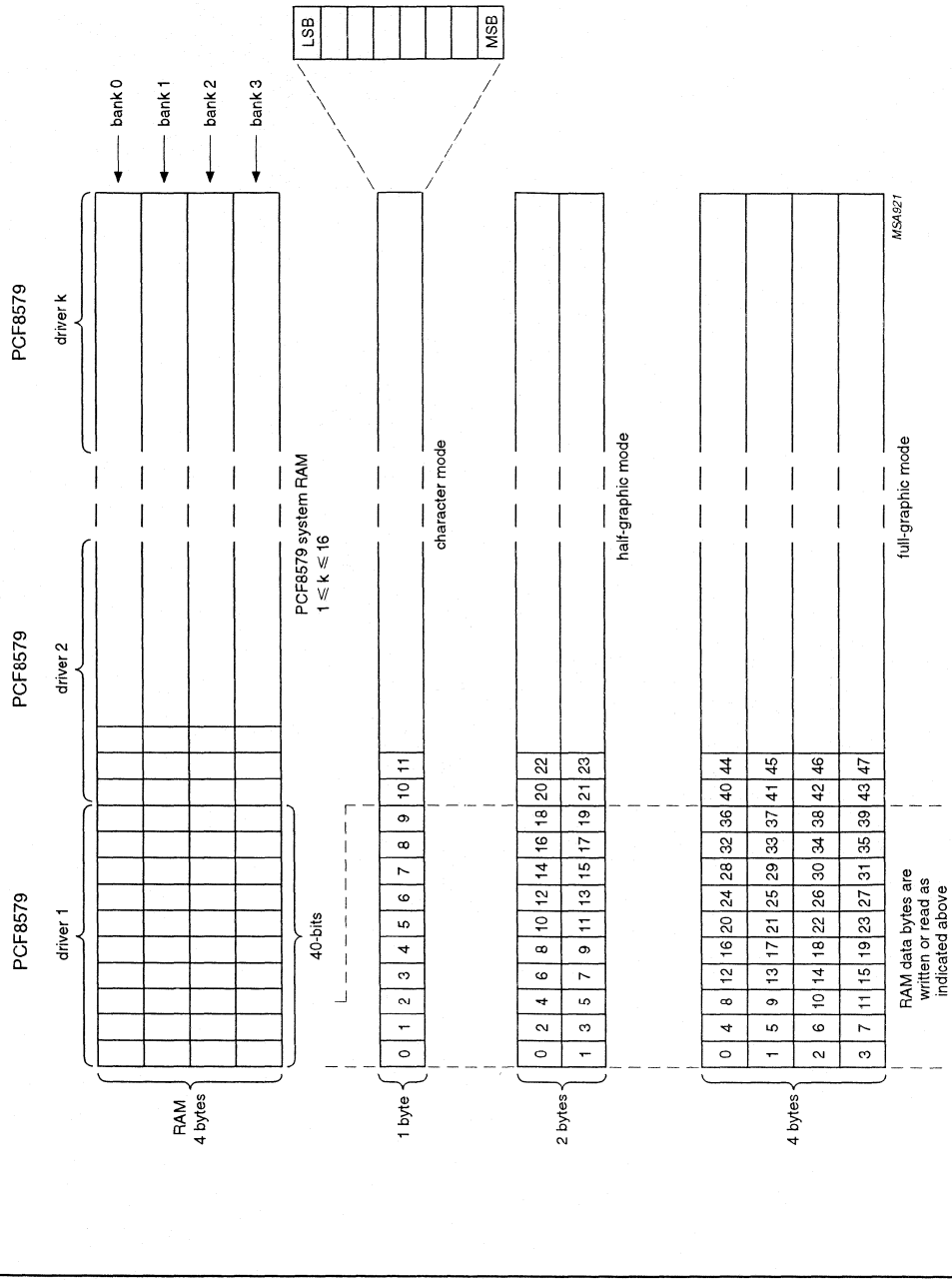


Fig.7 RAM access mode.

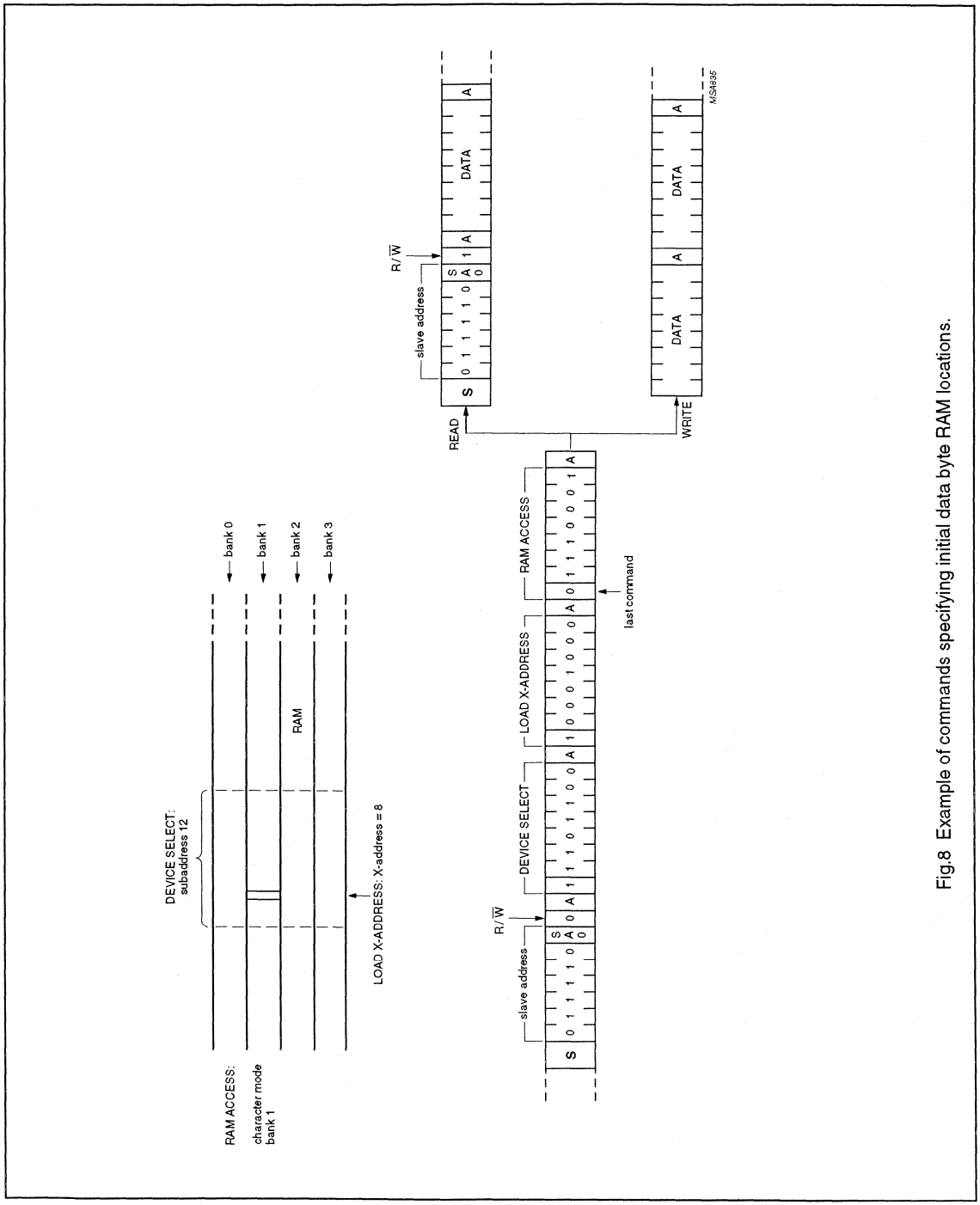


Fig.8 Example of commands specifying initial data byte RAM locations.

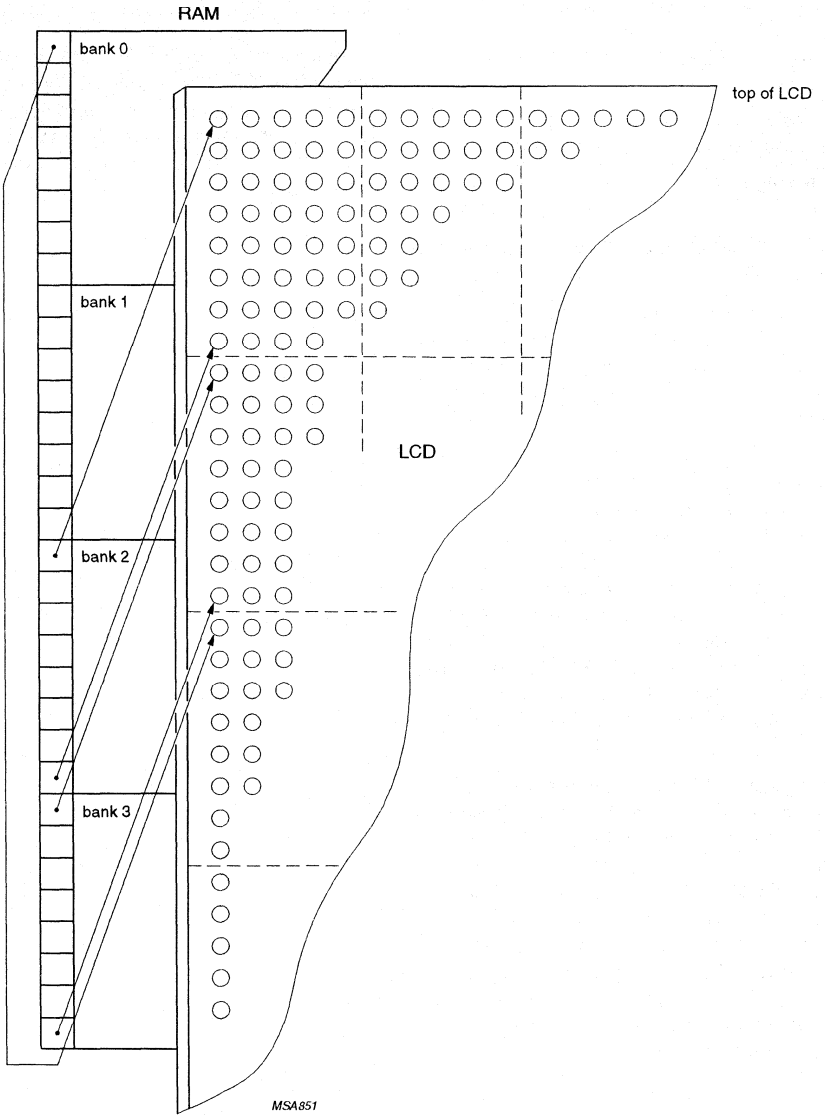


Fig.9 Relationship between display and SET START BANK; 1 : 32 multiplex rate and start bank = 2.

I²C-BUS PROTOCOL

Two 7-bit slave addresses (0111100 and 0111101) are reserved for both the PCF8578 and PCF8579. The least-significant bit of the slave address is set by connecting input SA0 to either 0 (V_{SS}) or 1 (V_{DD}). Therefore, two types of PCF8578 or PCF8579 can be distinguished on the same I²C-bus which allows:

1. One PCF8578 to operate with up to 32 PCF8579s on the same I²C-bus for very large applications.
2. The use of two types of LCD multiplex schemes on the same I²C-bus.

In most applications the PCF8578 will have the same slave address as the PCF8579.

The I²C-bus protocol is shown in Fig.10. All communications are initiated with a start condition (S) from the I²C-bus master, which is followed by the desired slave address and read/write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

In WRITE mode (indicated by setting the read/write bit LOW) one or more commands follow the slave address acknowledgement. The commands are also acknowledged by all addressed devices on the bus. The last command must clear the continuation bit C. After the last command a series of data bytes may follow. The acknowledgement after each byte is made only by the (A0, A1, A2 and A3) addressed PCF8579 or PCF8578 with its implicit subaddress 0. After the last data byte has been acknowledged, the I²C-bus master issues a stop condition (P).

In READ mode, indicated by setting the read/write bit HIGH, data bytes may be read from the RAM following the slave address acknowledgement. After this acknowledgement the master transmitter becomes a master receiver and the PCF8579 becomes a slave transmitter. The master receiver must acknowledge the reception of each byte in turn. The master receiver must signal an end of data to the slave transmitter, by **not** generating an acknowledge on the last byte clocked out of the slave. The slave transmitter then leaves the data line HIGH, enabling the master to generate a stop condition (P).

Display bytes are written into, or read from, the RAM at the address specified by the data pointer and subaddress counter. Both the data pointer and subaddress counter are automatically incremented, enabling a stream of data to be transferred either to, or from, the intended devices.

In multiple device applications, the hardware subaddress pins of the PCF8579s (A0 to A3) are connected to V_{SS} or V_{DD} to represent the desired hardware subaddress code. If two or more devices share the same slave address, then each device **must** be allocated a unique hardware subaddress.

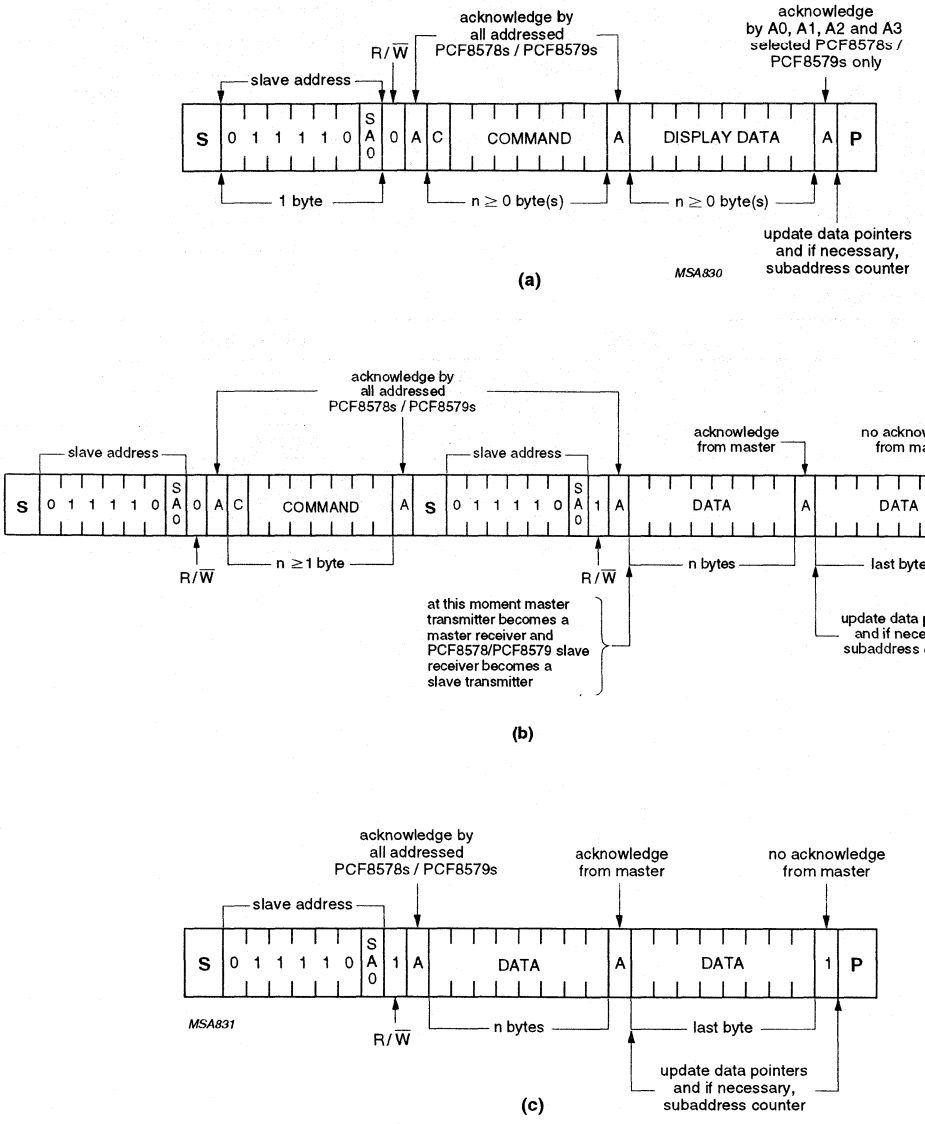
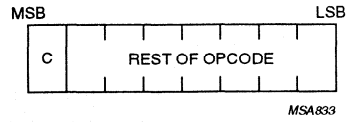


Fig.10 (a) Master transmits to slave receiver (WRITE mode); (b) Master reads after sending command string (WRITE commands; READ data); (c) Master reads slave immediately after sending slave address (READ mode).

Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. The most-significant bit of a command is the continuation bit C (see Fig.11). When this bit is set, it indicates that the next byte to be transferred will also be a command. If the bit is reset, it indicates the conclusion of the command transfer. Further bytes will be regarded as display data. Commands are transferred in WRITE mode only.

The five commands available to the PCF8579 are defined in Tables 2 and 3.



C = 0; last command.
C = 1; commands continue.

Fig.11 General format of command byte.

Table 2 Summary of commands.

COMMAND	OPCODE(1)								DESCRIPTION
SET MODE	C	1	0	D	D	D	D	D	multiplex rate, display status, system type
SET START BANK	C	1	1	1	1	1	D	D	defines bank at top of LCD
DEVICE SELECT	C	1	1	0	D	D	D	D	defines device subaddress
RAM ACCESS	C	1	1	1	D	D	D	D	graphic mode, bank select (D D D D ≥ 12 is not allowed; see SET START BANK opcode)
LOAD X-ADDRESS	C	0	D	D	D	D	D	D	0 to 39

Note

1. C = command continuation bit.
   D = may be a logic 1 or 0.

Table 3 Definition of PCF8578/PCF8579 commands.

COMMAND	OPCODE								OPTIONS	DESCRIPTION
SET MODE	C	1	0	T	E1	E0	M1	M0	see Table 4	defines LCD drive mode
									see Table 5	defines display status
									see Table 6	defines system type
SET START BANK	C	1	1	1	1	1	B1	B0	see Table 7	defines pointer to RAM bank corresponding to the top of the LCD; useful for scrolling, pseudo-motion and background preparation of new display
DEVICE SELECT	C	1	1	0	A3	A2	A1	A0	see Table 8	four bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of sixteen hardware subaddresses
RAM ACCESS	C	1	1	1	G1	G0	Y1	Y0	see Table 9	defines the auto-increment behaviour of the address for RAM access
									see Table 10	two bits of immediate data, bits Y0 to Y1, are transferred to the X-address pointer to define one of forty display RAM columns
LOAD X-ADDRESS	C	0	X5	X4	X3	X2	X1	X0	see Table 11	six bits of immediate data, bits X0 to X5, are transferred to the X-address pointer to define one of forty display RAM columns

Table 4 Set mode option 1.

LCD DRIVE MODE		BITS	
		M1	M0
1 : 8	MUX (8 rows)	0	1
1 : 16	MUX (16 rows)	1	0
1 : 24	MUX (24 rows)	1	1
1 : 32	MUX (32 rows)	0	0

Table 5 Set mode option 2.

DISPLAY STATUS	BITS	
	E1	E0
Blank	0	0
Normal	0	1
All segments on	1	0
Inverse video	1	1

Table 6 Set mode option 3.

SYSTEM TYPE	BIT T
PCF8578 row only	0
PCF8578 mixed mode	1

Table 7 Set start bank option 1.

START BANK POINTER	BITS	
	B1	B0
Bank 0	0	0
Bank 1	0	1
Bank 2	1	0
Bank 3	1	1

Table 8 Device select option 1.

DESCRIPTION	BITS			
Decimal value of 0 to 15	A3	A2	A1	A0

Table 9 RAM access option 1.

RAM ACCESS MODE	BITS	
	G1	G0
Character	0	0
Half-graphic	0	1
Full-graphic	1	0
Not allowed (note 1)	1	1

Note

1. See opcode for SET START BANK in Table 3.

Table 10 RAM access option 2.

DESCRIPTION	BITS	
Decimal value of 0 to 3	Y1	Y0

Table 11 Load X-address option 1.

DESCRIPTION	BITS					
Decimal value of 0 to 39	X5	X4	X3	X2	X1	X0

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL) which must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this moment will be interpreted as control signals.

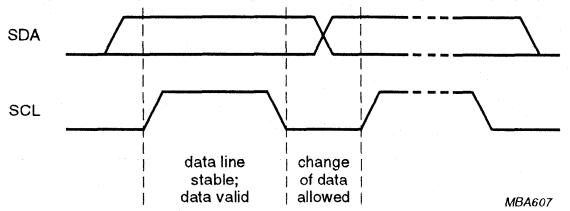


Fig.12 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

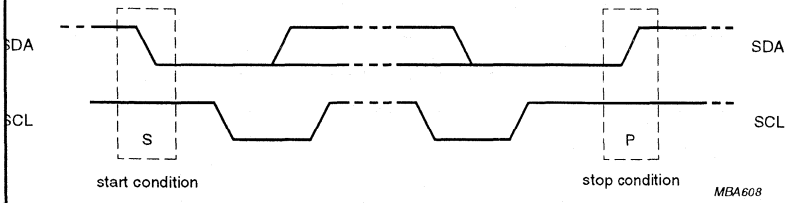


Fig.13 Definition of start and stop condition.

System configuration

A device transmitting a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message flow is the 'master' and the devices which are controlled by the master are the 'slaves'.

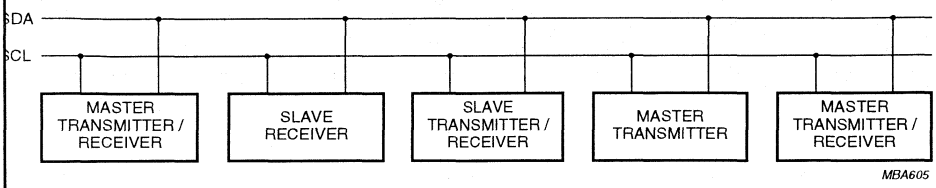
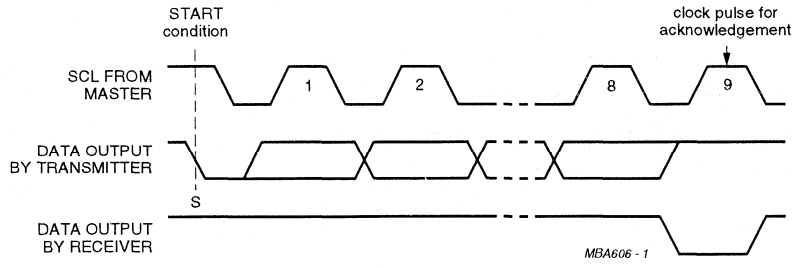


Fig.14 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal the end of a data transmission to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.



The general characteristics and detailed specification of the I²C-bus are available on request.

Fig.15 Acknowledgment on the I²C-bus.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+8.0	V
V_{LCD}	LCD supply voltage	V_{DD} − 11	V_{DD}	V
V_{I1}	input voltage SDA, SCL, $\overline{SYNC}$, CLK, TEST, SA0, A0, A1, A2 and A3	V_{SS} − 0.5	V_{DD} + 0.5	V
V_{I2}	input voltage V_3 and V_4	V_{LCD} − 0.5	V_{DD} + 0.5	V
V_{O1}	output voltage SDA	V_{SS} − 0.5	V_{DD} + 0.5	V
V_{O2}	output voltage C0 to C39	V_{LCD} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	−50	+50	mA
P_{tot}	total power dissipation per package	−	400	mW
P_o	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices.

DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.5	–	6.0	V
V_{LCD}	LCD supply voltage		V_{DD} − 9	–	V_{DD} − 3.5	V
I_{DD}	supply current	f_{clk} = 2 kHz; note 1	–	9	20	μA
V_{POR}	power-on reset level	note 2	–	1.3	1.8	V
Logic						
V_{IL}	LOW level input voltage		V_{SS}	–	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD}	V
I_{L1}	leakage current at SDA, SCL, $\overline{SYNC}$, CLK, TEST, SA0, A0, A1, A2 and A3	V_I = V_{DD} or V_{SS}	−1	–	+1	μA
I_{OL}	LOW level output current at SDA	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
C_I	input capacitance	note 3	–	–	5	pF
LCD outputs						
I_{L2}	leakage current at V_3 to V_4	V_I = V_{DD} or V_{LCD}	−2	–	+2	μA
V_{DC}	DC component of LCD drivers C0 to C39		–	±20	–	mV
R_{COL}	output resistance at C0 to C39	note 4	–	3	6	kΩ

Notes

1. Outputs are open; inputs at V_{DD} or V_{SS}; I^2C-bus inactive; clock with 50% duty factor.
2. Resets all logic when $V_{DD} < V_{POR}$.
3. Periodically sampled; not 100% tested.
4. Resistance measured between output terminal (C0 to C39) and bias input (V_3, V_4, V_{DD} and V_{LCD}) when the specified current flows through one output under the following conditions (see Table 1):
   - V_{op} = V_{DD} − V_{LCD} = 9 V;
   - V_3 − V_{LCD} ≥ 4.70 V; V_4 − V_{LCD} ≤ 4.30 V; I_{LOAD} = 100 μA.

AC CHARACTERISTICS

All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clk}	clock frequency	50% duty factor	–	note 1	10	kHz
t_{PLCD}	driver delays	$V_{DD} - V_{LCD}$ = 9 V; with test loads	–	–	100	µs
I²C-bus						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SW}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	start condition set-up time	repeated start codes only	4.7	–	–	µs
$t_{HD;STA}$	start condition hold time		4.0	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1.0	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	stop condition set-up time		4.0	–	–	µs

Note

1. Typically 0.9 to 3.3 kHz.

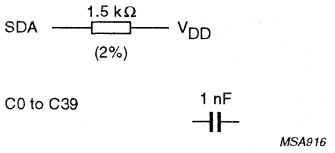


Fig.16 AC test loads.

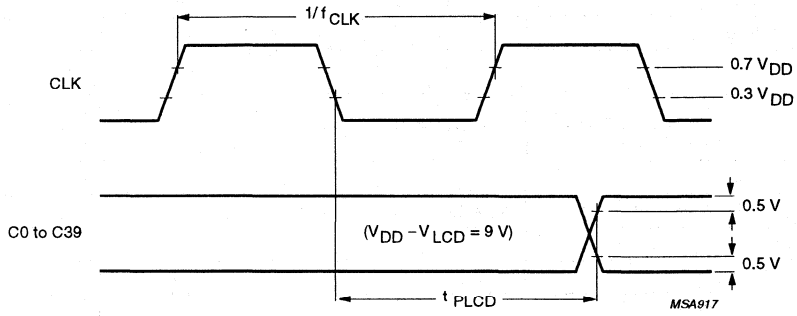


Fig.17 Driver timing waveforms.

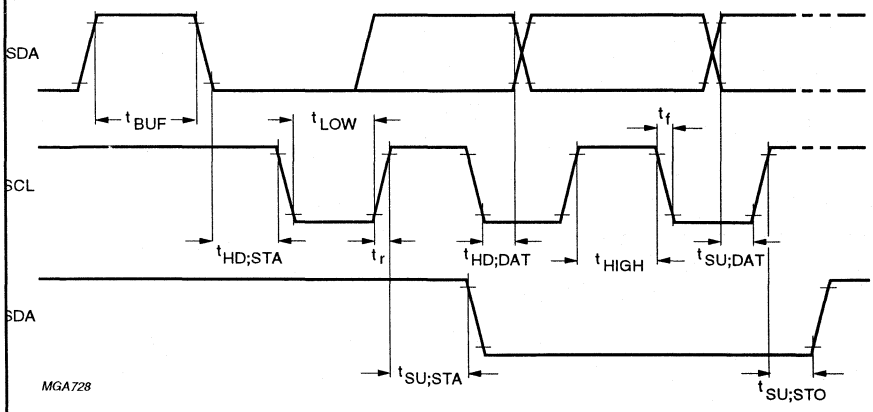


Fig.18 I²C-bus timing waveforms.

APPLICATION INFORMATION

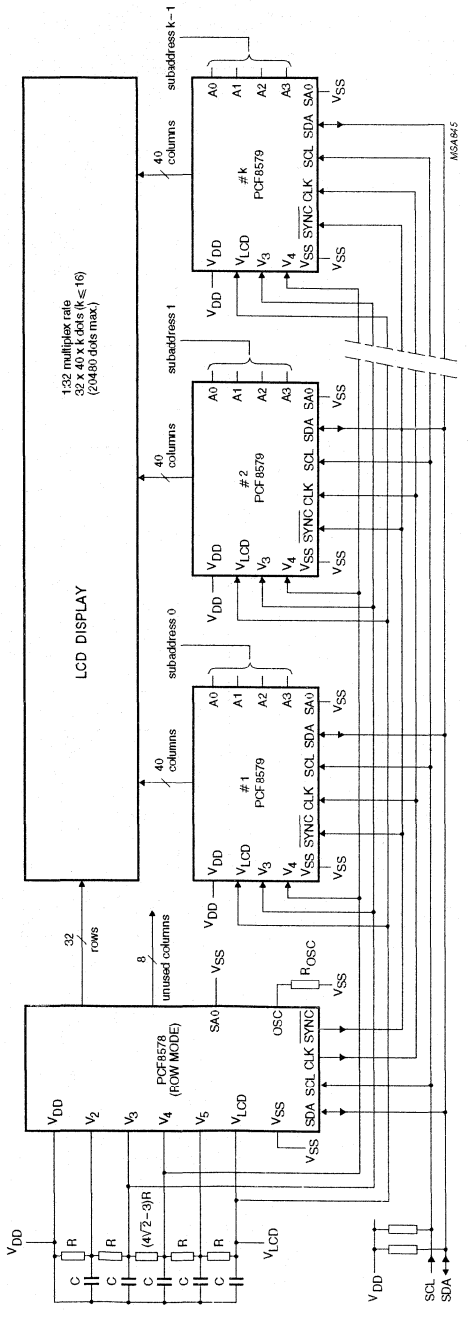


Fig.19 Typical LCD driver system with 1 : 32 multiplex rate.

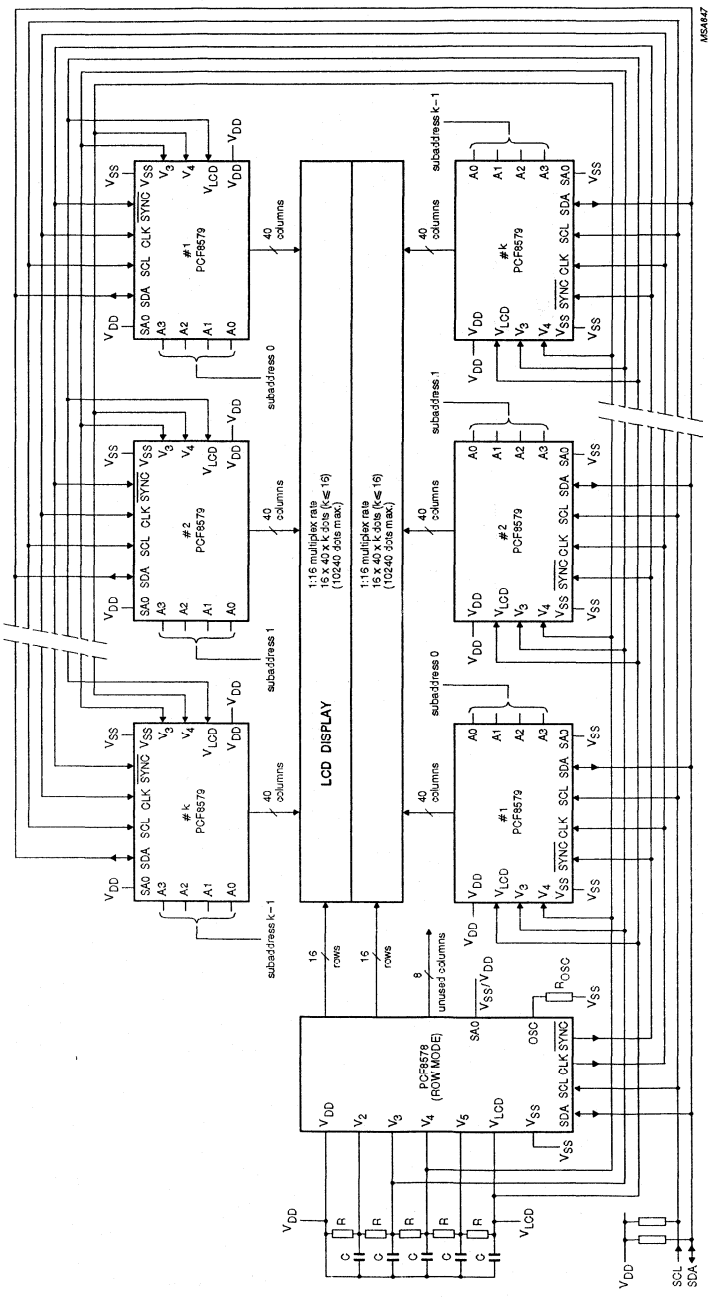


Fig.20 Split screen application with 1 : 16 multiplex rate for improved contrast.

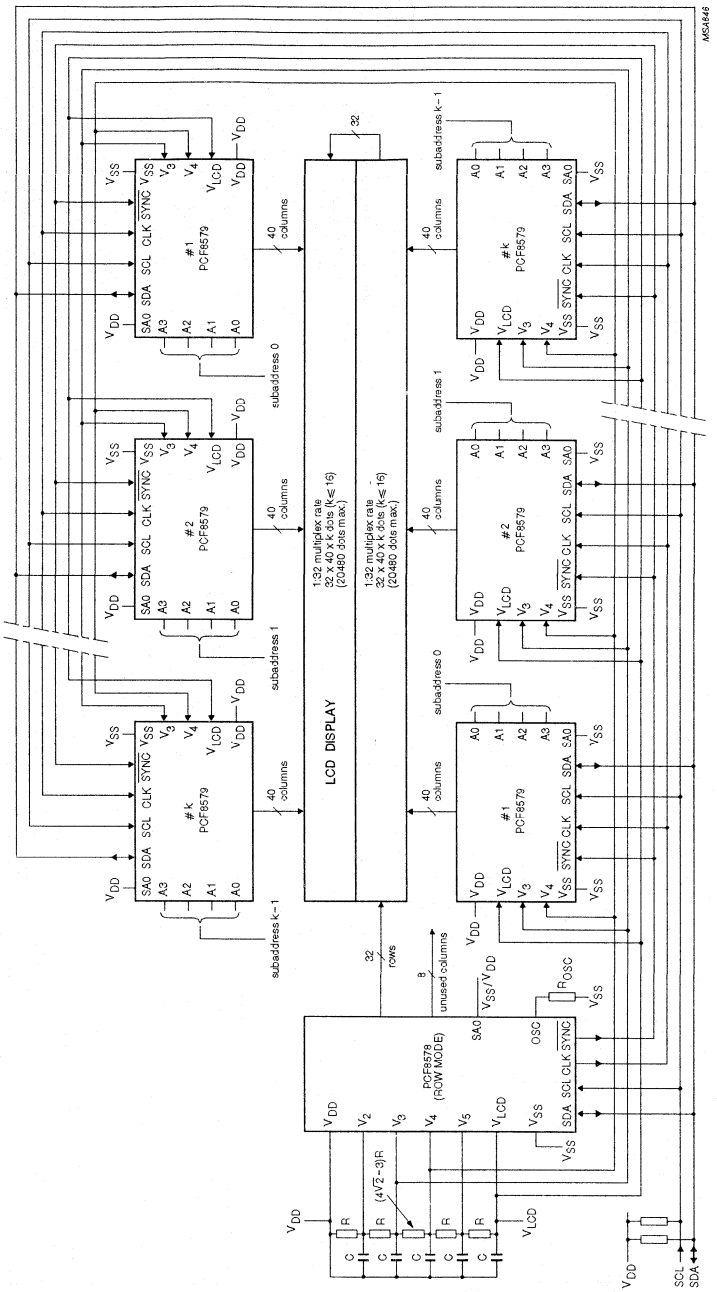


Fig.21 Split screen application with 1 : 32 multiplex rate.

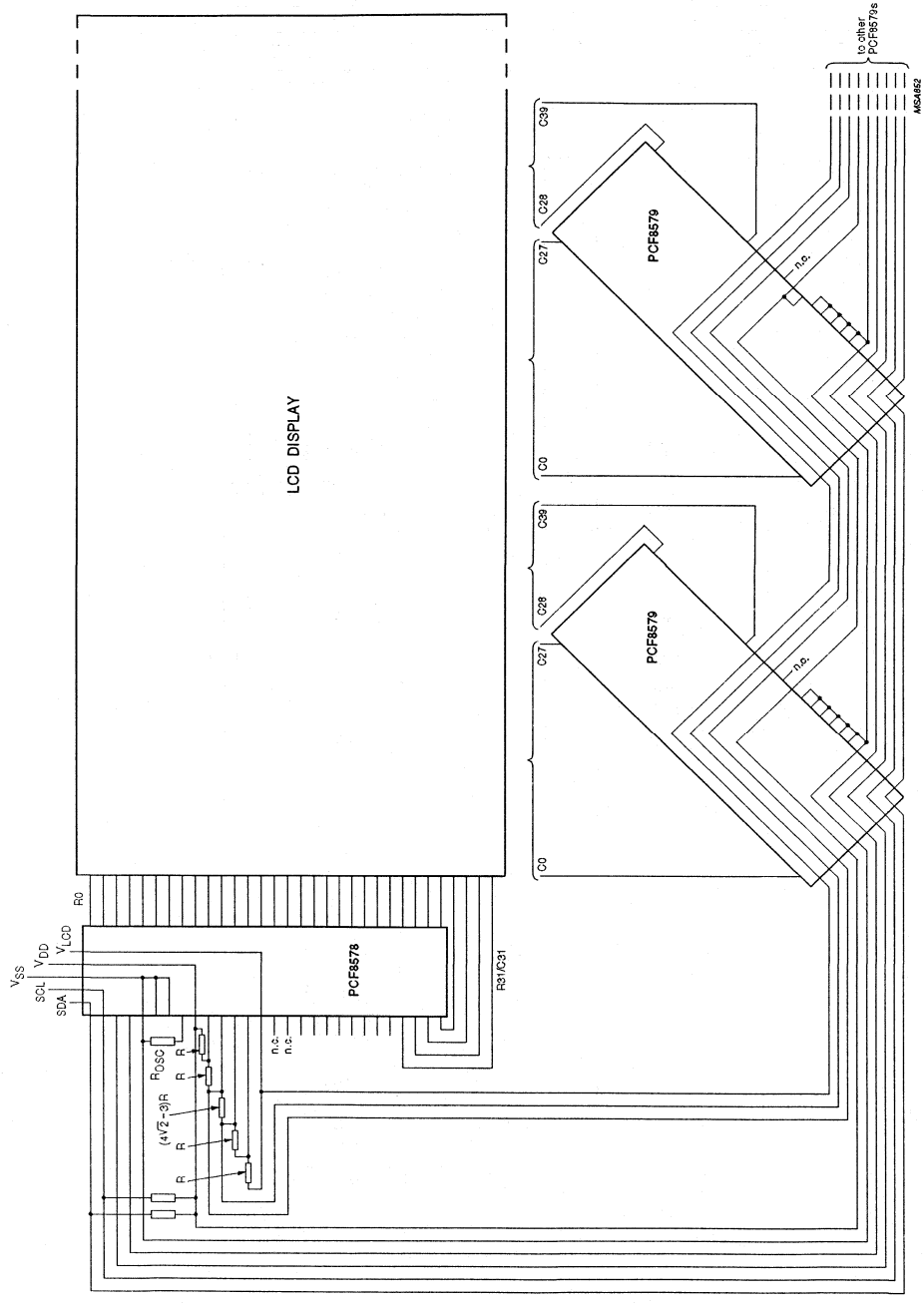
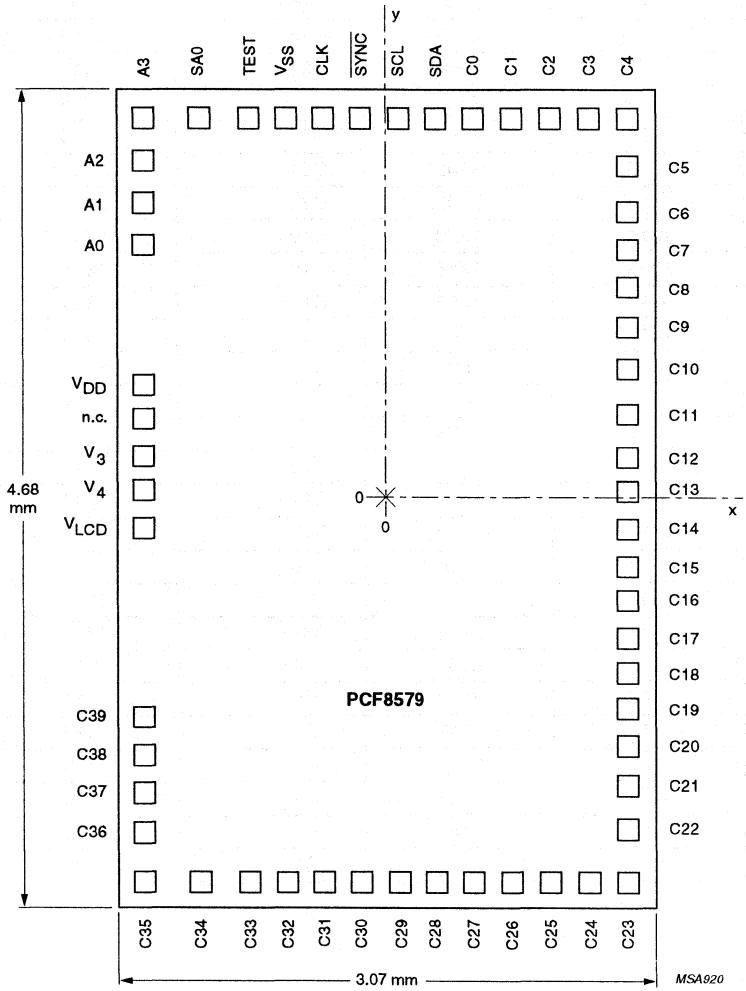


Fig.22 Example of single plane wiring, single screen with 1 : 32 multiplex rate (PCF8578 in row driver mode).

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



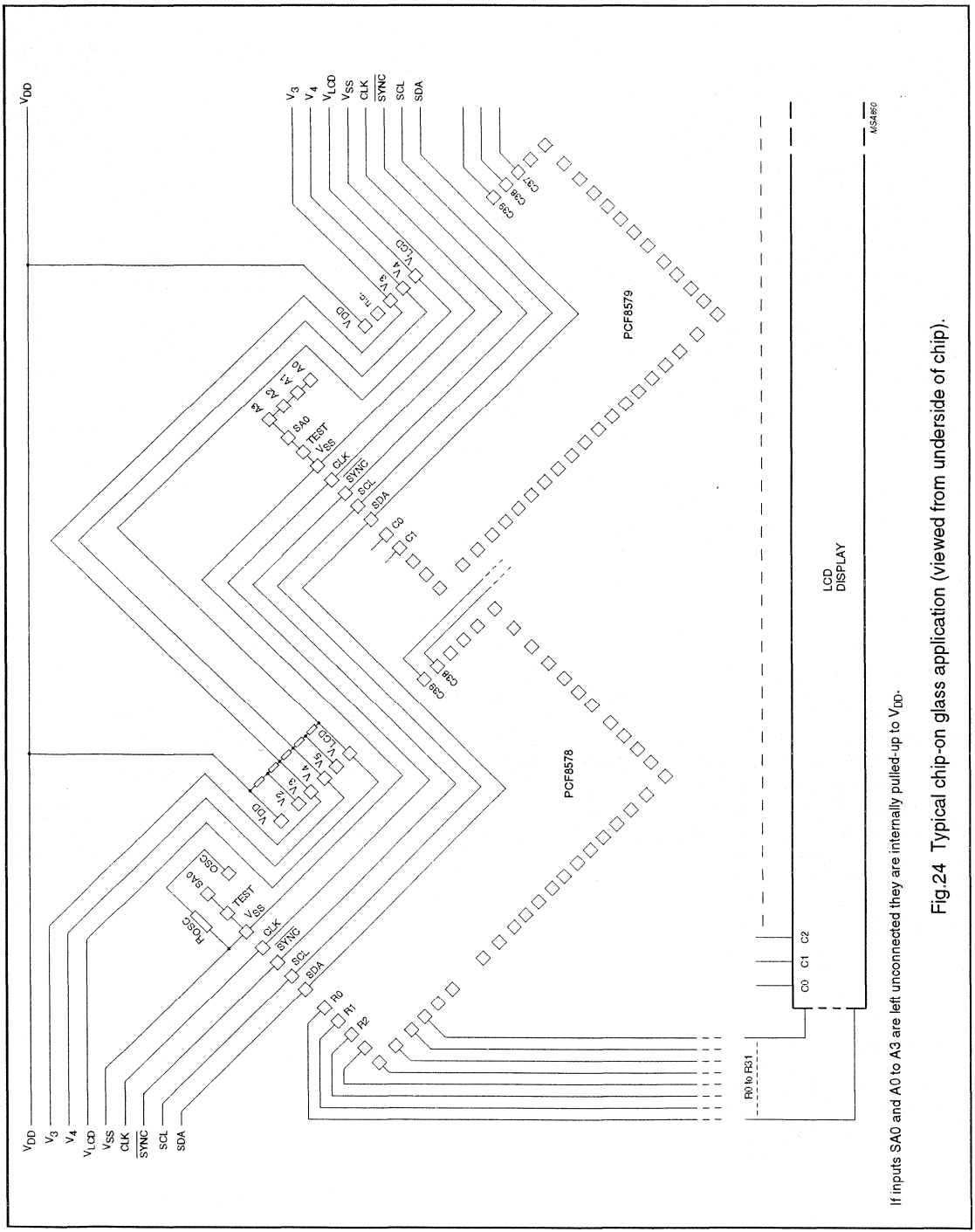
Chip area: 14.37 mm^2.
Bonding pad dimensions: 120 µm x 120 µm.

Fig.23 Bonding pad locations.

Table 12 Bonding pad locations (dimensions in μm).
All x/y coordinates are referenced to centre of chip, see Fig.23.

PAD	x	y	PAD	x	y
SDA	252	2142	C27	498	−2142
SCL	48	2142	C26	702	−2142
$\overline{SYNC}$	−156	2142	C25	906	−2142
CLK	−360	2142	C24	1110	−2142
V_{SS}	−564	2142	C23	1314	−2142
TEST	−786	2142	C22	1314	−1830
SA0	−1032	2142	C21	1314	−1570
A3	−1314	2142	C20	1314	−1326
A2	−1314	1920	C19	1314	−1122
A1	−1314	1716	C18	1314	−918
A0	−1314	1512	C17	1314	−714
V_{DD}	−1314	708	C16	1314	−510
n.c.	−1314	504	C15	1314	−306
V_3	−1314	300	C14	1314	−102
V_4	−1314	96	C13	1314	102
V_{LCD}	−1314	−108	C12	1314	306
C39	−1314	−1308	C11	1314	510
C38	−1314	−1512	C10	1314	714
C37	−1314	−1716	C9	1314	918
C36	−1314	−1920	C8	1314	1122
C35	−1314	−2142	C7	1314	1326
C34	−1032	−2142	C6	1314	1566
C33	−786	−2142	C5	1314	1830
C32	−564	−2142	C4	1314	2142
C31	−360	−2142	C3	1110	2142
C30	−156	−2142	C2	906	2142
C29	48	−2142	C1	702	2142
C28	252	−2142	C0	498	2142

CHIP-ON GLASS INFORMATION



If inputs SA0 and A0 to A3 are left unconnected they are internally pulled-up to V_{DD}.

Fig.24 Typical chip-on glass application (viewed from underside of chip).

Clock Calendar with 256 x 8-bit Static RAM

PCF8583

FEATURES

- I²C-bus interface operating supply voltage: 2.5 V to 6 V
- Clock operating supply voltage (0 to +70 °C): 1.0 V to 6.0 V
- Data retention voltage: 1.0 V to 6 V
- Operating current (f_{scl} = 0 Hz): max. 50 A
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Slave address, READ: A1 or A3, WRITE: A0 or A2.

GENERAL DESCRIPTION

The PCF8583 is a low power 2048-bit static CMOS RAM organized as 256 words by 8 bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. One address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware. The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
V_{DD}	supply voltage operating range	I²C-bus active	2.5	6.0	V
V_{DD}	supply voltage operating range	I²C-bus inactive	1.0	6.0	V
I_{DD}	supply current operating mode	f_{scl} =100 kHz	-	200	µA
I_{DDO}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 5 V f_{scl} = 0 Hz; V_{DD} = 1 V	- -	50 10	µA µA
T_{amb}	operating ambient temperature range		–40	+85	°C
T_{stg}	storage temperature range		–65	+150	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8583P	8	DIL	plastic	SOT97
PCF8583T	8	mini-pack	plastic	SO8L; SOT176C

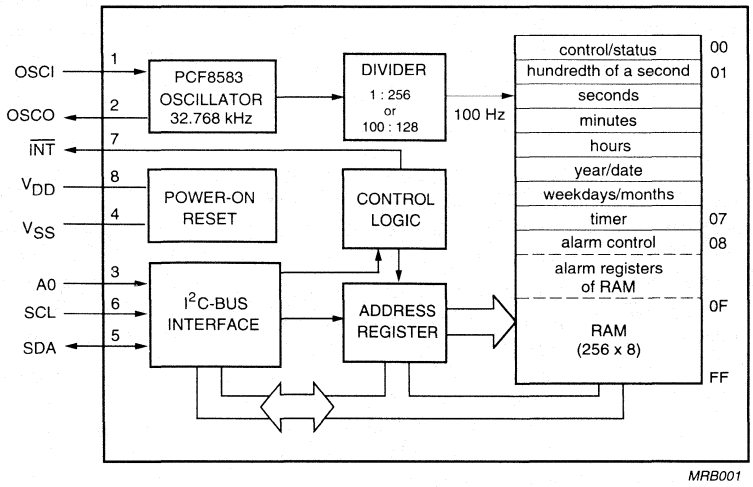


Fig.1 Block diagram.

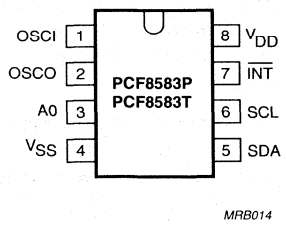


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
A0	3	address input
V_{SS}	4	negative supply
SDA	5	serial data line
SCL	6	serial clock line
$\overline{INT}$	7	open drain interrupt output (active LOW)
V_{DD}	8	positive supply

FUNCTIONAL DESCRIPTION

The PCF8583 contains a 256 by 8-bit RAM with an 8-bit auto-increment address register, an on-chip 32.768 kHz oscillator circuit, a frequency divider, a serial two-line bidirectional I²C-bus interface and a power-on reset circuit.

The first 8 bytes of the RAM (memory addresses 00 to 07) are designed as addressable 8-bit parallel registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F are free RAM locations or may be programmed as alarm registers.

Counter function modes

When the control/status register is programmed, a 32.768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredth of a second, seconds, minutes, hours, date, month (four year calendar) and weekday are stored in a BCD format. The timer register stores up to 99 days. The event counter mode is used to count pulses applied to the oscillator input (OSCO left open). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore, faulty reading of the count during a carry condition is prevented.

When a counter is written, other counters are not affected.

Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a weekday alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled). The flags remain set until directly reset by a write operation.

When a timer function without any function is programmed the remaining alarm registers (addresses 09 to 0F) may be used as free RAM space.

Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I²C-bus. All functions and options are controlled by the contents of the control/status register (see Fig. 3).

Counter registers

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig 5.

The year and date are packed into memory location 05 (see Fig 6). The weekdays and months are packed into memory location 06 (see Fig. 7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

In the different modes the counter registers are programmed and arranged as shown in Fig 4. Counter cycles are listed in Table 1.

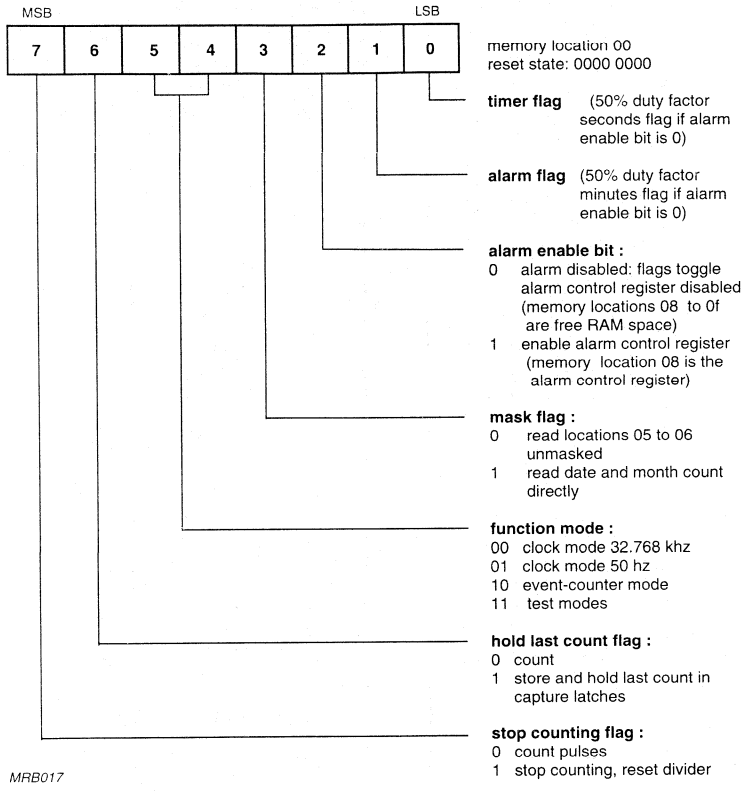


Fig.3 Control/status register.

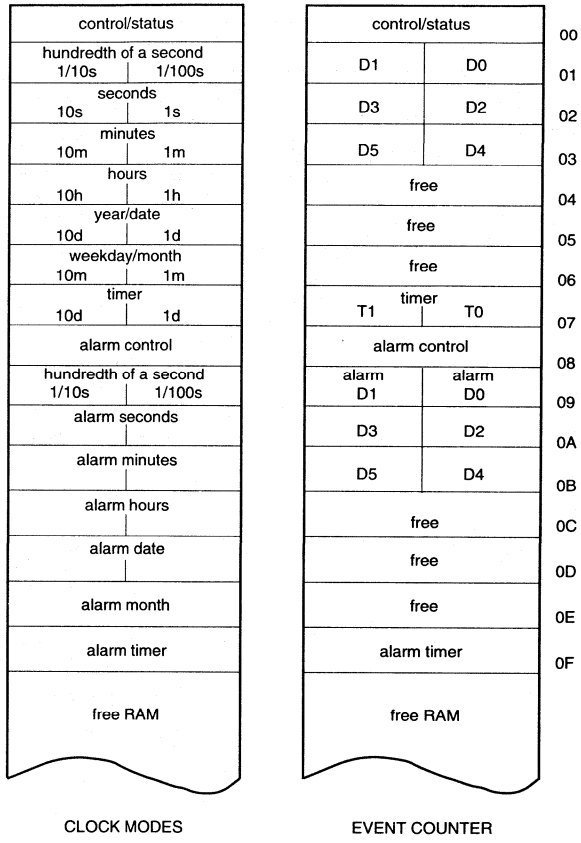


Fig.4 Register arrangement.

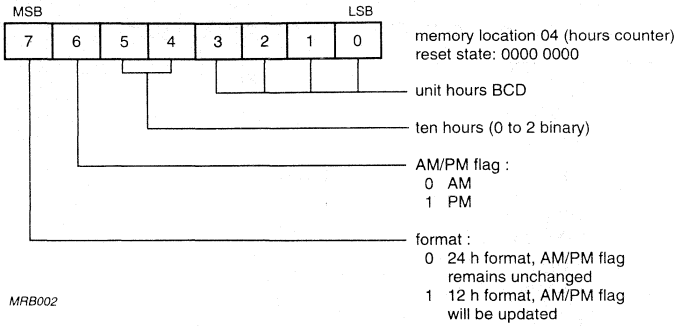


Fig.5 Format of the hours counter.

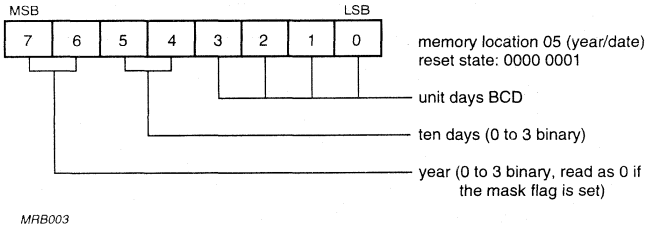


Fig.6 Format of the year/date counter.

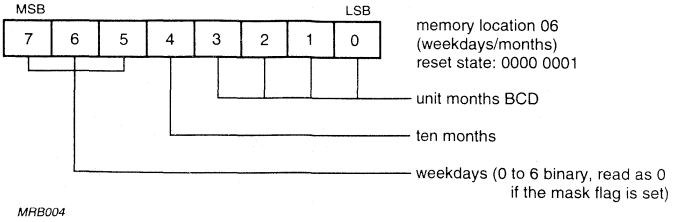


Fig.7 Format of the weekdays/months counter.

Table 1 Cycle length of the time counters, clock modes

UNIT	COUNTING CYCLE	CARRY TO NEXT UNIT	CONTENTS OF THE MONTH COUNTER
hundredths of a second	00 to 99	99 to 00	
seconds	00 to 59	59 to 00	
minutes	00 to 59	59 to 00	
hours (24 h)	00 to 23	23 to 00	
hours (12 h)	12 AM; 01 AM to 11 AM; 12 PM; 01 PM to 11 PM	 11 PM to 12 AM	
date	01 to 31	31 to 01	1, 3, 5, 7, 8, 10, 12
	01 to 30	30 to 01	4, 6, 9, 11
	01 to 29	29 to 01	2, year = 0
	01 to 28	28 to 01	2, year = 1, 2, 3
months	01 to 12	12 to 01	
year	0 to 3		
weekdays	0 to 6	6 to 0	
timer	00 to 99	no carry	

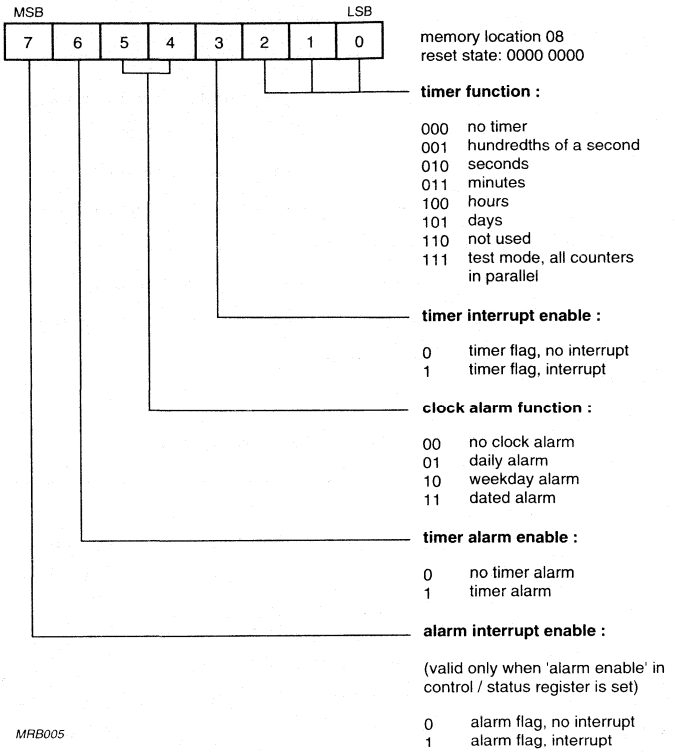


Fig.8 Alarm control register; clock mode.

Alarm Control register

When the alarm enable bit of the control/status register is set (address 00, bit 2) the Alarm Control register (address 08) is activated. All alarm, timer, and interrupt output functions are controlled by the contents of the alarm control register (see Fig 8).

Alarm registers

All alarm registers are allocated with a constant address offset of hex 08 to the corresponding counter registers (see Fig 4, Register arrangement).

An alarm signal is generated when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected , the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig. 9).

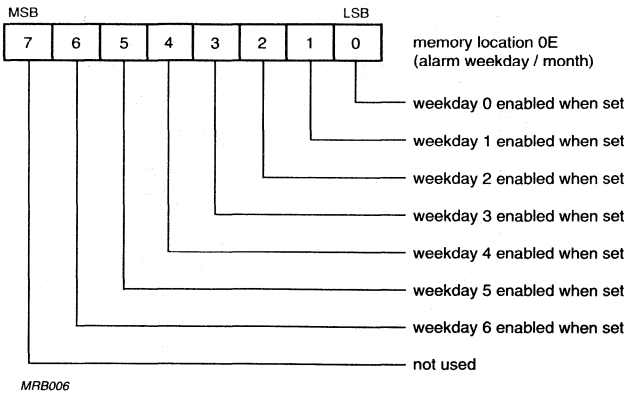


Fig.9 Selection of alarm weekdays.

Note:

In the 12 h mode, bits 6 and 7 of the alarm hours register must be the same as the hours counter.

Timer

The timer (location 07) is enabled by setting the Control/Status register = XX0X X1XX. The timer counts up from 0 (or a programmed value) to 99. On overflow, the timer resets to 0. The Timer flag (LSB of Control/Status register) is set on overflow of the timer. This flag must be reset by software. The inverted value of this flag can be transferred to the external interrupt by setting bit 3 of the Alarm Control register.

Additionally, a timer alarm can be programmed by setting the Timer Alarm enable (bit 6 of the Alarm Control register). When the value of the timer equals a pre-programmed value in the Alarm Timer register (location 0F), the Alarm flag is set (bit 1 of the Control/status register). The inverted value of the alarm flag can be transferred to the external interrupt by enabling the Alarm interrupt (bit 6 of the Alarm Control register).

Resolution of the timer is programmed via the 3 LSBs of the Alarm Control register. See fig 11: Alarm and Timer Interrupt logic diagram.

Event Counter Mode

Event Counter mode is selected by bits 4 and 5 = 10 in the Control/status register. The event counter mode is used to count pulses externally applied to the oscillator input (OSCO left open). The event counter stores up to 6 digits of data, which are stored as 6 hexadecimal values located in locations 1, 2, and 3. Thus, up to 1 million events may be recorded.

An event counter alarm occurs when the event counter registers match the value programmed in locations 9, A, and B, and the event alarm is enabled (bits 4 and 5 = 01 in the Alarm Control register). In this case, the Alarm flag (bit 1 of the Control/status register) is set. The inverted value of this flag can be transferred to the interrupt pin (pin 7) by setting the Alarm interrupt enable in the Alarm Control register. In this mode, the timer (location 07) increments once for every one, one-hundred, ten thousand, or 1 million events, depending on the value programmed in bits 0 1 2 of the Alarm Control register. In all other respects, the timer functions as in the clock mode.

Interrupt output

The conditions for activating the open-drain n-channel interrupt output (active LOW) are determined by appropriate programming of the Alarm Control register. These conditions are: Clock alarm, timer alarm, timer overflow, and event counter alarm. An interrupt occurs when the alarm flag or the timer flag is set, and the corresponding interrupt is enabled. In all cases, the interrupt is cleared only by software resetting of the flag which initiated the interrupt.

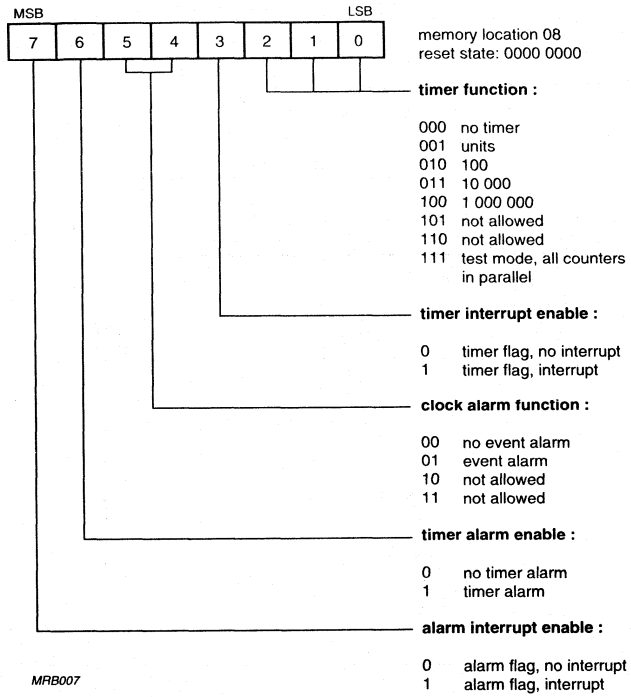


Fig.10 Alarm control register, event-counter mode.

In the clock mode, if the Alarm enable is not activated (Alarm Enable bit of Control/status register = 0), the interrupt output toggles with at 1 Hz with a 50% duty cycle. This is the default power-on state of the device. The OFF voltage of the interrupt output may exceed the supply voltage, up to a maximum of 6.0 V. A logic diagram of the interrupt output is shown in Fig 11.

Oscillator and divider

A 32.768 kHz quartz crystal has to be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator (see quartz frequency adjustment). A 100 Hz clock signal is derived from the quartz oscillator for the clock counters.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high impedance state. This allows the user to feed the 50 Hz reference frequency or an external high speed event signal into the input OSCI.

Initialization

When power-up occurs the I²C-bus interface, the control/status register and all clock counters are reset. The device starts time-keeping in the 32.768 kHz clock mode with the 24 h format on the first of January at 0.00.00: 00. A 1 Hz square wave with 50% duty cycle appears at the interrupt output pin (starts HIGH).

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states may lead to a temporary clock malfunction.

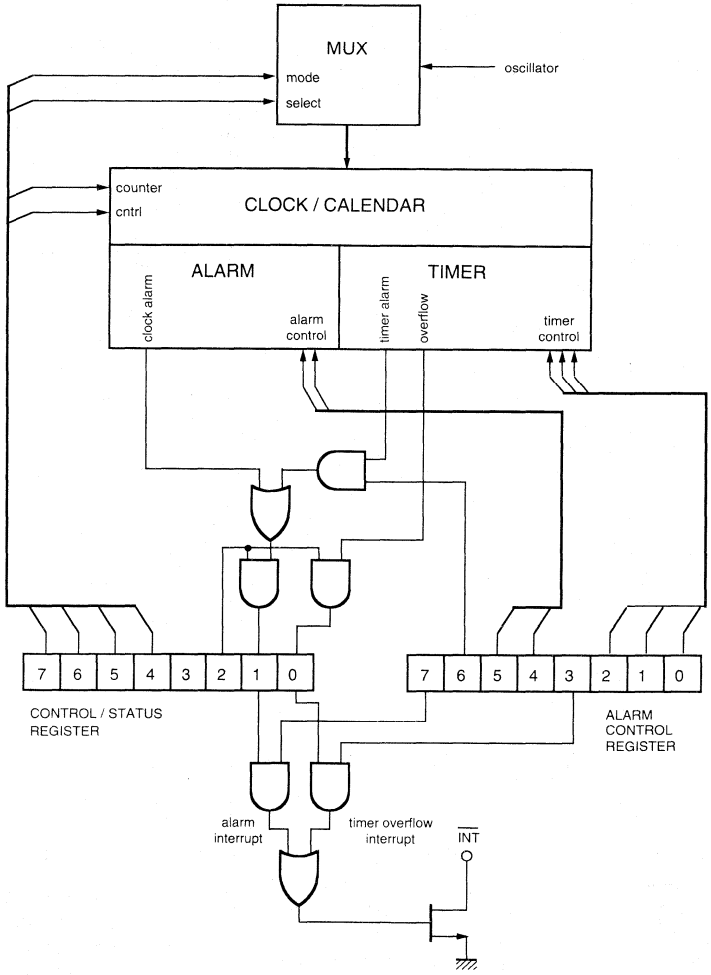


Fig.11 Alarm and Timer Interrupt logic diagram.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF8583 READ and WRITE cycles is shown in Figs. 16, 17 and 18.

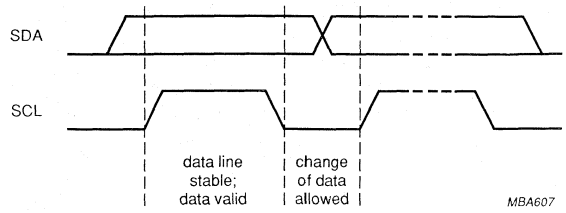


Fig.12 Bit transfer.

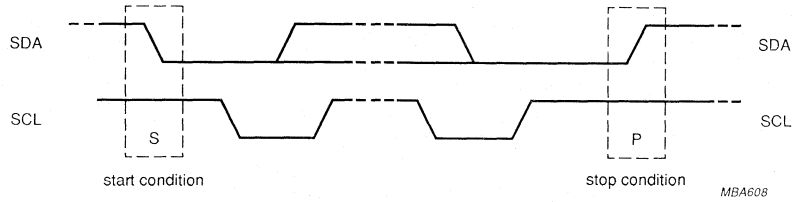


Fig.13 Definition of start and stop conditions.

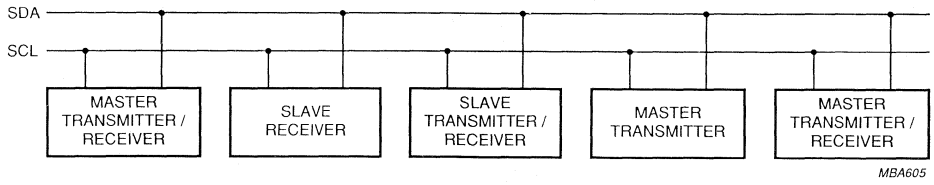


Fig.14 System configuration.

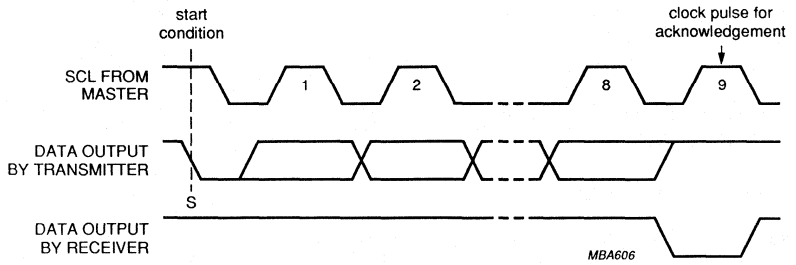


Fig.15 Acknowledgement on the I²C-bus.

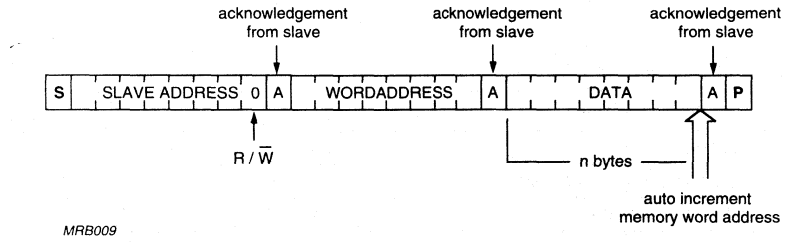


Fig.16 Master transmits to slave receiver (WRITE mode).

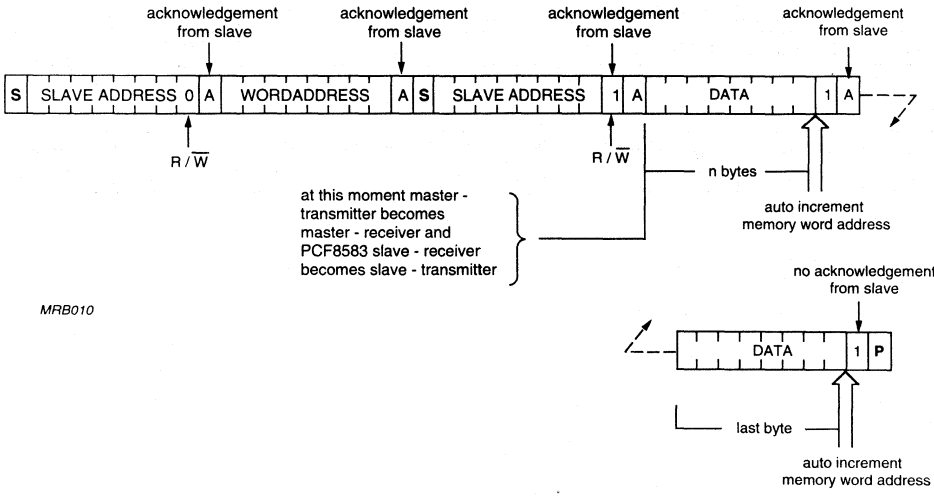


Fig.17 Master reads after setting word address (Write word address; READ data)

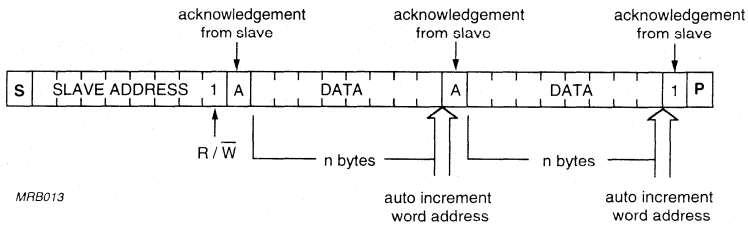


Fig.18 Master reads slave immediately after first byte (READ mode).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range (pin 8)	−0.8	+7.0	V
I_{SS}; I_{DD}	supply current (pin 4 or pin 8)	-	50	mA
V_I	input voltage range	−0.8 to V_{DD}	+0.8	V
I_I	DC input current	-	10	mA
I_O	DC output current	-	10	mA
P_{tot}	power dissipation per package	-	300	mW
P_O	power dissipation per output	-	50	mW
T_{amb}	operating ambient temperature range	−40	+85	°C
T_{stg}	storage temperature range	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range	I²C-bus active	2.5	-	6.0	V
		I²C-bus inactive	1.0	-	6.0	V
	quartz oscillator supply voltage range	T_{amb} = 0 to 70 °C; note 1	1.0	-	6.0	V
I_{DD}	supply current operating mode	f_{scl} =100 kHz; clock mode; note 2	-	-	200	µA
I_{DDO}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 5 V; f_{scl} = 0 Hz; V_{DD} = 1 V	- -	10 2	50 10	µA µA
I_{DDR}	data retention	f_{OSCI} = 0 Hz; V_{DD} = 1 V; T_{amb} = –40 to +85 °C	-	-	5	µA
		f_{OSCI} = 0 Hz; V_{DD} = 1 V T_{amb} = –25 to +70 °C	-	-	2	µA
V_{EN}	I²C-bus enable level	note 3	1.5	1.9	2.3	V
SDA						
V_{IL}	input voltage LOW	note 4	–0.8	-	0.3 V_{DD}	V
V_{IH}	input voltage HIGH	note 4	0.7 V_{DD}	-	V_{DD} +0.8	V
I_{OL}	output current LOW	V_{OL} = 0.4 V	3	-	-	mA
$\|I_L\|$	leakage current	V_I = V_{DD} or V_{SS}	-	-	1	µA
C_I	input capacitance	note 5	-	-	7	pF
A0; OSCI						
$\|I_L\|$	leakage current	V_I = V_{DD} or V_{SS}	-	-	250	nA
$\overline{\text{INT}}$						
I_{OL}	output current LOW	V_{OL} = 0.4 V	3	-	-	mA
$\|I_L\|$	leakage current	V_I = V_{DD} or V_{SS}	-	-	1	µA
SCL						
C_I	input capacitance	note 5	-	-	7	pF
$\|I_L\|$	leakage current	V_I = V_{DD} or V_{SS}	-	-	1	µA

Notes

1. When powering up the device, V_{DD} must exceed 1.5 V until stable operation of the oscillator is established.
2. Event counter mode: supply current dependant upon input frequency.
3. The I²C-bus logic is disabled if $V_{DD} < V_{EN}$.
4. When the voltages are above or below the supply voltages V_{DD} or V_{SS}, an input current may flow; this current must not exceed ±0.5 mA.
5. Tested on sample basis.

AC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
C_{OSC}	integrated oscillator capacitance		-	40	-	pF
f/f_{OSC}	oscillator stability	for ΔV_{DD} = 100 mV; T_{amb} = 25 °C; V_{DD} = 1.5 V	-	2 x 10^{-7}	-	
f_i	Input frequency	note 1	-	-	1	MHz
Quartz crystal parameters (frequency = 32.768 kHz)						
R_S	series resistance		-	-	40	kΩ
C_L	parallel capacitance		-	10	-	pF
C_T	trimmer capacitance		5	-	25	pF
I²C-bus timing (note 2)						
f_{scl}	SCL clock frequency		-	-	100	kHz
t_{SW}	tolerable spike width on bus		-	-	100	ns
t_{BUF}	bus free time		4.7	-	-	µs
$t_{SU;STA}$	start condition set-up time		4.7	-	-	µs
$t_{HD;STA}$	start condition hold time		4.0	-	-	µs
t_{LOW}	SCL LOW time		4.7	-	-	µs
t_{HIGH}	SCL HIGH time		4.0	-	-	µs
t_r	SCL and SDA rise time		-	-	1.0	µs
t_f	SCL and SDA fall time		-	-	0.3	µs
$t_{SU;DAT}$	data set-up time		250	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{VD;DAT}$	SCL LOW to data out valid		-	-	3.4	µs
$t_{SU;STO}$	stop condition set-up time		4.0	-	-	µs

Notes

1. Event counter mode only.
2. All timing values are valid within the operating supply voltage and ambient temperature range and refer V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

Note:

The general characteristics and detailed specification of the I²C-bus are available on request.

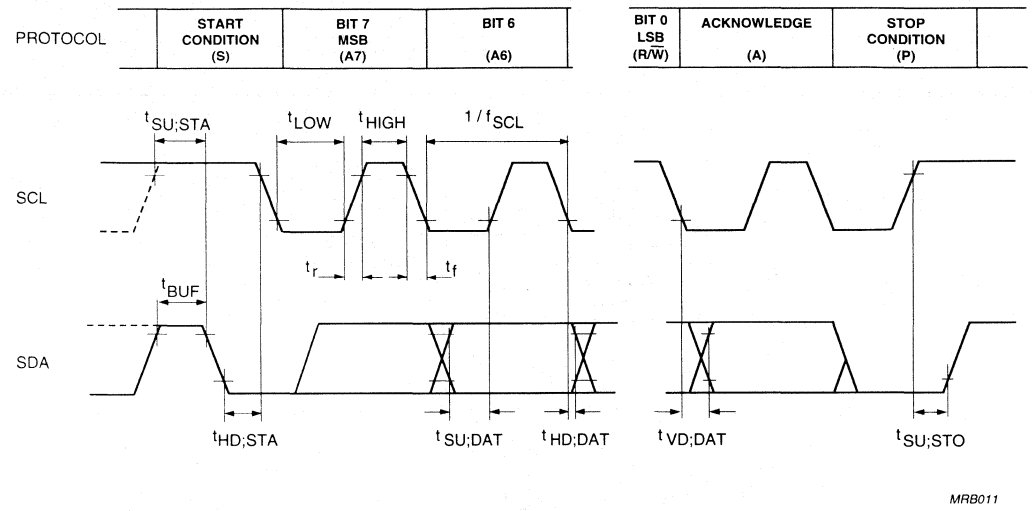


Fig.19 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

APPLICATION INFORMATION

Quartz frequency adjustment

METHOD 1: FIXED OSCI CAPACITOR

By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 1 Hz signal available after power-on at the interrupt output (pin 7). The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average ±5 x 10^{-6}). Average deviations of ±5 minutes per year can be achieved.

METHOD 2 : OSCI TRIMMER

Using the alarm function (via the I²C-bus) a signal faster than 1 Hz can be generated at the interrupt output for fast setting of a trimmer.

Procedure:

- Power-on
- Initialization (alarm functions).

Routine:

- Set clock to time T and set alarm to time T + dT
- At time T + dT (interrupt) repeat routine.

METHOD 3:

Direct measurement of OSC out (accounting for test probe capacitance).

The PCF8583 slave address has a fixed combination 1010 as group 1.

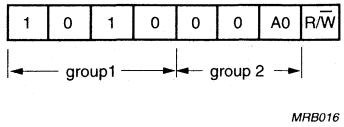


Fig.20 Slave address.

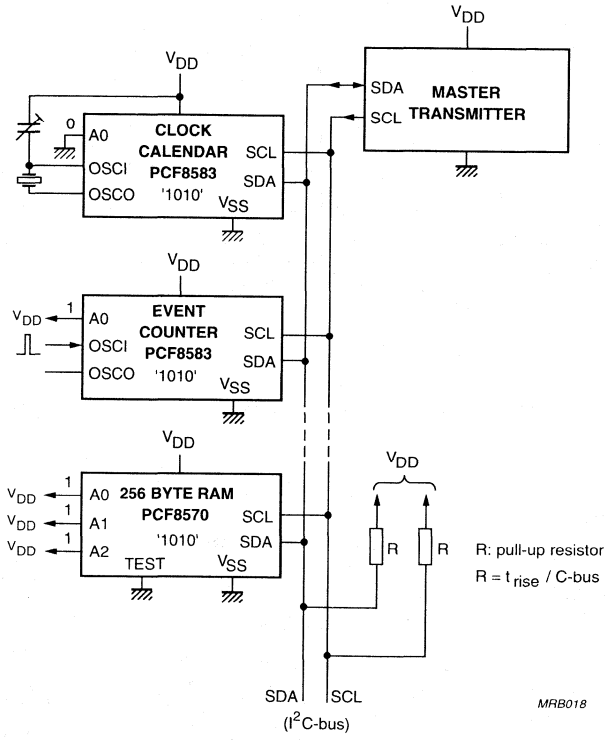


Fig.21 Application diagram.

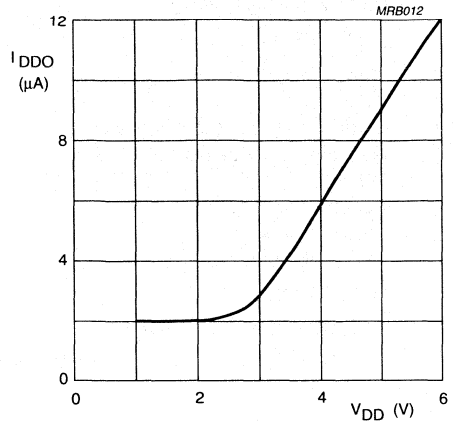


Fig.22 Typical supply current as a function of supply voltage (clock = 32 kHz; T_{amb} = –40 to +85 °C)

I²C-bus controller PCF8584

CONTENTS

I²C-bus controller PCF8584

1 FEATURES

- Parallel-bus to I²C-bus protocol converter and interface
- Compatible with most parallel-bus microcontrollers/microprocessors including 8049, 8051, 6800, 68000, and Z80
- Both master and slave functions
- Automatic detection and adaption to bus interface type
- Programmable interrupt vector
- Multi-master capability
- I²C-bus monitor mode
- Long-distance mode (4-wire)
- Operating supply voltage 4.5 to 5.5 V
- Operating temperature range: –40 to +85 °C.

2 GENERAL DESCRIPTION

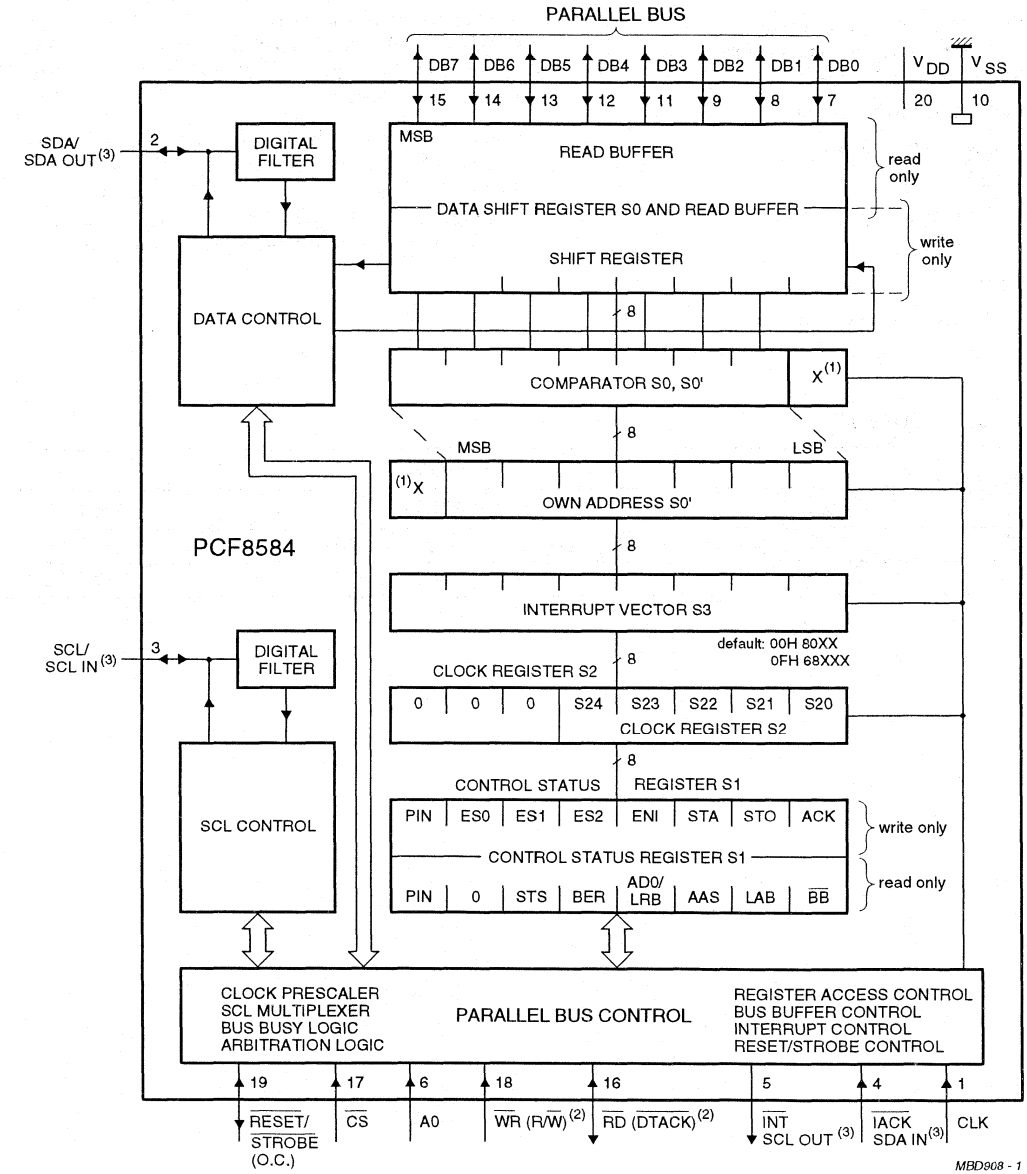
The PCF8584 is an integrated circuit designed in CMOS technology which serves as an interface between most standard parallel-bus microcontrollers/microprocessors and the serial I²C-bus. The PCF8584 provides both master and slave functions.

Communication with the I²C-bus is carried out on a byte-wise basis using interrupt or polled handshake. It controls all the I²C-bus specific sequences, protocol, arbitration and timing. The PCF8584 allows parallel-bus systems to communicate bidirectionally with the I²C-bus.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8584P	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
PCF8584T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

4 BLOCK DIAGRAM



(1) X = don't care.

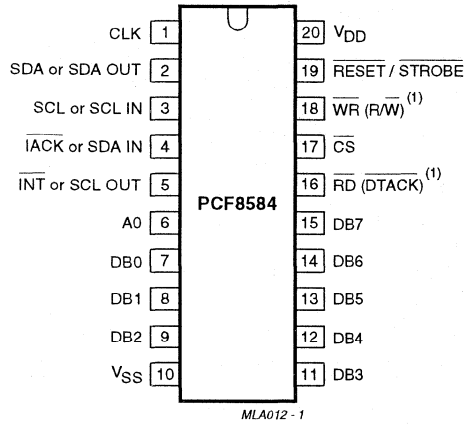
(2) Pin mnemonics between brackets indicate the 68000 mode pin designations.

(3) These pin mnemonics represent the long-distance mode pin designations.

Fig.1 Block diagram.

5 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
CLK	1	I	clock input from microcontroller clock generator (internal pull-up)
SDA or SDA OUT	2	I/O	I²C-bus serial data input/output (open-drain). Serial data output in long-distance mode.
SCL or SCL IN	3	I/O	I²C-serial clock input/output (open-drain). Serial clock input in long-distance mode.
$\overline{\text{IACK}}$ or SDA IN	4	I	Interrupt acknowledge input (internal pull-up); when this signal is asserted the interrupt vector in register S3 will be available at the bus Port if the ENI flag is set. Serial data input in long-distance mode.
$\overline{\text{INT}}$ or SCL OUT	5	O	Interrupt output (open-drain); this signal is enabled by the ENI flag in register S1. It is asserted when the PIN flag is reset. (PIN is reset after 1 byte is transmitted or received over the I²C-bus). Serial clock output in long-distance mode.
A0	6	I	Register select input (internal pull-up); this input selects between the control/status register and the other registers. Logic 1 selects register S1, logic 0 selects one of the other registers depending on bits loaded in ESO, ES1, and ES2 of register S1.
DB0	7	I/O	bidirectional 8-bit bus Port 0
DB1	8	I/O	bidirectional 8-bit bus Port 1
DB2	9	I/O	bidirectional 8-bit bus Port 2
V_{SS}	10	–	ground
DB3	11	I/O	bidirectional 8-bit bus Port 3
DB4	12	I/O	bidirectional 8-bit bus Port 4
DB5	13	I/O	bidirectional 8-bit bus Port 5
DB6	14	I/O	bidirectional 8-bit bus Port 6
DB7	15	I/O	bidirectional 8-bit bus Port 7
$\overline{\text{RD}}$ ($\overline{\text{DTACK}}$)	16	I/(O)	$\overline{\text{RD}}$ is the read control input for MAB8049, MAB8051 or Z80-types. $\overline{\text{DTACK}}$ is the data transfer control output for 68000-types (open-drain).
$\overline{\text{CS}}$	17	I	chip select input (internal pull-up)
$\overline{\text{WR}}$ (R/$\overline{\text{W}}$)	18	I	$\overline{\text{WR}}$ is the write control input for MAB8048, MAB8051, or Z80-types (internal pull-up). R/$\overline{\text{W}}$ control input for 68000-types.
$\overline{\text{RESET}}$/ $\overline{\text{STROBE}}$	19	I/O	Reset input (open-drain); this input forces the I²C-bus controller into a predefined state; all flags are reset, except PIN, which is set. Also functions as strobe output.
V_{DD}	20	–	supply voltage



(1) Pin mnemonics between brackets indicate the 68000 mode pin designations.

Fig.2 Pin configuration.

6 FUNCTIONAL DESCRIPTION

6.1 General

The PCF8584 acts as an interface device between standard high-speed parallel buses and the serial I²C-bus. On the I²C-bus, it can act either as master or slave. Bidirectional data transfer between the I²C-bus and the parallel-bus microcontroller is carried out on a byte-wise basis, using either an interrupt or polled handshake. Interface to either 80XX-type (e.g. MAB8048, MAB8051, Z80) or 68000-type buses is possible. Selection of bus type is automatically performed (see Section 6.2).

Table 1 Control signals utilized by the PCF8584 for microcontroller/microprocessor interfacing

TYPE	R/$\overline{W}$	$\overline{WR}$	$\overline{R}$	$\overline{DTACK}$	$\overline{IACK}$
8048/ 8051	no	yes	yes	no	no
68000	yes	no	no	yes	yes
Z80	no	yes	yes	no	yes

The structure of the PCF8584 is similar to that of the I²C-bus interface section of the MABXXXX/PCF84(C)XX-series of microcontrollers, but with a modified control structure. The PCF8584 has five internal register locations. Three of these (own address register S0', clock register S2 and interrupt vector S3) are used for initialization of the PCF8584. Normally they are only written once directly after resetting of the PCF8584.

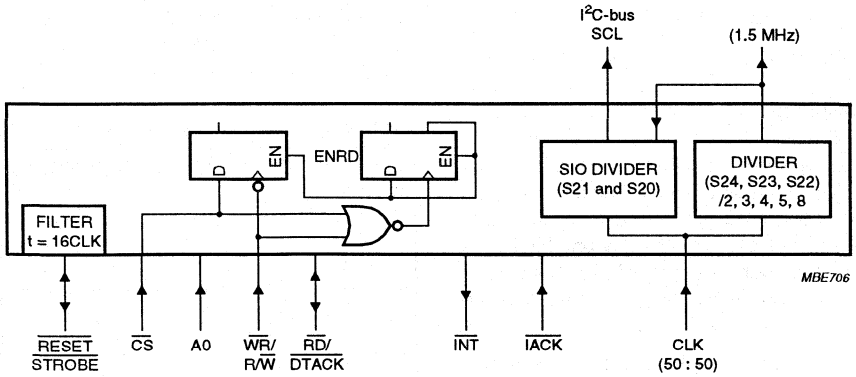
The remaining two registers function as double registers (data buffer/shift register S0, and control/status register S1) which are used during actual data transmission/reception. By using these double registers, which are separately write and read accessible, overhead for register access is reduced. Register S0 is a combination of a shift register and data buffer.

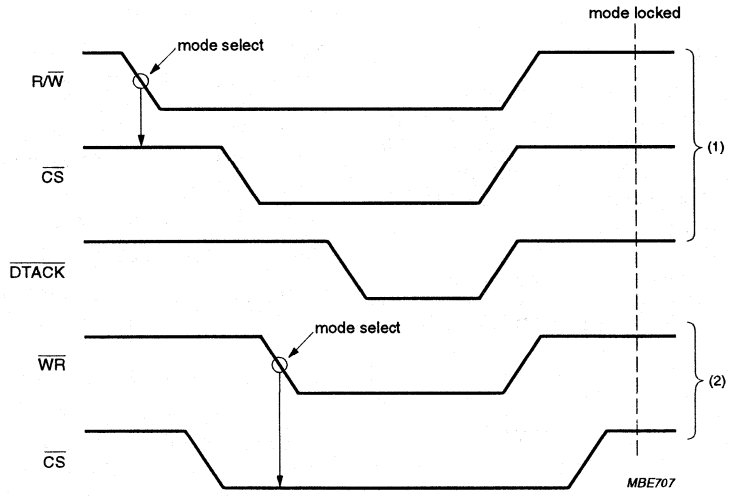
Register S0 performs all serial-to-parallel interfacing with the I²C-bus.

Register S1 contains I²C-bus status information required for bus access and/or monitoring.

6.2 Interface Mode Control (IMC)

Selection of either an 80XX mode or 68000 mode interface is achieved by detection of the first $\overline{WR}$-$\overline{CS}$ signal sequence. The concept takes advantage of the fact that the write control input is common for both types of interfaces. An 80XX-type interface is default. If a HIGH-to-LOW transition of $\overline{WR}$ (R/$\overline{W}$) is detected while $\overline{CS}$ is HIGH, the 68000-type interface mode is selected and the $\overline{DTACK}$ output is enabled. Care must be taken that $\overline{WR}$ and $\overline{CS}$ are stable after reset.





(1) Bus timing; 68000 mode write cycle.
(2) Bus timing; 80XX mode.

Fig.3 68000/80XX timing sequence utilized by the Interface Mode Control (IMC).

6.3 Set-up registers S0', S2 and S3

Registers S0', S2 and S3 are used for initialization of the PCF8584 (see Fig.5 'Initialization sequence' flowchart).

6.4 Own address register S0'

When the PCF8584 is addressed as slave, this register must be loaded with the 7-bit I²C-bus address to which the PCF8584 is to respond. During initialization, the own address register S0' must be written to, regardless whether it is later used. The Addressed As Slave (AAS) bit in status register S1 is set when this address is received (the value in S0 is compared with the value in S0'). Note that the S0 and S0' registers are offset by one bit; hence, programming the own address register S0' with a value of 55H will result in the value AAH being recognized as the PCF8584's slave address (see Fig.1).

Programming of S0' is accomplished via the parallel-bus when A0 is LOW, with the appropriate bit combinations set in control status register S1 (S1 is written when pin A0 = HIGH). Bit combinations for accessing all registers are given in Table 5. After reset, S0' has default address 00H (PCF8584 is thus initially in monitor mode, see Section 6.12).

6.5 Clock register S2

Register S2 provides control over chip clock frequency and SCL clock frequency. S20 and S21 provide a selection of 4 different I²C-bus SCL frequencies which are shown in Table 2. Note that these SCL frequencies are only obtained when bits S24, S23 and S22 are programmed to the correct input clock frequency (f_{clk}).

Table 2 Register S2 selection of SCL frequency

BIT		APPROXIMATE SCL FREQUENCY f_{SCL} (kHz)
S21	S20	
0	0	90
0	1	45
1	0	11
1	1	1.5

S22, S23 and S24 are used for control of the internal clock prescaler. Due to the possibility of varying microcontroller clock signals, the prescaler can be programmed to adapt to 5 different clock rates, thus providing a constant internal clock. This is required to provide a stable time base for the SCL generator and the digital filters associated with the I²C-bus signals SCL and SDA. Selection for adaption to external clock rates is shown in Table 3.

Programming of S2 is accomplished via the parallel-bus when A0 = LOW, with the appropriate bit combinations set in control status register S1 (S1 is written when A0 = HIGH). Bit combinations for accessing all registers are given in Table 5.

Table 3 Register S2 selection of clock frequency

INTERNAL CLOCK FREQUENCY			
S24	S23	S22	f_{clk} (MHz)
0	X(1)	X(1)	3
1	0	0	4.43
1	0	1	6
1	1	0	8
1	1	1	12

Note

1. X = don't care.

6.6 Interrupt vector S3

The interrupt vector register provides an 8-bit user-programmable vector for vectored-interrupt microcontrollers. The vector is sent to the bus port (DB7 to DB0) when an interrupt acknowledge signal is asserted and the ENI (enable interrupt) flag is set. Default vector values are:

- Vector is '00H' in 80XX mode
- Vector is '0FH' in 68000 mode.

On reset the PCF8584 is in the 80XX mode, thus the default interrupt vector is '00H'.

6.7 Data shift register/read buffer S0

Register S0 acts as serial shift register and read buffer interfacing to the I²C-bus. All read and write operations to/from the I²C-bus are done via this register. S0 is a combination of a shift register and a data buffer; parallel data is always written to the shift register, and read from the data buffer. I²C-bus data is always shifted in or out of shift register S0.

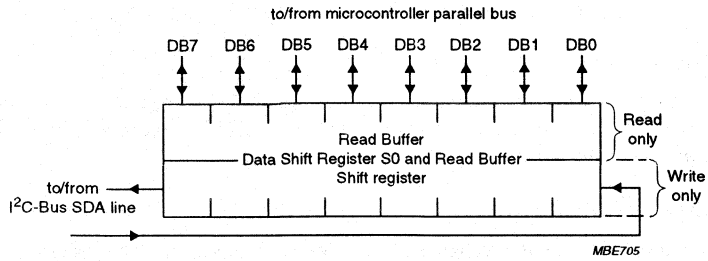


Fig.4 Data shift register/bus buffer S0.

In receiver mode the data from the shift register is copied to the read buffer during the acknowledge phase. Further reception of data is inhibited (SCL held LOW) until the S0 read buffer is read (see Section 6.8.1.1).

In the transmitter mode data is transmitted to the I²C-bus as soon as it is written to the S0 shift register if the serial I/O is enabled (ESO = 1).

Remarks:

1. A minimum of 6 clock cycles must elapse between consecutive parallel-bus accesses to the PCF8584 when the I²C-bus controller operates at 8 or 12 MHz. This may be reduced to 3 clock cycles for lower operating frequencies.
2. To start a read operation immediately after a write, it is necessary to read the S0 read buffer in order to invoke reception of the first byte ('dummy read' of the address). Immediately after the acknowledgement, this first byte will be transferred from the shift register to the read buffer. The **next** read will then transfer the correct value of the first byte to the microcontroller bus (see Fig.7).

6.8 Control/status register S1

Register S1 controls I²C-bus operation and provides I²C-bus status information. Register S1 is accessed by a HIGH signal on register select input A0. For more efficient communication between microcontroller/processor and the I²C-bus, register S1 has separate read and write functions for all bit positions (see Fig.3). The write-only section provides register access control and control over I²C-bus signals, while the read-only section provides I²C-bus status information.

Table 4 Control/status register S1

CONTROL/STATUS	BITS								MODE
Control[1]	PIN	ESO	ES1	ES2	ENI	STA	STO	ACK	write only
Status[2]	PIN	0[3]	STS	BER	AD0/ LRB	AAS	LAB	$\overline{BB}$	read only

Notes

1. For further information see Section 6.8.1.
2. For further information see Section 6.8.2.
3. Logic 1 if not-initialized.

6.8.1 REGISTER S1 CONTROL SECTION

The write-only section of S1 enables access to registers S0, S0', S1, S2 and S3, and controls I²C-bus operation; see Table 4.

6.8.1.1 PIN (Pending Interrupt Not)

When the PIN bit is written with a logic 1, all status bits are reset to logic 0. This may serve as a software reset function (see Figs 5 to 9). PIN is the only bit in S1 which may be both read and written to. PIN is mostly used as a status bit for synchronizing serial communication, see Section 6.8.2.

6.8.1.2 ESO (Enable Serial Output)

ESO enables or disables the serial I²C-bus I/O. When ESO is LOW, register access for initialization is possible. When ESO is HIGH, I²C-bus communication is enabled; communication with serial shift register S0 is enabled and the S1 bus status bits are made available for reading.

Table 5 Register access control; ESO = 0 (serial interface off) and ESO = 1 (serial interface on)

INTERNAL REGISTER ADDRESSING 2-WIRE MODE				
A0	**ES1**	**ES2**	**$\overline{\text{IACK}}$**	**FUNCTION**
ESO = 0; serial interface off(1)				
1	0	X	1(2)	R/W S1: control
0	0	0	1(2)	R/W S0': (own address)
0	0	1	1(2)	R/W S3: (interrupt vector)
0	1	0	1(2)	R/W S2: (clock register)
ESO = 0; serial interface on				
1	0	X	1	W S1: control
1	0	X	1	R S1; status
0	0	0	1	R/W S0: (data)
0	0	1	1	R/W S3: (interrupt vector)
X	0	X	0	R S3: (interrupt vector ACK cycle))

Notes

1. With ESO = 0, bits ENI, STA, STO and ACK of S1 can be read for test purposes.
2. 'X' if ENI = 0.

6.8.1.3 ES1 and ES2

ES1 and ES2 control selection of other registers for initialization and control of normal operation. After these bits are programmed for access to the desired register (shown in Table 5), the register is selected by a logic LOW level on register select pin A0.

6.8.1.4 ENI

This bit enables the external interrupt output $\overline{\text{INT}}$, which is generated when the PIN bit is active (logic 0).

This bit must be set to logic 0 before entering the long-distance mode, and remain at logic 0 during operation in long-distance mode.

6.8.1.5 STA and STO

These bits control the generation of the I²C-bus START condition and transmission of slave address and R/$\overline{W}$ bit, generation of repeated START condition, and generation of the STOP condition (see Table 7).

Table 6 Register access control; ESO = 1 (serial interface on) and ES1 = 1; long-distance (4-wire) mode; note 1

INTERNAL REGISTER ADDRESSING: LONG-DISTANCE (4-WIRE) MODE				
A0	**ES1**	**ES2**	**$\overline{IACK}$**	**FUNCTION**
1	1	X	1	W S1: control
1	1	X	X	R S1; status
0	1	X	X	R/W S0; (data)

Note

1. Trying to read from or write to registers other than S0 and S1 (setting ESO = 0) brings the PCF8584 out of the long-distance mode.

Table 7 Instruction table for serial bus control

STA	STO	PRESENT MODE	FUNCTION	OPERATION
1	0	SLV/REC	START	transmit START + address, remain MST/TRM if R/$\overline{W}$ = 0; go to MST/REC if R/$\overline{W}$ = 1
1	0	MST/TRM	REPEAT START	same as for SLV/REC
0	1	MST/REC; MST/TRM	STOP READ; STOP WRITE	transmit STOP go to SLV/REC mode; note 1
1	1	MST	DATA CHAINING	send STOP, START and address after last master frame without STOP sent; note 2
0	0	ANY	NOP	no operation; note 3

Notes

1. In master receiver mode, the last byte must be terminated with ACK bit HIGH ('negative acknowledge').
2. If both STA and STO are set HIGH simultaneously in master mode, a STOP condition followed by a START condition + address will be generated. This allows 'chaining' of transmissions without relinquishing bus control.
3. All other STA and STO mode combinations not mentioned in Table 7 are NOPs.

6.8.1.6 ACK

This bit must be set normally to a logic 1. This causes the I²C-bus controller to send an acknowledge automatically after each byte (this occurs during the 9th clock pulse). The bit must be reset (to logic 0) when the I²C-bus controller is operating in master/receiver mode and requires no further data to be sent from the slave transmitter. This causes a negative acknowledge on the I²C-bus, which halts further transmission from the slave device.

6.8.2 REGISTER S1 STATUS SECTION

The read-only section of S1 enables access to I²C-bus status information; see Table 4.

6.8.2.1 PIN bit

'Pending Interrupt Not' (MSB of register S1) is a status flag which is used to synchronize serial communication and is set to logic 0 whenever the PCF8584 requires servicing. The PIN bit is normally read in polled applications to determine when an I²C-bus byte transmission/reception is completed. The PIN bit may also be written, see Section 6.8.1.

Each time a serial data transmission is initiated (by setting the STA bit in the same register), the PIN bit will be set to logic 1 automatically (inactive). When acting as transmitter, PIN is also set to logic 1 (inactive) each time S0 is written. In receiver mode, the PIN bit is automatically set to logic 1 (inactive) each time the data register S0 is read.

After transmission or reception of one byte on the I²C-bus (9 clock pulses, including acknowledge), the PIN bit will be automatically reset to logic 0 (active) indicating a complete byte transmission/reception. When the PIN bit is subsequently set to logic 1 (inactive), all status bits will be reset to logic 0. PIN is also set to zero on a BER (bus error) condition.

In polled applications, the PIN bit is tested to determine when a serial transmission/reception has been completed. When the ENI bit (bit 4 of write-only section of register S1) is also set to logic 1 the hardware interrupt is enabled. In this case, the PIN flag also triggers an external interrupt (active LOW) via the $\overline{INT}$ output each time PIN is reset to logic 0 (active).

When acting as slave transmitter or slave receiver, while PIN = 0, the PCF8584 will suspend I²C-bus transmission by holding the SCL line LOW until the PIN bit is set to logic 1 (inactive). This prevents further data from being transmitted or received until the current data byte in S0 has been read (when acting as slave receiver) or the next data byte is written to S0 (when acting as slave transmitter).

PIN bit summary:

- The PIN bit can be used in polled applications to test when a serial transmission has been completed. When the ENI bit is also set, the PIN flag sets the external interrupt via the $\overline{INT}$ output.
- Setting the STA bit (start bit) will set PIN = 1 (inactive).
- In transmitter mode, after successful transmission of one byte on the I²C-bus the PIN bit will be automatically reset to logic 0 (active) indicating a complete byte transmission.
- In transmitter mode, PIN is set to logic 1 (inactive) each time register S0 is written.
- In receiver mode, PIN is set to logic 0 (active) on completion of each received byte. Subsequently, the SCL line will be held LOW until PIN is set to logic 1.
- In receiver mode, when register S0 is read, PIN is set to logic 1 (inactive).
- In slave receiver mode, an I²C-bus STOP condition will set PIN = 0 (active).
- PIN = 0 if a bus error (BER) occurs.

6.8.2.2 STS

When in slave receiver mode, this flag is asserted when an externally generated STOP condition is detected (used only in slave receiver mode).

6.8.2.3 BER

Bus error; a misplaced START or STOP condition has been detected. Resets $\overline{BB}$ (to logic 1; inactive), sets PIN = 0 (active).

6.8.2.4 LRB/AD0

'Last Received Bit' or 'Address 0 (General Call) bit'. This status bit serves a dual function, and is valid only while PIN = 0:

1. LRB holds the value of the last received bit over the I²C-bus while AAS = 0 (not addressed as slave). Normally this will be the value of the slave acknowledgement; thus checking for slave acknowledgement is done via testing of the LRB.
2. AD0; when AAS = 1 ('Addressed As Slave' condition), the I²C-bus controller has been addressed as a slave. Under this condition, this bit becomes the 'AD0' bit and will be set to logic 1 if the slave address received was the 'general call' (00H) address, or logic 0 if it was the I²C-bus controller's own slave address.

6.8.2.5 AAS

'Addressed As Slave' bit. Valid only when PIN = 0. When acting as slave receiver, this flag is set when an incoming address over the I²C-bus matches the value in own address register S0' (shifted by one bit, see Section 6.4), or if the I²C-bus 'General Call' address (00H) has been received ('General Call' is indicated when AD0 status bit is also set to logic 1, see Section 6.8.2.4).

6.8.2.6 LAB

'Lost Arbitration' Bit. This bit is set when, in multi-master operation, arbitration is lost to another master on the I²C-bus.

6.8.2.7 $\overline{BB}$

'Bus Busy' bit. This is a read-only flag indicating when the I²C-bus is in use. A zero indicates that the bus is busy, and access is not possible. This bit is set/reset (logic 1/logic 0) by STOP/START conditions.

6.9 Multi-master operation

To avoid conflict between data and repeated START and STOP operations, multi-master systems have some limitations:

- When powering up multiple PCF8584s in multi-master systems, the possibility exists that one node may power up slightly after another node has already begun an I²C-bus transmission; the Bus Busy condition will thus not have been detected. To avoid this condition, a delay should be introduced in the initialization sequence of each PCF8584 equal to the longest I²C-bus transmission, see flowchart 'PCF8584 initialization' (Fig.5).

6.10 Reset

A LOW level pulse on the $\overline{RESET}$ input forces the I²C-bus controller into a well-defined state. All flags in S1 are reset to logic 0, except the PIN flag, which is set to logic 1. S0' and S3 are set to 00H.

The $\overline{RESET}$ pin is also used for the $\overline{STROBE}$ output signal. Both functions are separated on-chip by a digital filter. The reset input signal has to be sufficiently long (minimum 30 clock cycles) to pass through the filter. The $\overline{STROBE}$ output signal is sufficiently short (8 clock cycles) to be blocked by the filter. For more detailed information on the strobe function see Section 6.12.

6.11 Comparison to the MAB8400 I²C-bus interface

The structure of the PCF8584 is similar to that of the MAB8400 series of microcontrollers, but with a modified control structure. Access to all I²C-bus control and status registers is done via the parallel-bus port in conjunction with register select input A0, and control bits ESO, ES1 and ES2.

6.11.1 DELETED FUNCTIONS

The following functions are not available in the PCF8584:

- Always selected (ALS flag)
- Access to the bit counter (BC0 to BC2)
- Full SCL frequency selection (2 bits instead of 5 bits)
- The non-acknowledge mode (ACK flag)
- Asymmetrical clock (ASC flag).

6.11.2 ADDED FUNCTIONS

The following functions either replace the deleted functions or are completely new:

- Chip clock prescaler
- Assert acknowledge bit (ACK flag)
- Register selection bits (ES1 and ES2 flags)
- Additional status flags (BER, 'bus error')
- Automatic interface control between 80XX and 68000-type microcontrollers
- Programmable interrupt vector
- Strobe generator
- Bus monitor function
- Long-distance mode [non-I²C-bus mode (4-wire); only for communication between parallel-bus processors using the PCF8584 at each interface point].

6.12 Special function modes

6.12.1 STROBE

When the I²C-bus controller receives its own address (or the '00H' general call address) followed immediately by a STOP condition (i.e. no further data transmitted after the address), a strobe output signal is generated at the $\overline{RESET}$/$\overline{STROBE}$ pin (pin 19). The $\overline{STROBE}$ signal consists of a monostable output pulse (active LOW), 8 clock cycles long (see Fig.9). It is generated after the STOP condition is received, preceded by the correct slave address. This output can be used as a bus access controller for multi-master parallel-bus systems.

6.12.2 LONG-DISTANCE MODE

The long-distance mode provides the possibility of longer-distance serial communication between parallel processors via two I²C-bus controllers. This mode is selected by setting ES1 to logic 1 while the serial interface is enabled (ESO = 1).

In this mode the I²C-bus protocol is transmitted over 4 unidirectional lines, SDA OUT, SCL IN, SDA IN and SCL IN (pins 2, 3, 4 and 5). These communication lines should be connected to line drivers/receivers (example: RS422) for long-distance applications. Hardware characteristics for long-distance transmission are then given by the chosen standard. Control of data transmission is the same as in normal I²C-bus mode. After reading or writing data to shift register S0, long-distance mode must be initialized by setting $\overline{\text{ESO}}$ and ES1 to logic 1. Because the interrupt output $\overline{\text{INT}}$ is not available in this operating mode, synchronization of data transmission/reception must be polled via the PIN bit.

Remarks:

Before entering the long-distance mode, ENI must be set to logic 0.

When powering up an PCF8584-node in long-distance mode, the PCF8584 must be isolated from the 4-wire bus via 3-state line drivers/receivers until the PCF8584 is properly initialized for long-distance mode. Failure to implement this precaution will result in system malfunction.

6.12.3 MONITOR MODE

When the 7-bit own address register S0' is loaded with all zeros, the I²C-bus controller acts as a passive I²C monitor. The main features of the monitor mode are:

- The controller is always selected.
- The controller is always in the slave receiver mode.
- The controller never generates an acknowledge.
- The controller never generates an interrupt request.
- A pending interrupt condition does not force SCL LOW.
- $\overline{\text{BB}}$ is set to logic 0 after detection of a START condition, and reset to logic 1 after a STOP condition.
- Received data is automatically transferred to the read buffer.
- Bus traffic is monitored by the PIN bit, which is reset to logic 0 after the acknowledge bit of an incoming byte has been received, and is set to logic 1 as soon as the first bit of the next incoming byte is detected. Reading the data buffer S0 sets the PIN bit to logic 1. Data in the read buffer is valid from PIN = 0 and during the next 8 clock pulses (until next acknowledge).
- AAS is set to logic 1 at every START condition, and reset at every 9th clock pulse.

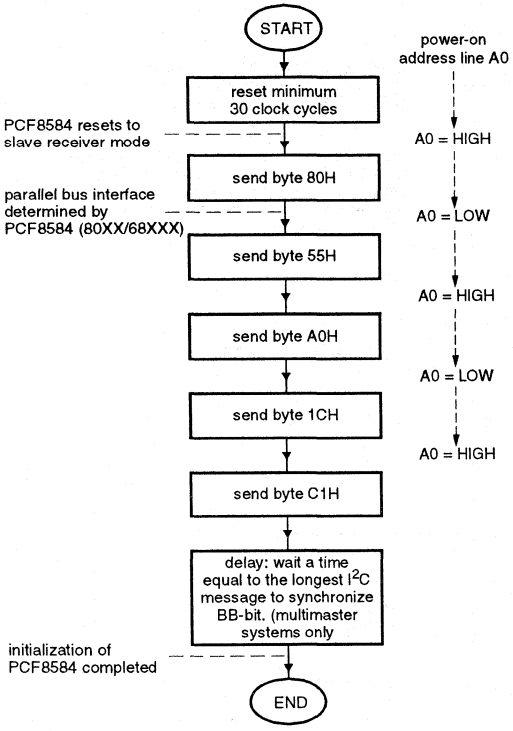
7 SOFTWARE FLOWCHART EXAMPLES

7.1 Initialization

The flowchart of Fig.5 gives an example of a proper initialization sequence of the PCF8584. When implemented in 808X-type bus systems with peripherals sharing a common $\overline{\text{WR}}$ signal, this procedure should be executed first before communicating with other bus peripherals to avoid false programming of the PCF8584 (see Section 6.2)

7.2 Implementation

The flowcharts (Figs 6 to 9) illustrate proper programming sequences for implementing master transmitter, master receive, and master transmitter, repeated start and master receiver modes in polled applications.



A0 = HIGH	enables data transfer to/from register S1
A0 = LOW	Access to all other registers defined by the bit pattern in register S1

Loads byte 80H into register S1, i.e. next byte will be loaded into register S0 (own address register); serial interface off.

Loads byte 55H into register S0'; effective own address becomes AAH.

Loads byte A0H into register S1, i.e. next byte will be loaded into the clock control register S2.

Loads byte 1CH into register S2; system clock is 12 MHz; SCL = 90 kHz.

Loads byte C1H into register S1; register enable serial interface, set I²C-bus into idle mode; SDA and SCL are HIGH. The next write or read operation will be to/from data transfer register S0 if A0 = LOW.

On power-on, if an PCF8584 node is powered-up slightly after another node has already begun an I²C-bus transmission, the bus busy condition will not have been detected. Thus, introducing this delay will insure that this condition will not occur.

MBE714

Fig.5 PCF8584 initialization sequence.

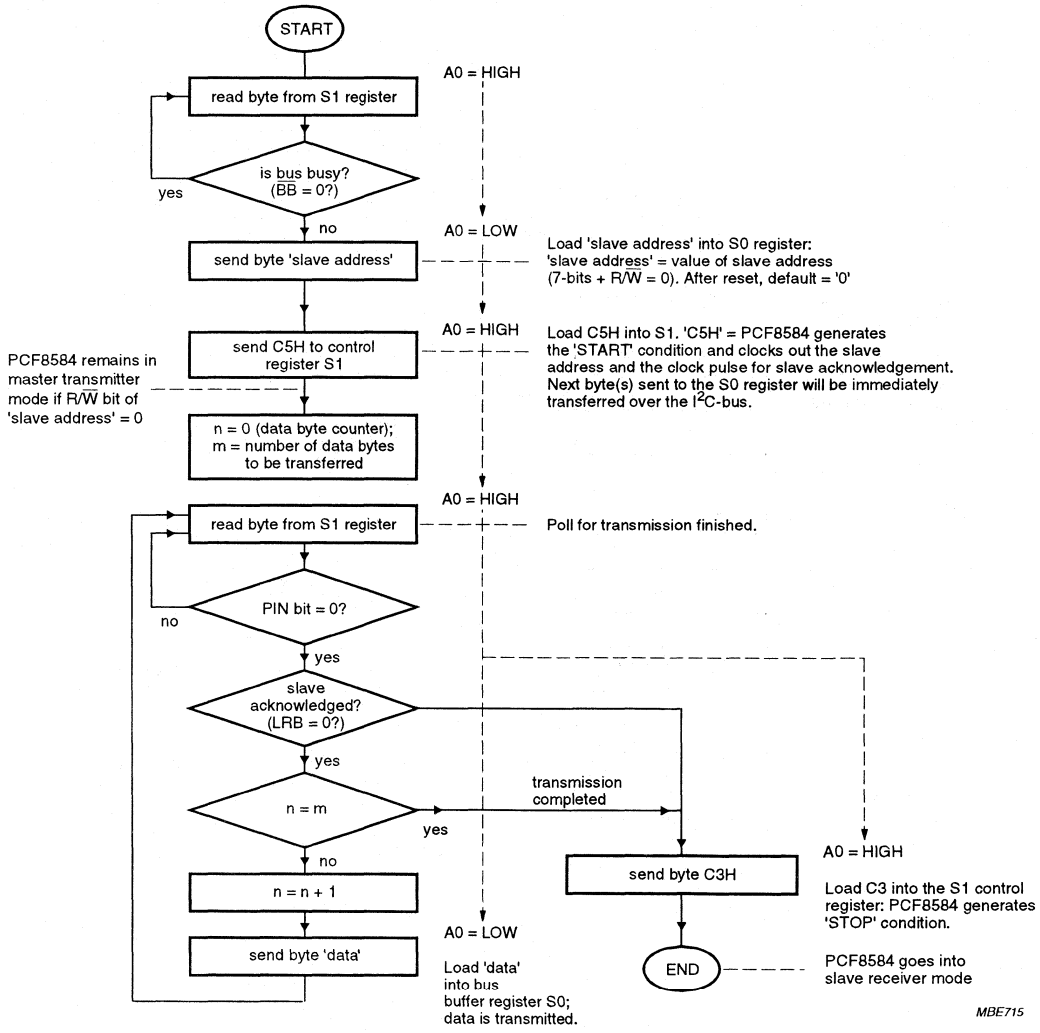


Fig.6 PCF8584 master transmitter mode.

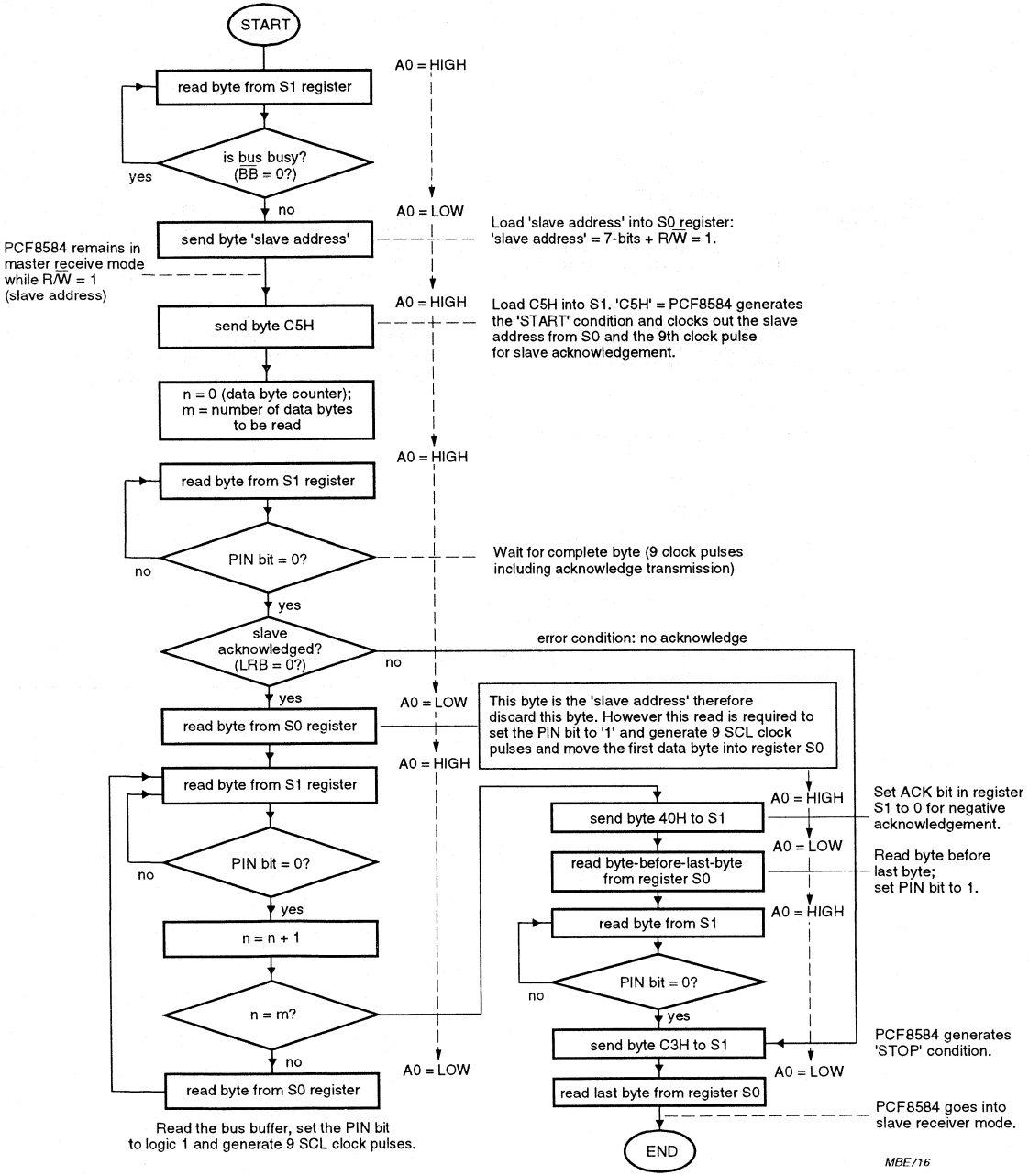


Fig.7 PCF8584 master receiver mode.

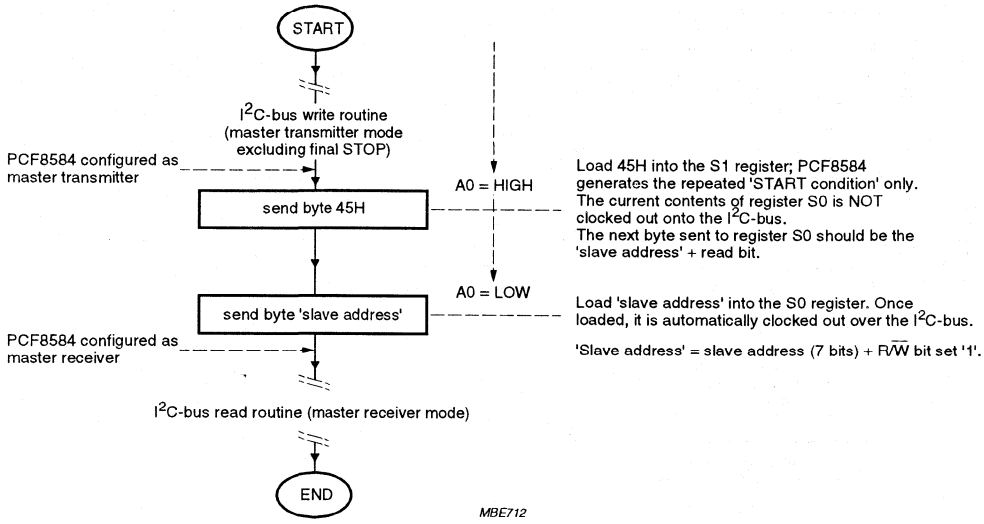


Fig.8 Master transmitter followed by repeated START and becoming master receiver.

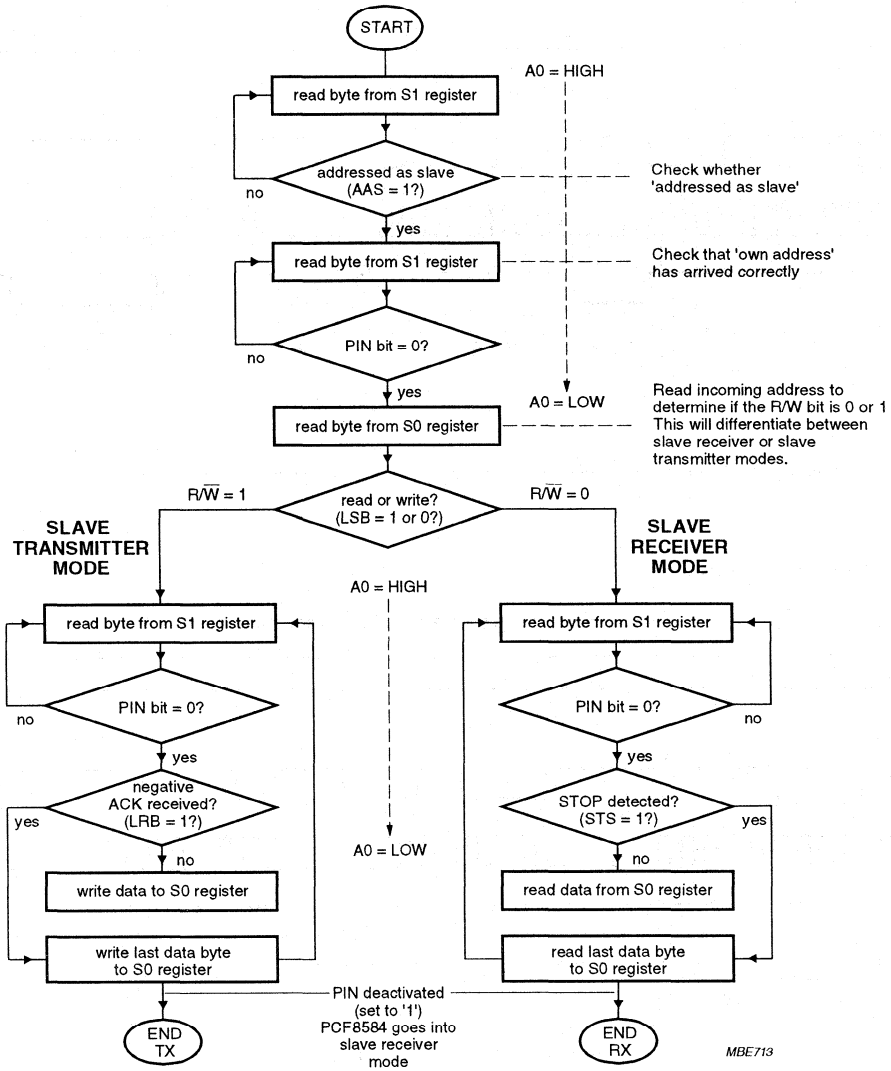
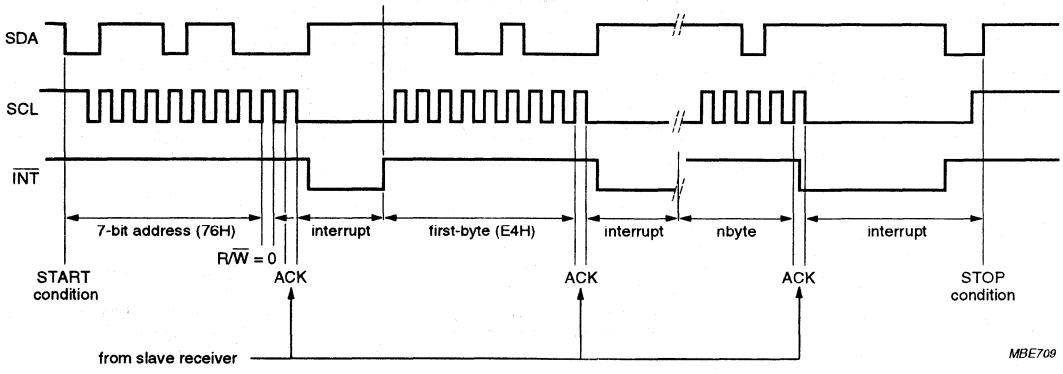


Fig.9 Slave receiver/slave transmitter modes.

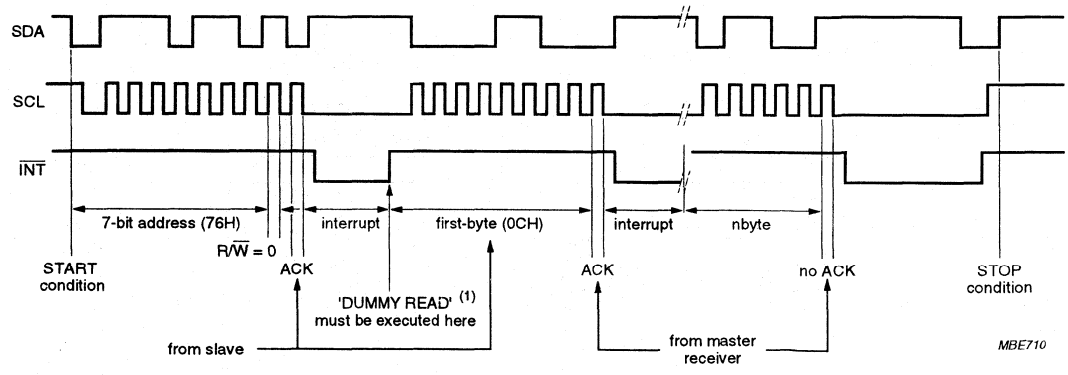
8 I²C-BUS TIMING DIAGRAMS

The diagrams (Figs 10 to 13) illustrate typical timing diagrams for the PCF8584 in master/slave functions. For detailed description of the I²C-bus protocol, please refer to *"The I²C-bus and how to use it"*; Philips document ordering number 9398 393 40011.



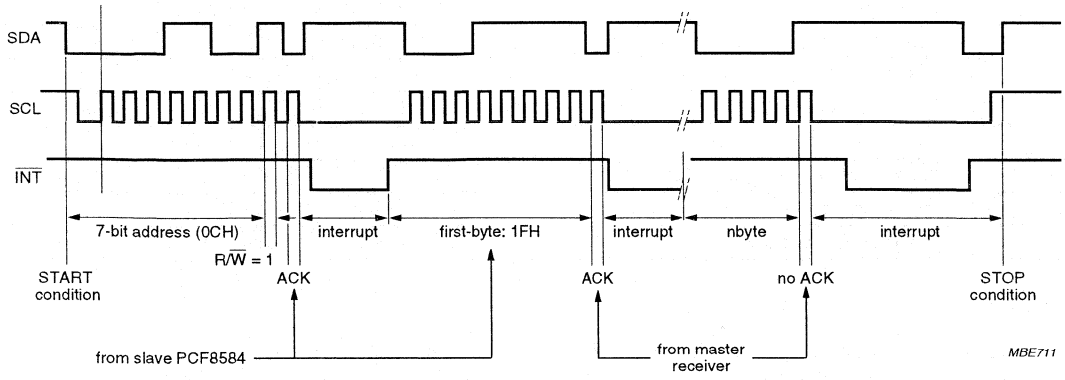
Master PCF8584 writes data to slave receiver.

Fig.10 Bus timing diagram; master transmitter mode.



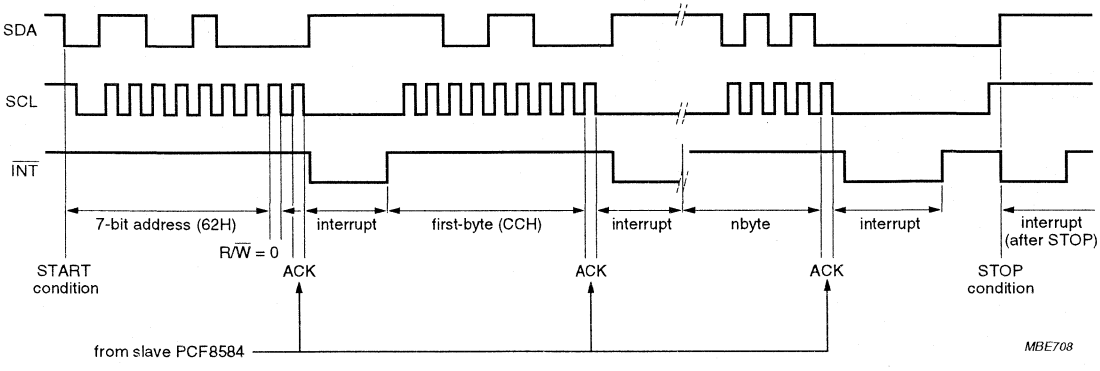
Master PCF8584 reads data from slave receiver.

Fig.11 Bus timing diagram; master receiver mode.



External master receiver reads data from PCF8584.

Fig.12 Bus timing diagram; slave transmitter mode.



Slave PCF8584 is written to by external master transmitter.

Fig.13 Bus timing diagram; slave receiver mode.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.3	+7.0	V
V_I	voltage range (any input)	−0.8	V_{DD} + 0.5	V
I_I	DC input current (any input)	−10	+10	mA
I_O	DC output current (any output)	−10	+10	mA
P_{tot}	total power dissipation	−	300	mW
P_O	power dissipation per output	−	50	mW
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

11 DC CHARACTERISTICS

V_{DD} = 5 V ±10%; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		4.5	5.0	5.5	V
I_{DD}	supply current	standby; note 1	–	–	2.5	μA
		operating; notes 1 and 2	–	–	1.5	mA
Inputs						
CLK, $\overline{IACK}$, A0, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{RESET}$ AND D0 to D7						
V_{IL}	LOW level input voltage	note 3	0	–	0.8	V
V_{IH}	HIGH level input voltage	note 3	2.0	–	V_{DD}	V
SDA AND SCL						
V_{IL}	LOW level input voltage	note 4	0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	note 4	$0.7V_{DD}$	–	V_{DD}	V
R_i	resistance to V_{DD}	T_{amb} = 25 °C; note 5	25	–	100	kΩ
Outputs						
I_{OL}	LOW level output current	V_{OH} = 2.4 V; note 6	−2.4	–	–	mA
I_{OH}	HIGH level output current	V_{OL} = 0.4 V; note 6	3.0	–	–	mA
I_{OL}	leakage current	note 7	−1	–	+1	μA

Notes

1. Test conditions: 22 kΩ pull-up resistors on D0 to D7; 10 kΩ pull-up resistors on SDA, SCL, $\overline{RD}$; $\overline{RESET}$ connected to V_{SS}; remaining pins open-circuit.
2. CLK waveform of 12 MHz with 50% duty factor.
3. CLK, $\overline{IACK}$, A0, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{RESET}$ and D0 to D7 are TTL level inputs.
4. SDA and SCL are CMOS level inputs.
5. CLK, $\overline{IACK}$, A0, $\overline{CS}$ and $\overline{WR}$.
6. D0 to D7.
7. D0 to D7 3-state, SDA, SCL, $\overline{INT}$, $\overline{RD}$, $\overline{RESET}$.

12 I²C-BUS TIMING SPECIFICATIONS

All the timing limits are valid within the operating supply voltage and ambient temperature range; V_{DD} = 5 V ±10%; T_{amb} = −40 to +85 °C; and refer to V_{IL} and V_{IH} with an input voltage of V_{SS} to V_{DD}.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
f_{SCL}	SCL clock frequency	–	–	100	kHz
t_{SW}	tolerable spike width on bus	–	–	100	ns
t_{BUF}	bus free time	4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time	4.7	–	–	µs
$t_{HD;STA}$	START condition hold time	4.0	–	–	µs
t_{LOW}	SCL LOW time	4.7	–	–	µs
t_{HIGH}	SCL HIGH time	4.0	–	–	µs
t_r	SCL and SDA rise time	–	–	1.0	µs
t_f	SCL and SDA fall time	–	–	0.3	µs
$t_{SU;DAT}$	data set-up time	250	–	–	ns
$t_{HD;DAT}$	data hold time	0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid	–	–	3.4	µs
$t_{SU;STO}$	STOP condition set-up time	4.0	–	–	µs

13 PARALLEL INTERFACE TIMING

All the timing limits are valid within the operating supply voltage and ambient temperature range: V_{DD} = 5 V ±10%; T_{amb} = −40 to +85 °C; and refer to V_{IL} and V_{IH} with an input voltage of V_{SS} to V_{DD}. C_L = 100 pF; R_L = 1.5 kΩ (connected to V_{DD}) for open-drain and high-impedance outputs, where applicable (for measurement purposes only).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	clock rise time	see Fig.14	–	–	6	ns
t_f	clock fall time	see Fig.14	–	–	6	ns
t_{CLK}	input clock period (50% ±5% duty factor)	see Fig.14	83	–	333	ns
t_{CLRL}	$\overline{CS}$ set-up to $\overline{RD}$ LOW	see Fig.16 and note 1	20	–	–	ns
t_{CLWL}	$\overline{CS}$ set-up to $\overline{WR}$ LOW	see Fig.15 and note 1	20	–	–	ns
t_{RHCH}	$\overline{CS}$ hold from $\overline{RD}$ HIGH	see Fig.16	0	–	–	ns
t_{WHCH}	$\overline{CS}$ hold from $\overline{WR}$ HIGH	see Fig.15	0	–	–	ns
t_{AVWL}	A0 set-up to $\overline{WR}$ LOW	see Fig.15	10	–	–	ns
t_{AVRL}	A0 set-up to $\overline{RD}$ LOW	see Fig.16	10	–	–	ns
t_{WHAI}	A0 hold from $\overline{WR}$ HIGH	see Fig.15	20	–	–	ns
t_{RHAI}	A0 hold from $\overline{RD}$ HIGH	see Fig.16	10	–	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	see Fig.15	250	–	1000	ns
t_{RLRH}	$\overline{RD}$ pulse width	see Fig.16	250	–	1000	ns
t_{DVWH}	data set-up before $\overline{WR}$ HIGH	see Fig.15	150	–	–	ns
t_{RLDV}	data valid after $\overline{RD}$ LOW	see Fig.16	–	160	230	ns
t_{WHDI}	data hold after $\overline{WR}$ HIGH	see Fig.15	20	–	–	ns
t_{RHDF}	data bus floating after $\overline{RD}$ HIGH	see Fig.16 and note 4	–	160	180	ns
t_{AVCL}	A0 set-up to $\overline{CS}$ LOW	see Figs 17 and 18	10	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{WLCL}	R/$\overline{WR}$ set-up to $\overline{CS}$ LOW	see Fig.17	10	–	–	ns
t_{RHCL}	R/$\overline{WR}$ set-up to $\overline{CS}$ LOW	see Fig.18	10	–	–	ns
t_{CLDV}	data valid after $\overline{CS}$ LOW	see Fig.18 and note 3	–	160	230	ns
t_{CLDL}	$\overline{DTACK}$ LOW after $\overline{CS}$ LOW	see Figs 17 and 18	–	$2t_{CLK}$ + 75	$3t_{CLK}$ + 150	ns
t_{CHAI}	A0 hold from $\overline{CS}$ HIGH	see Fig.18	0	–	–	ns
t_{CHRL}	R/$\overline{WR}$ hold from $\overline{CS}$ HIGH	see Fig.18	0	–	–	ns
t_{CHWH}	R/$\overline{WR}$ hold from $\overline{CS}$ HIGH	see Fig.17	0	–	–	ns
t_{CHDF}	data bus float after $\overline{CS}$ HIGH	see Fig.18 and note 4	–	160	180	ns
t_{CHDE}	$\overline{DTACK}$ HIGH from $\overline{CS}$ HIGH	see Figs 17 and 18	–	100	120	ns
t_{CHDI}	data hold after $\overline{CS}$ HIGH	see Fig.17 and note 4	0	–	–	ns
t_{DVCL}	data set-up to $\overline{CS}$ LOW	see Fig.17	0	–	–	ns
t_{ALIE}	$\overline{INT}$ HIGH from $\overline{IACK}$ LOW	see Figs 19 and 20	–	130	180	ns
t_{ALDV}	data valid after $\overline{IACK}$ LOW	see Figs 19 and 20	–	200	250	ns
t_{ALAE}	$\overline{IACK}$ pulse width	see Fig.20	280	–	–	ns
t_{AHDI}	data hold after $\overline{IACK}$ HIGH	see Fig.20	–	–	150	ns
t_{ALDL}	$\overline{DTACK}$ LOW from $\overline{IACK}$ LOW	see Fig.20	–	$2t_{CLK}$ + 75	$3t_{CLK}$ + 150	ns
t_{AHDE}	$\overline{DTACK}$ HIGH from $\overline{IACK}$ HIGH	see Fig.20	–	120	140	ns
t_{W4}	$\overline{RESET}$ pulse width	see Fig.21	$30t_{CLK}$	–	–	ns
t_{W5}	$\overline{STROBE}$ pulse width	see Fig.22	$8t_{CLK}$	$8t_{CLK}$ + 90	–	ns
t_{CLCL}	$\overline{CS}$ LOW	see Figs 17 and 18	–	t_{CLDL} + t_{CHDE}	–	ns

Notes

1. A minimum of 6 clock cycles must elapse between consecutive parallel-bus accesses when the I²C-bus controller operates at 8 or 12 MHz. This may be reduced to 3 clock cycles for lower operating frequencies.
2. After reset the chip clock default is 12 MHz.
3. Not for S1.
4. Not tested.

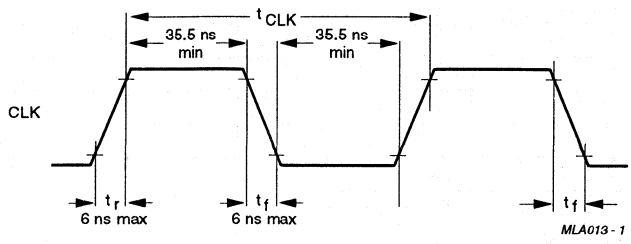


Fig.14 Clock input timing.

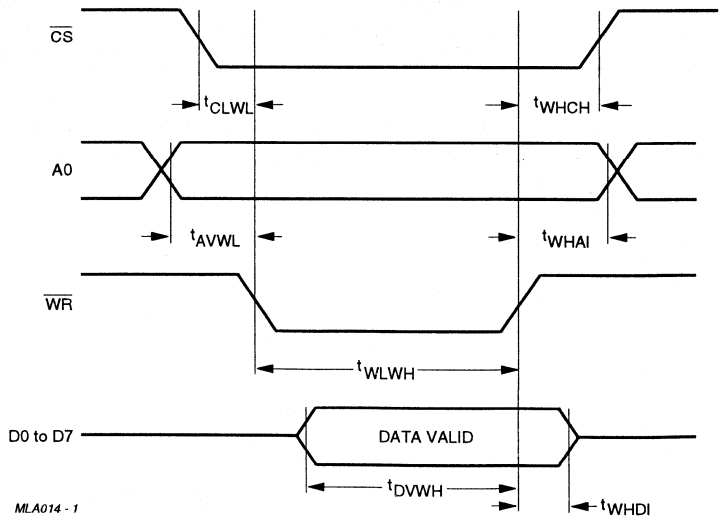


Fig.15 Bus timing (80XX mode); write cycle.

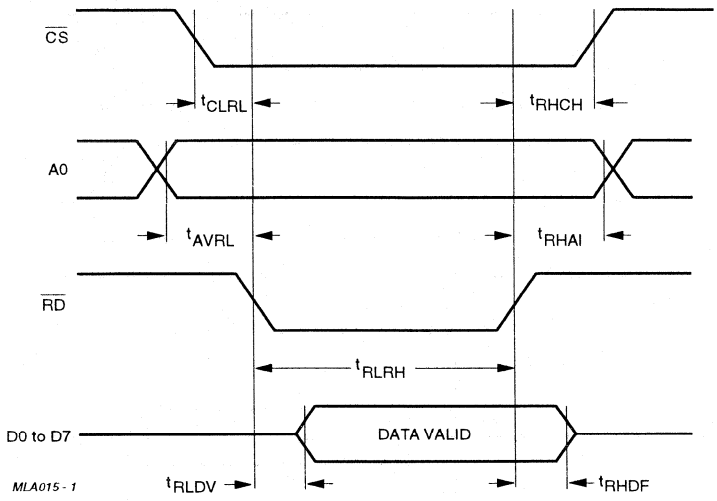


Fig.16 Bus timing (80XX mode); read cycle.

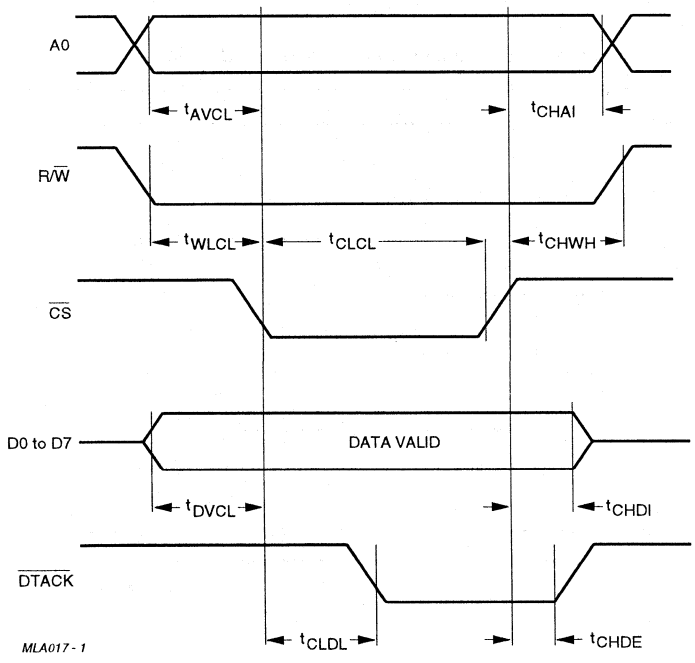


Fig.17 Bus timing (68000 mode); write cycle.

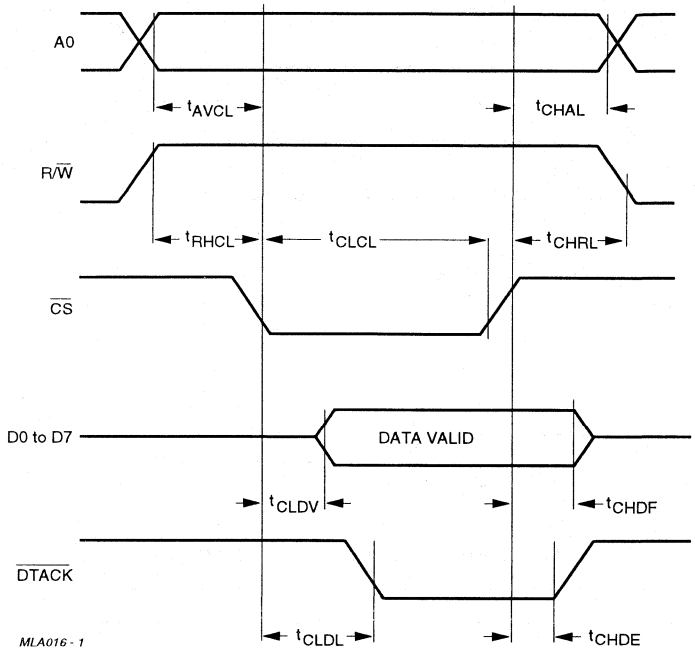


Fig.18 Bus timing (68000 mode); read cycle.

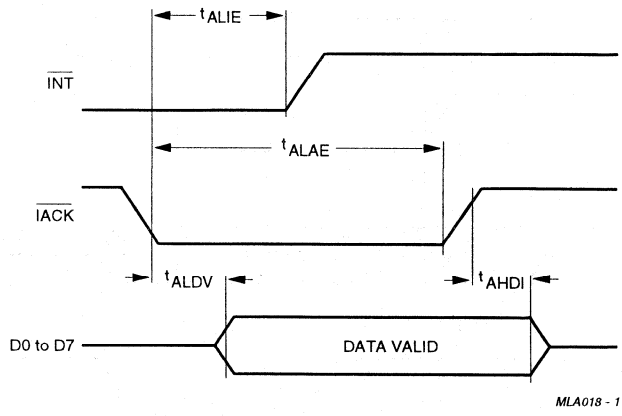


Fig.19 Interrupt timing (80XX mode).

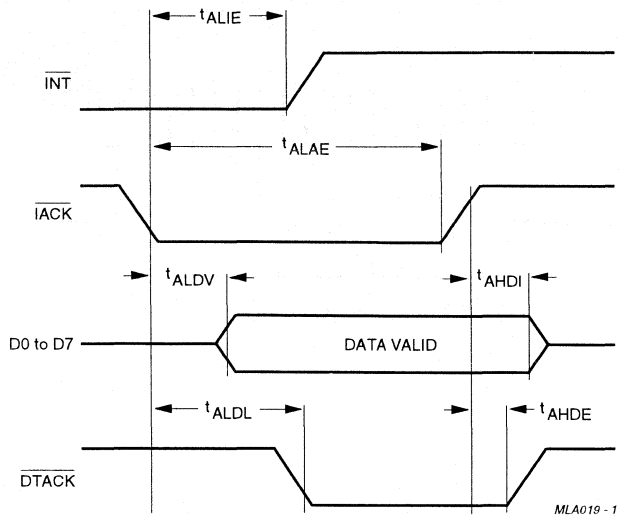


Fig.20 Interrupt timing (68000 mode).

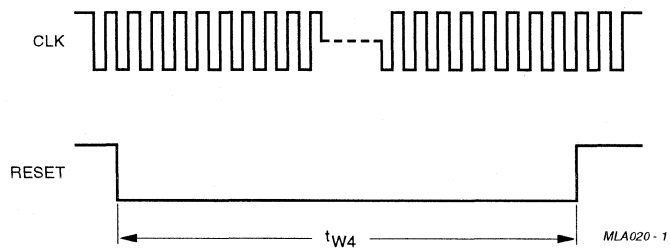


Fig.21 Reset timing.

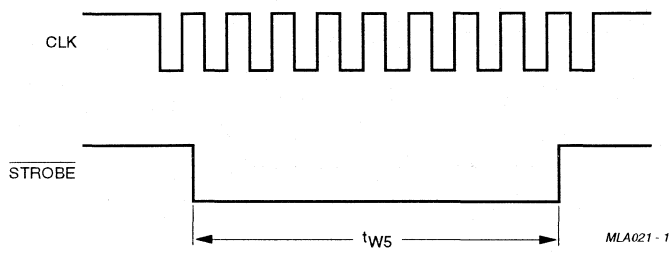


Fig.22 Strobe timing.

14 APPLICATION INFORMATION

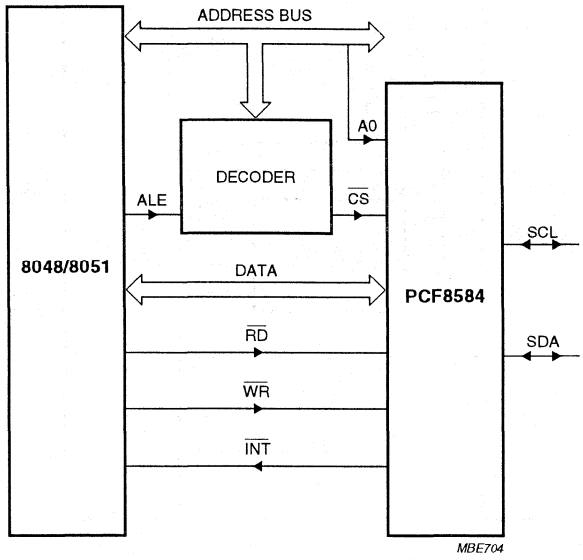


Fig.23 Application diagram using the 8048/8051.

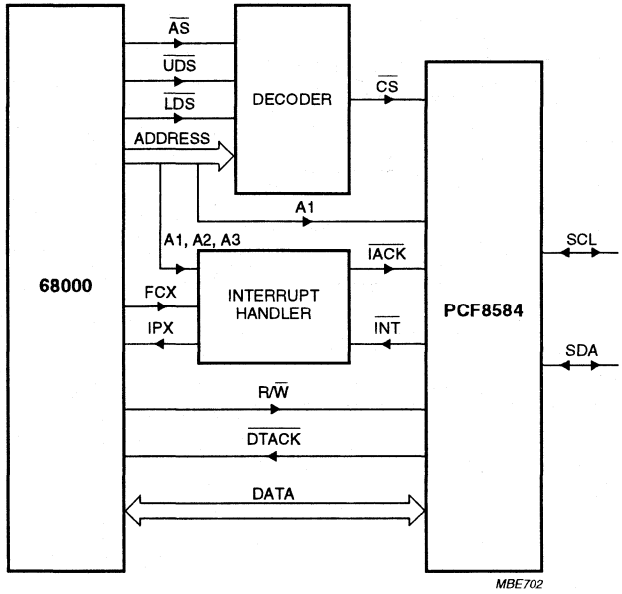


Fig.24 Application diagram using the 68000.

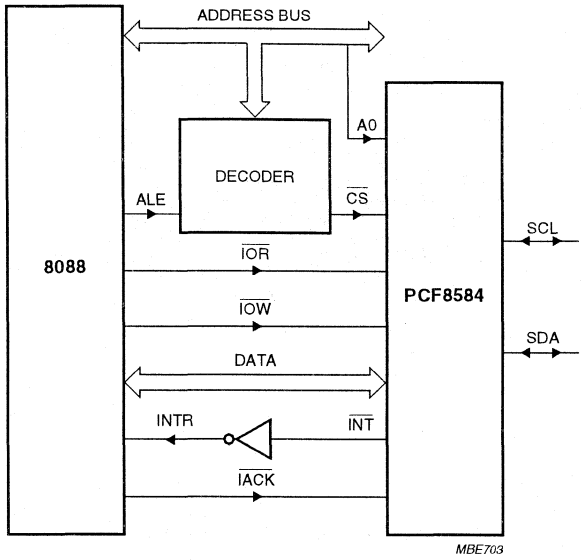
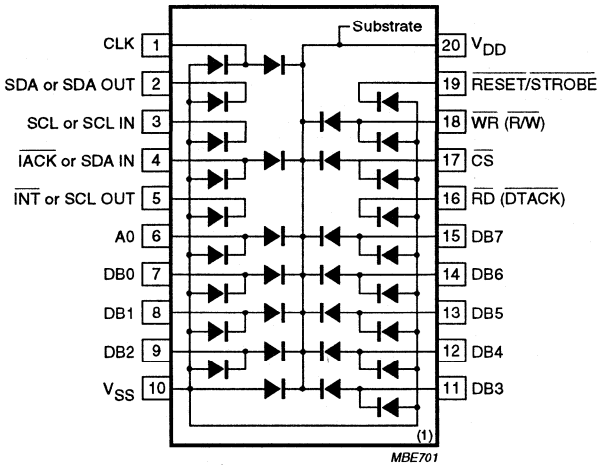


Fig.25 Application diagram using the 8088.



Maximum forward current: 5 mA; maximum reverse voltage: 5 V.

Fig.26 PCF8584 diode protection.

8-BIT A/D AND D/A CONVERTER

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I^2C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I^2C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I^2C bus.

Features

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I^2C bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P:16-lead DIL; plastic (SOT38).
PCF8591T:16-lead mini-pack; plastic (SO16L; SOT162A).

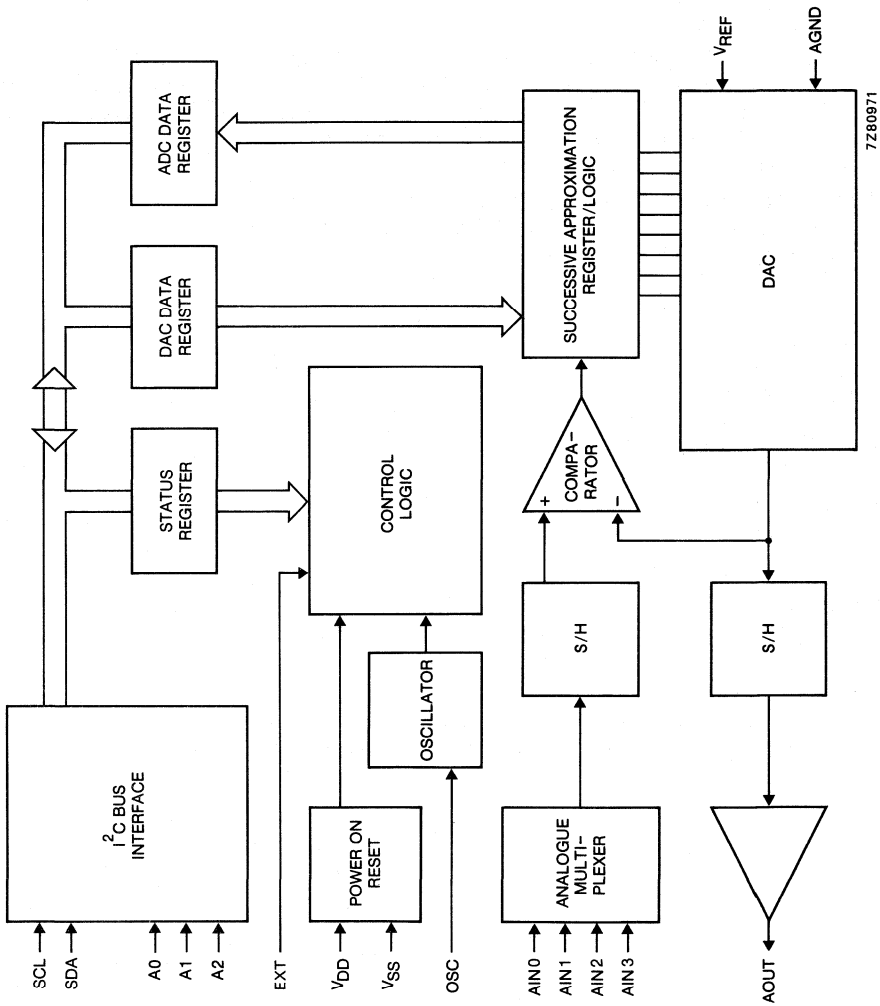


Fig. 1 Block diagram.

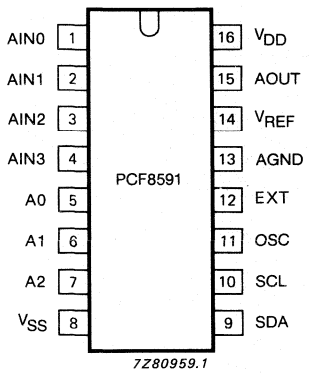


Fig. 2 Pinning diagram.

PINNING

1.	AIN0	analogue inputs (A/D converter)
2.	AIN1	
3.	AIN2	
4.	AIN3	
5.	A0	hardware address
6.	A1	
7.	A2	
8.	V_{SS}	negative supply voltage
9.	SDA	I^2C bus data input/output
10.	SCL	I^2C bus clock input/output
11.	OSC	oscillator input/output
12.	EXT	external/internal switch for oscillator input
13.	AGND	analogue ground
14.	V_{REF}	voltage reference input
15.	AOUT	analogue output (D/A converter)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Adressing

Each PCF8591 device in an I^2C bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address always has to be sent as the first byte after the start condition in the I^2C bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Figs 3 and 10).

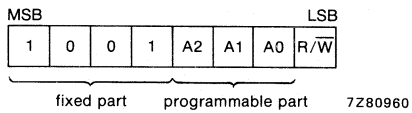


Fig. 3 Address byte.

Control byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function.

The upper nibble of the control register is used for enabling the analogue output, and for programming the analogue inputs as single-ended or differential inputs. The lower nibble selects one of the analogue input channels defined by the upper nibble (see Fig. 4). If the auto-increment flag is set the channel number is incremented automatically after each A/D conversion.

If the auto-increment mode is desired in applications where the internal oscillator is used, the analogue output enable flag in the control byte (bit 6) should be set. This allows the internal oscillator to run continuously, thereby preventing conversion errors resulting from oscillator start-up delay. The analogue output enable flag may be reset at other times to reduce quiescent power consumption.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will be always channel 0. The most significant bits of both nibbles are reserved for future functions and have to be set to 0. After a power-on reset condition all bits of the control register are reset to 0. The D/A converter and the oscillator are disabled for power saving. The analogue output is switched to a high impedance state.

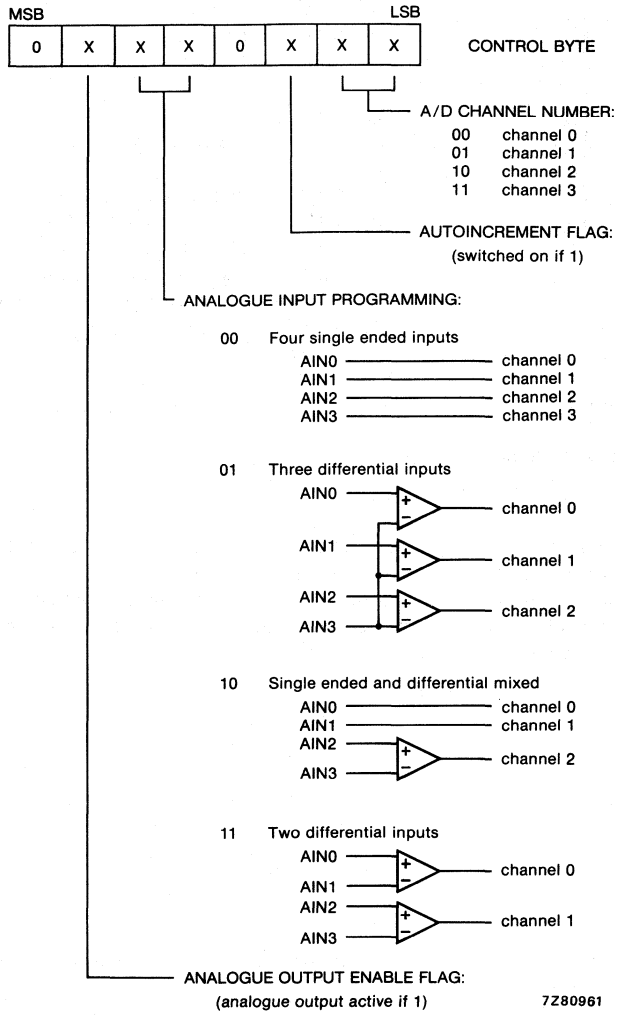


Fig. 4 Control byte.

D/A conversion

The third byte sent to a PCF8591 device is stored in the DAC data register and is converted to the corresponding analogue voltage using the on-chip D/A converter. This D/A converter consists of a resistor divider chain connected to the external reference voltage with 256 taps and selection switches. The tap-decoder switches one of these taps to the DAC output line (see Fig. 5).

The analogue output voltage is buffered by an auto-zeroed unity gain amplifier. This buffer amplifier may be switched on or off by setting the analogue output enable flag of the control register. In the active state the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analogue output AOUT is given by the formula shown in Fig. 6. The waveforms of a D/A conversion sequence are shown in Fig. 7.

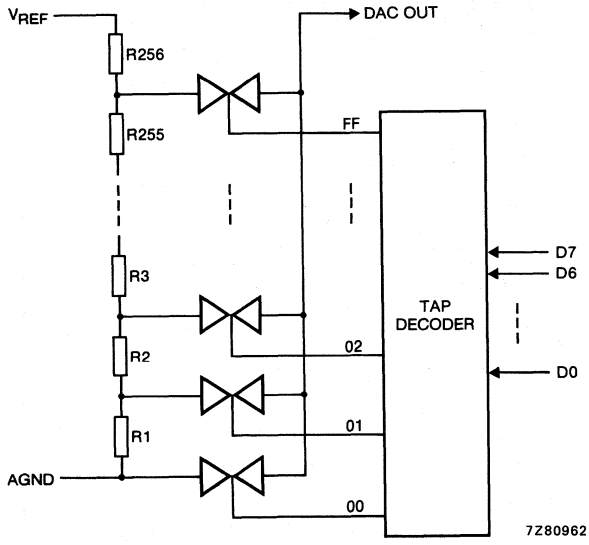


Fig. 5 DAC resistor divider chain.

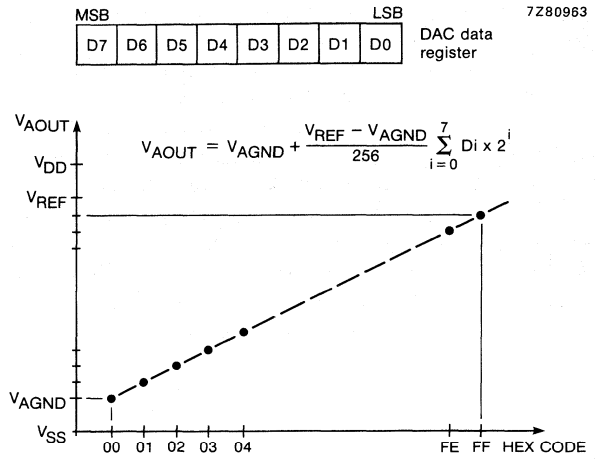


Fig. 6 DAC data and d.c. conversion characteristics.

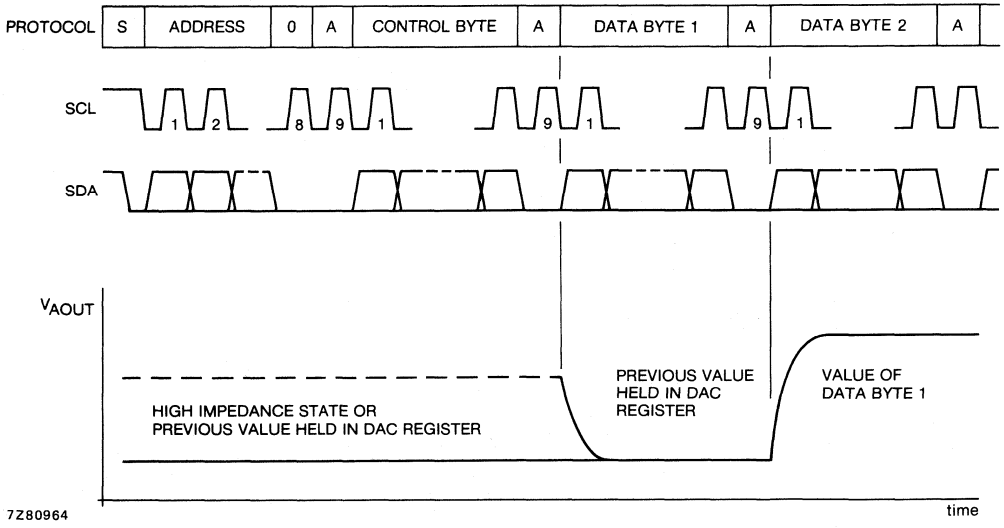


Fig. 7 D/A conversion sequence.

A/D conversion

The A/D converter makes use of the successive approximation conversion technique. The on-chip D/A converter and a high gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Fig. 8).

Once a conversion cycle is triggered an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Fig. 9). The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a power-on reset condition the first byte read is a hexadecimal 80. The protocol of an I^2C bus read cycle is shown in Fig. 10.

The maximum A/D conversion rate is given by the actual speed of the I^2C bus.

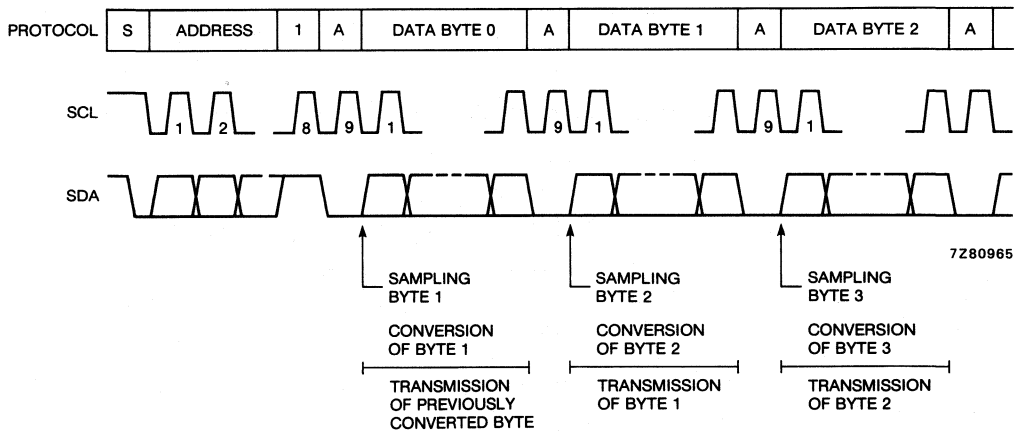


Fig. 8 A/D conversion sequence.

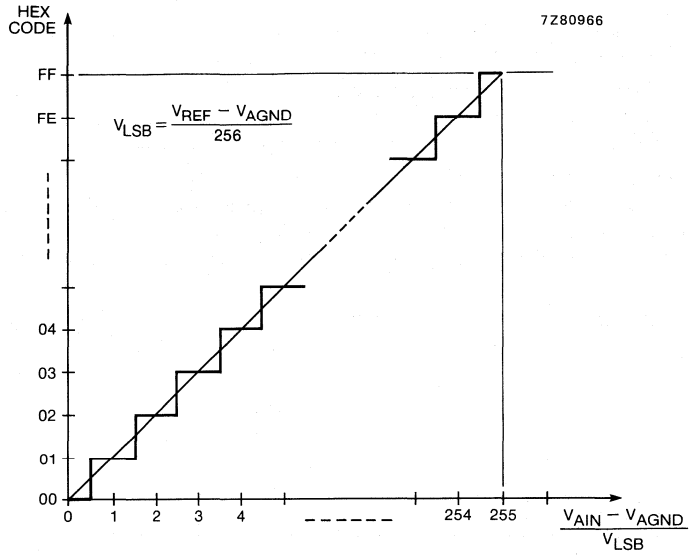


Fig. 9a A/D conversion characteristics of single-ended inputs.

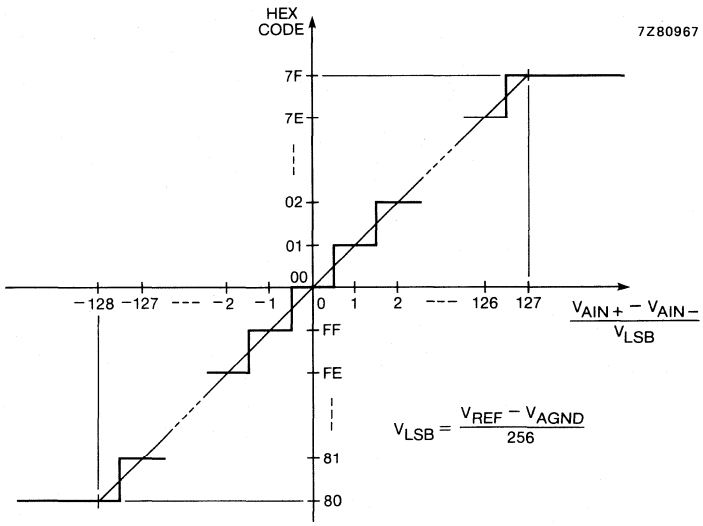


Fig. 9b A/D conversion characteristics of differential inputs.

Reference voltage

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins V_{REF} and AGND). The AGND pin has to be connected to the system analogue ground and may have a d.c. off-set with reference to V_{SS}.

A low frequency may be applied to the V_{REF} and AGND pins. This allows the use of the D/A converter as a one-quadrant multiplier; see Application Information and Fig. 6.

The A/D converter may also be used as a one or two quadrant analogue divider. The analogue input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin has to be connected to V_{SS}. At the OSC pin the oscillator frequency is available.

If the EXT pin is connected to V_{DD} the oscillator output OSC is switched to a high impedance state allowing the user to feed an external clock signal to OSC.

Bus protocol

After a start condition a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I^2C bus characteristics. In the write mode a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.

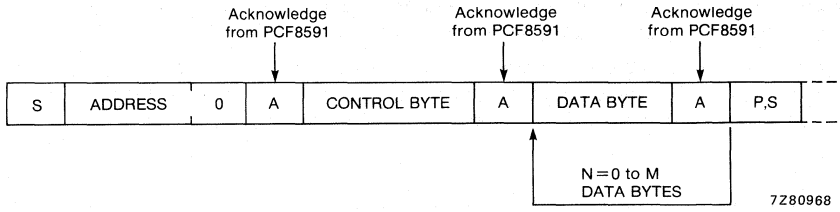


Fig. 10a Bus protocol for write mode, D/A conversion.

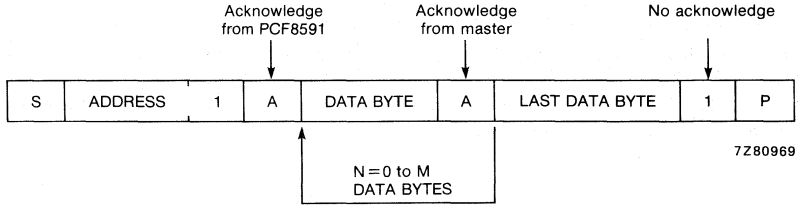


Fig. 10b Bus protocol for read mode, A/D conversion.

CHARACTERICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transfered during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

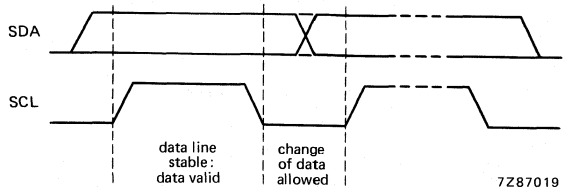


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

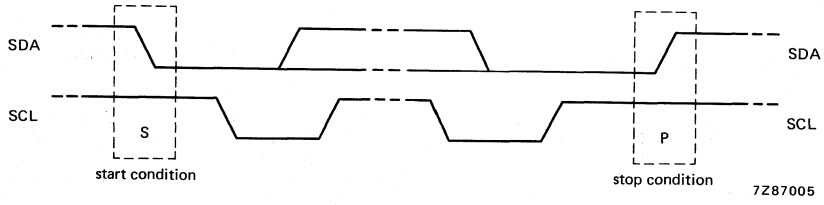


Fig. 12 Definition of start and stop condition.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

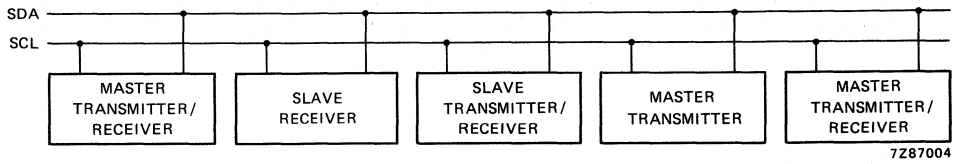


Fig. 13 System configuration.

Acknowledge.

The number of data bytes transfered between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

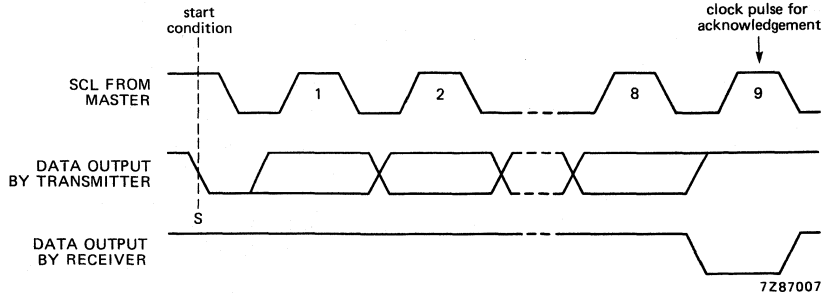


Fig. 14 Acknowledgement on the I^2C bus.

DEVELOPMENT DATA

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,0	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_R	–	–	1,0	μs
SCL and SDA fall time	t_F	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs

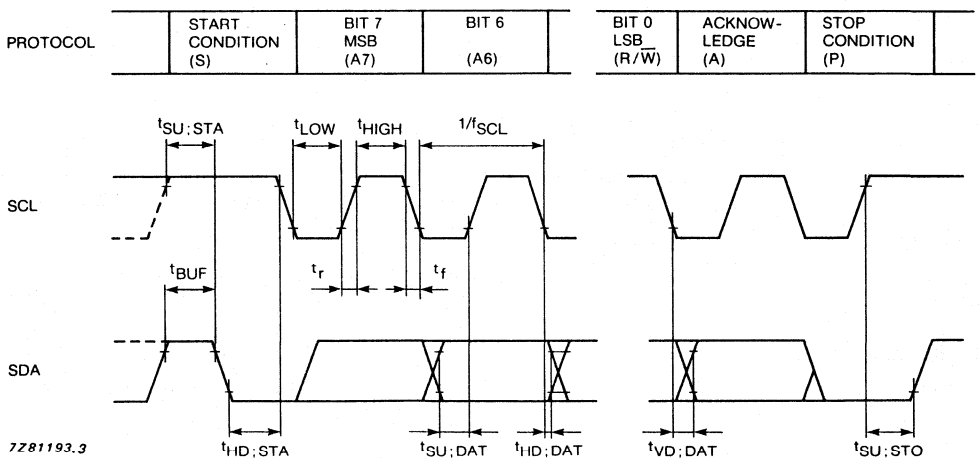


Fig. 15 I^2C bus timing diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to +8,0 V
Voltage on any pin	V_I		−0,5 to V_{DD} +0,5 V
Input current d.c.	I_I	max.	10 mA
Output current d.c.	I_O	max.	20 mA
V_{DD} or V_{SS} current	I_{DD}, I_{SS}	max.	50 mA
Power dissipation per package	P_{tot}	max.	300 mW
Power dissipation per output	P	max.	100 mW
Storage temperature range	T_{stg}		−65 to +150 °C
Operating ambient temperature range	T_{amb}		−40 to +85 °C

Note:

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	operating	V_{DD}	2,5	–	6,0	V
Supply current	standby V_I = V_{SS} or V_{DD}; no load	I_{DD0}	–	1	15	μA
Supply current	operating; AOUT off; f_{SCL} = 100 kHz	I_{DD1}	–	125	250	μA
Supply current	AOUT active; f_{SCL} = 100 kHz	I_{DD2}	–	0,45	1,0	mA
Power-on reset level	note 1	V_{POR}	0,8	–	2,0	V
Digital inputs/output	SCL, SDA, A0, A1, A2					
Input voltage	LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage	HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Leakage current A0–A2	V_I = V_{SS} to V_{DD}	$\lvert I_L \rvert$	–	–	250	nA
Input capacitance		C_I	–	–	5	pF
Leakage current SCL, SDA	V_I = V_{SS} to V_{DD}	$\lvert I_L \rvert$	–	–	1	μA
SDA output current	LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Reference voltage inputs						
Voltage range*	$V_{REF} > V_{AGND}$	V_{REF}	$V_{SS}+1,6$	–	V_{DD}	V
Voltage range*	$V_{REF} > V_{AGND}$	V_{AGND}	V_{SS}	–	$V_{DD}-0,8$	V
Input current	leakage	I_I	–	–	250	nA
Input resistance	V_{REF} to AGND	R_{REF}	–	100	–	kΩ
Oscillator	OSC, EXT					
Input current	leakage	I_I	–	–	250	nA
Oscillator frequency		f_{OSC}	0,75	–	1,25	MHz

D/A CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{load} = 10 kΩ; C_{load} = 100 pF; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue output						
Output voltage range	no resistive load	V_{OA}	V_{SS}	–	V_{DD}	V
Output voltage range	R_{load} = 10 kΩ	V_{OA}	V_{SS}	–	$0,9 \times V_{DD}$	V
Output current	leakage; AOUT disabled	I_{LO}	–	–	250	nA
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	50	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error	no resistive load	G_e	–	–	1	%
Settling time	to ½ LSB full scale step	t_{DAC}	–	–	90	μs
Conversion rate		f_{DAC}	–	–	11,1	kHz
Supply noise rejection	at f = 100 Hz; V_{DD} = 0,1 V_{PP}	SNRR	–	40	–	dB

* A further extension of the range is possible, if the following conditions are fulfilled:

$$\frac{V_{REF} + V_{AGND}}{2} \geqslant 0,8 \text{ V and } V_{DD} - \frac{V_{REF} + V_{AGND}}{2} \geqslant 0,4 \text{ V.}$$

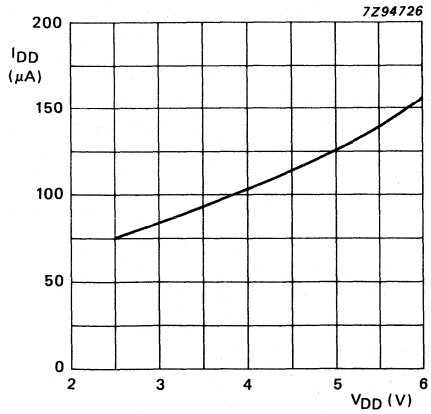
A/D CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{source} = 10 kΩ; T_{amb} = −40 °C to +85 °C unless otherwise specified

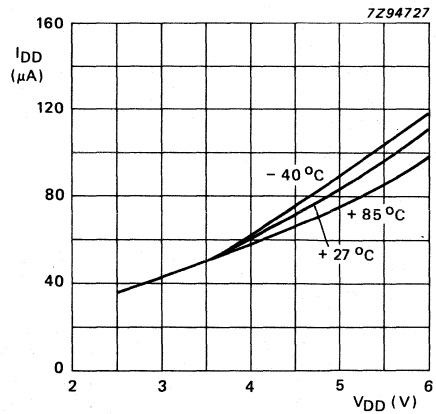
parameter	conditions	symbol	min.	typ.	max.	unit
Analogue inputs						
Input voltage range		V_{IA}	V_{SS}	–	V_{DD}	V
Input current	leakage	I_{IA}	–	–	100	nA
Input capacitance		C_{IA}	–	10	–	pF
Input capacitance	differential	C_{ID}	–	10	–	pF
Single-ended voltage	measuring range	V_{IS}	V_{AGND}	–	V_{REF}	V
Differential voltage	measuring range; $V_{FS} = V_{REF} - V_{AGND}$	V_{ID}	$\frac{-V_{FS}}{2}$	–	$\frac{+V_{FS}}{2}$	V
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	20	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error		G_e	–	–	1	%
Gain error	small-signal; ΔV_{IN} = 16 LSB	GS_e	–	–	5	%
Rejection ratio	common-mode	CMRR	–	60	–	dB
Supply noise rejection	at f = 100 Hz; $V_{DDN} = 0{,}1 \times V_{PP}$	SNRR	–	40	–	dB
Conversion time		t_{ADC}	–	–	90	μs
Sampling/conversion rate		f_{ADC}	–	–	11,1	kHz

Note

1. The power on reset circuit resets the I^2C bus logic when V_{DD} is less than V_{POR}.

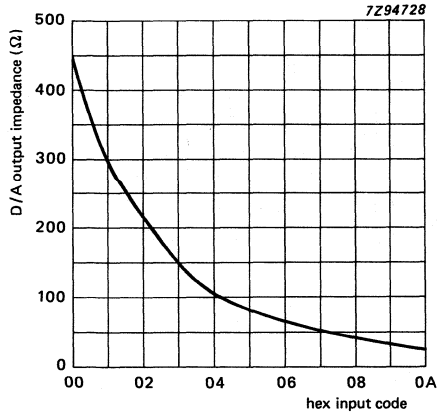


(a) internal oscillator; T_{amb} = + 27 °C.

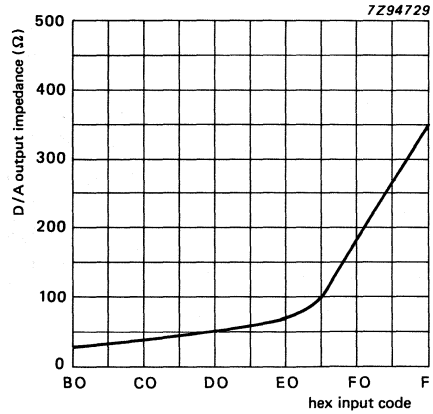


(b) external oscillator.

Fig. 16 Operating supply current against supply voltage (analogue output disabled).



(a) output impedance near negative power rail; T_{amb} = + 27 °C.



(b) output impedance near positive power rail; T_{amb} = + 27 °C.

Fig. 17 Output impedance of analogue output buffer (near power rails).

The x-axis represents the hex input-code equivalent of the output voltage.

APPLICATION INFORMATION

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analogue inputs may also be connected to AGND or V_{REF}.

In order to prevent excessive ground and supply noise and to minimize cross-talk of the digital to analogue signal paths the user has to design the printed-circuit board layout very carefully. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors ($> 10\ \mu F$) are recommended for power supply and reference voltage inputs.

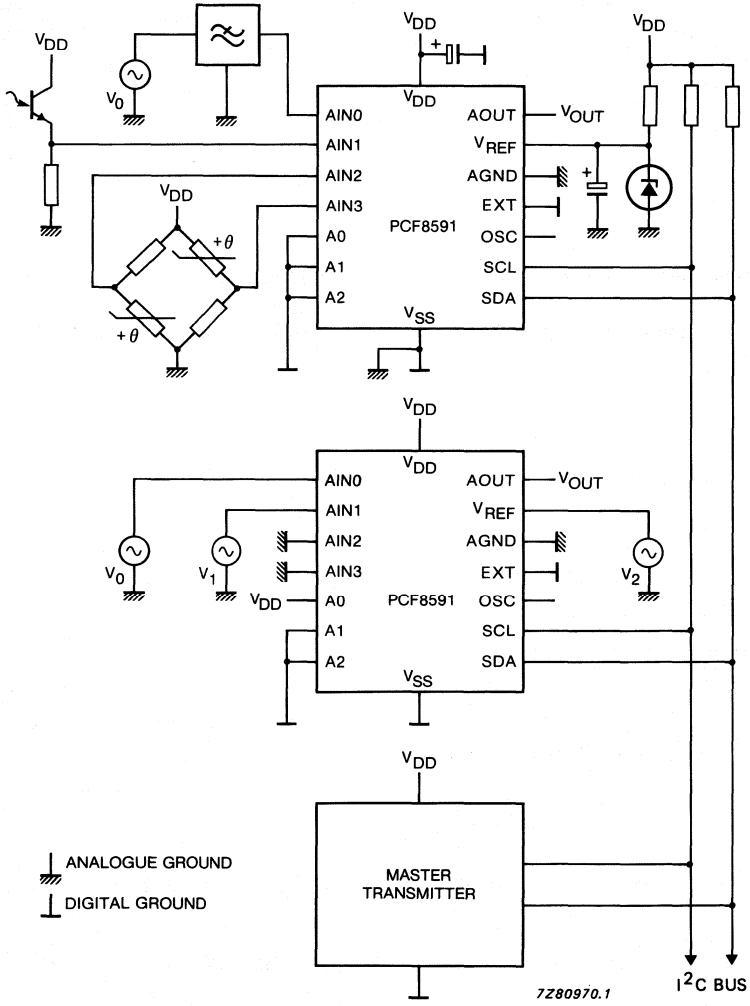


Fig. 18 Application diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Low power clock calendar PCF8593

FEATURES

- I²C-bus interface operating supply voltage: 2.5 to 6.0 V
- Clock operating supply voltage (T_{amb} = 0 to +70 °C): 1.0 to 6.0 V
- Data retention voltage: 1.0 to 6.0 V
- External $\overline{\text{RESET}}$ input pin
- Operating current (f_{scl} = 0 Hz, 32 kHz time base, V_{DD} = 2.0 V): typ. 1 μA
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I²C-bus)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Space-saving SO8 package
- Slave address:
  - READ A3H
  - WRITE A2H.

GENERAL DESCRIPTION

The PCF8593 is a CMOS Real-time clock/calendar optimized for low power consumption. Addresses and data are transferred serially via a two-line bidirectional bus (I²C-bus). The built-in word address register is incremented automatically after each written or read data byte. The built-in 32.768 kHz oscillator circuit and the first 8 registers are used for the clock/calendar and counter functions. The next 8 registers may be programmed as alarm registers or used as free RAM space.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage operating mode	I²C-bus active	2.5	6.0	V
		I²C-bus inactive	1.0	6.0	V
I_{DD}	supply current operating mode	f_{scl} = 100 kHz	–	200	μA
I_{DD}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 5 V	4.0	15.0	μA
		f_{scl} = 0 Hz; V_{DD} = 2 V	1.0	8.0	μA
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8593P	8	DIL	plastic	SOT97-1
PCF8593T	8	SO8	plastic	SOT96-1

BLOCK DIAGRAM

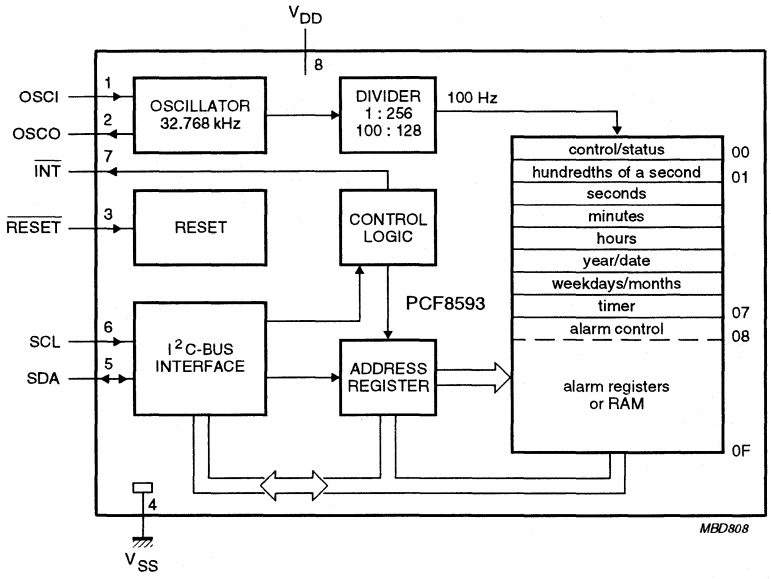


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
$\overline{RESET}$	3	reset input (active LOW)
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
$\overline{INT}$	7	open drain interrupt output (active LOW)
V_{DD}	8	positive supply

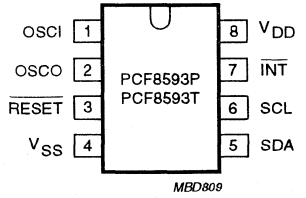


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The PCF8593 contains sixteen 8-bit registers with an 8-bit auto-incrementing address register, an on-chip 32.768 kHz oscillator circuit, a frequency divider and a serial two-line bidirectional I^2C-bus interface.

The first 8 registers (memory addresses 00 to 07) are designed as addressable 8-bit parallel registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F may be programmed as alarm registers or used as free RAM locations.

Counter function modes

When the control/status register is programmed, a 32.768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and week day are stored in a BCD format. The timer register stores up to 99 days. The event counter mode is used to count pulses applied to the oscillator input (OSCO left open-circuit). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore, faulty reading of the count during a carry condition is prevented.

When a counter is written, other counters are not affected.

Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a week day alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open-drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled). The flags remain set until directly reset by a write operation.

When a timer function without any function is programmed the remaining alarm registers (addresses 09 to 0F) may be used as free RAM space.

Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I^2C-bus. All functions and options are controlled by the contents of the control/status register (see Fig.3).

Counter registers

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig.5.

The year and date are packed into memory location 05 (see Fig 6). The weekdays and months are packed into memory location 06 (see Fig.7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

In the different modes the counter registers are programmed and arranged as shown in Fig.4. Counter cycles are listed in Table 1.

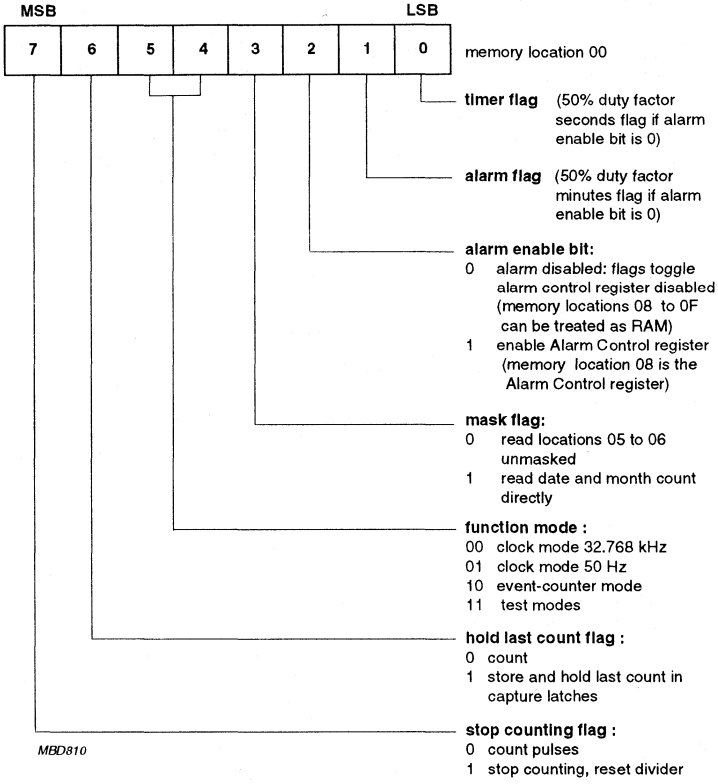


Fig.3 Control/status register.

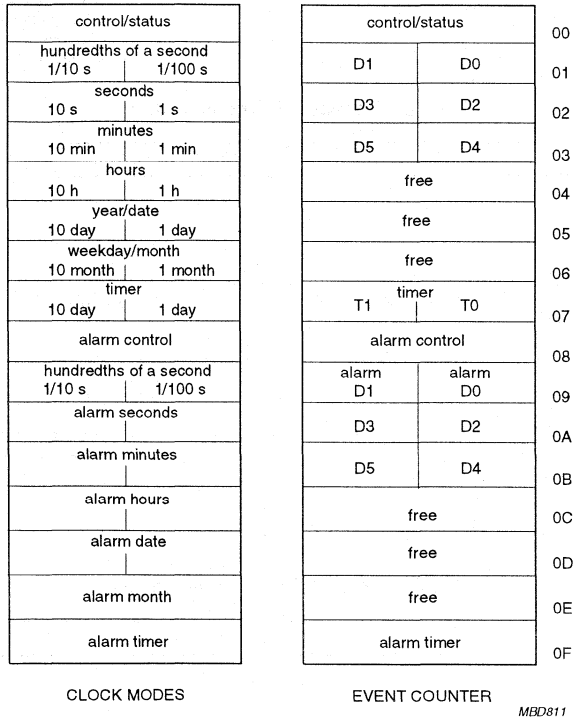


Fig.4 Register arrangement.

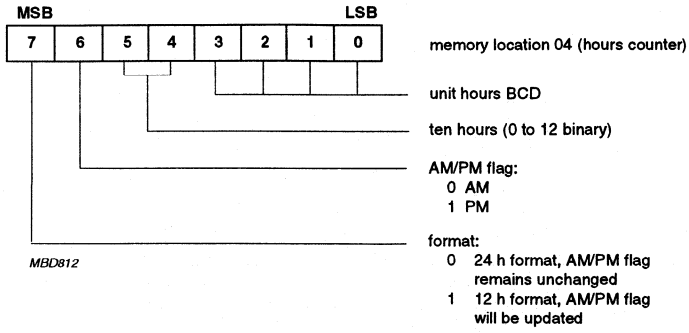


Fig.5 Format of the hours counter.

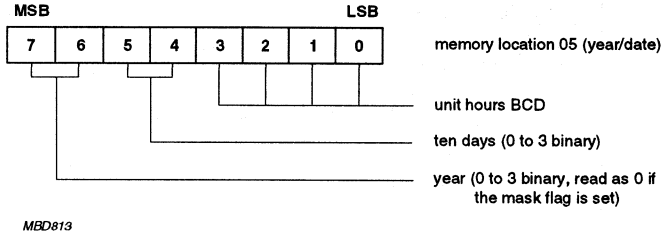


Fig.6 Format of the year/date counter.

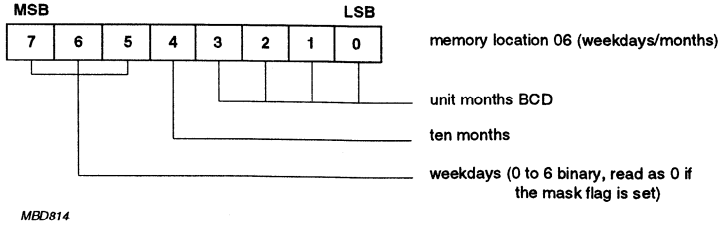


Fig.7 Format of the weekdays/months counter.

Table 1 Cycle length of the time counters, clock modes.

UNIT	COUNTING CYCLE	CARRY TO NEXT UNIT	CONTENTS OF THE MONTH COUNTER
Hundredths of a second	00 to 99	99 to 00	–
Seconds	00 to 59	59 to 00	–
Minutes	00 to 59	59 to 00	–
Hours (24 h)	00 to 23	23 to 00	–
Hours (12 h)	12 AM	–	–
	01 AM to 11 AM	–	–
	12 PM	–	–
	01 PM to 11 PM	11 PM to 12 AM	–
Date	01 to 31	31 to 01	1, 3, 5, 7, 8, 10 and 12
	01 to 30	30 to 01	4, 6, 9 and 11
	01 to 29	29 to 01	2, year = 0
	01 to 28	28 to 01	2, year = 1, 2 and 3
Months	01 to 12	12 to 01	–
Year	0 to 3	–	–
Weekdays	0 to 6	6 to 0	–
Timer	00 to 99	no carry	–

Alarm control register

When the alarm enable bit of the control/status register is set (address 00, bit 2) the alarm control register (address 08) is activated. All alarm, timer, and interrupt output functions are controlled by the contents of the alarm control register (see Fig.8).

Alarm registers

All alarm registers are allocated with a constant address offset of hexadecimal 08 to the corresponding counter registers (see Fig.4; Register arrangement).

An alarm signal is generated when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig.9).

Remark: in the 12 h mode, bits 6 and 7 of the alarm hours register must be the same as the hours counter.

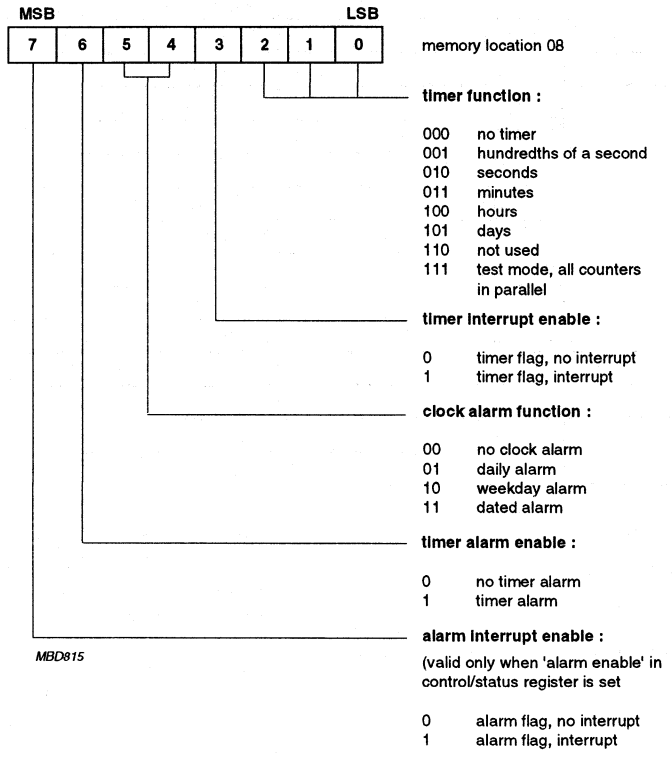


Fig.8 Alarm control register; clock mode.

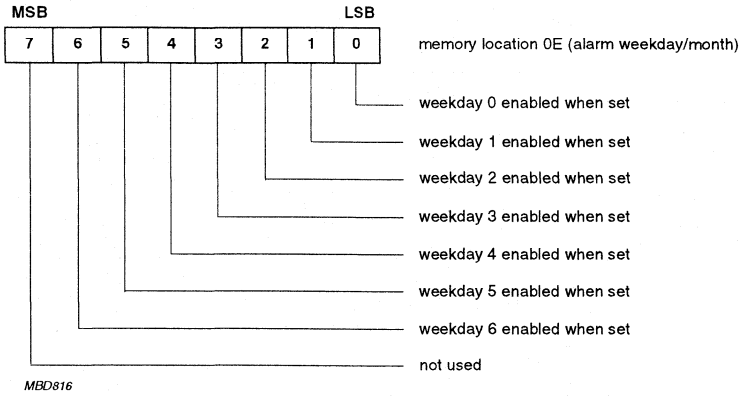


Fig.9 Selection of alarm weekdays.

Timer

The timer (location 07) is enabled by setting the control/status register = XX0X X1XX. The timer counts up from 0 (or a programmed value) to 99. On overflow, the timer resets to 0. The timer flag (LSB of control/status register) is set on overflow of the timer. This flag must be reset by software. The inverted value of this flag can be transferred to the external interrupt by setting bit 3 of the alarm control register.

Additionally, a timer alarm can be programmed by setting the timer alarm enable (bit 6 of the alarm control register). When the value of the timer equals a pre-programmed value in the alarm timer register (location 0F), the alarm flag is set (bit 1 of the control/status register). The inverted value of the alarm flag can be transferred to the external interrupt by enabling the alarm interrupt (bit 6 of the alarm control register).

Resolution of the timer is programmed via the 3 LSBs of the alarm control register (see Fig.11; Alarm and timer Interrupt logic diagram).

Event counter mode

Event counter mode is selected by bits 4 and 5 which are logic 1, 0 in the control/status register. The event counter mode is used to count pulses externally applied to the oscillator input (OSCO left open-circuit). The event counter stores up to 6 digits of data, which are stored as 6 hexadecimal values located in locations 1, 2, and 3. Thus, up to 1 million events may be recorded.

An event counter alarm occurs when the event counter registers match the value programmed in locations 9, A, and B, and the event alarm is enabled (bits 4 and 5 which are logic 0, 1 in the alarm control register). In this event, the alarm flag (bit 1 of the control/status register) is set. The inverted value of this flag can be transferred to the interrupt pin (pin 7) by setting the alarm interrupt enable in the alarm control register. In this mode, the timer (location 07) increments once for every one, one-hundred, ten thousand, or 1 million events, depending on the value programmed in bits 0,1 and 2 of the alarm control register. In all other events, the timer functions are as in the clock mode.

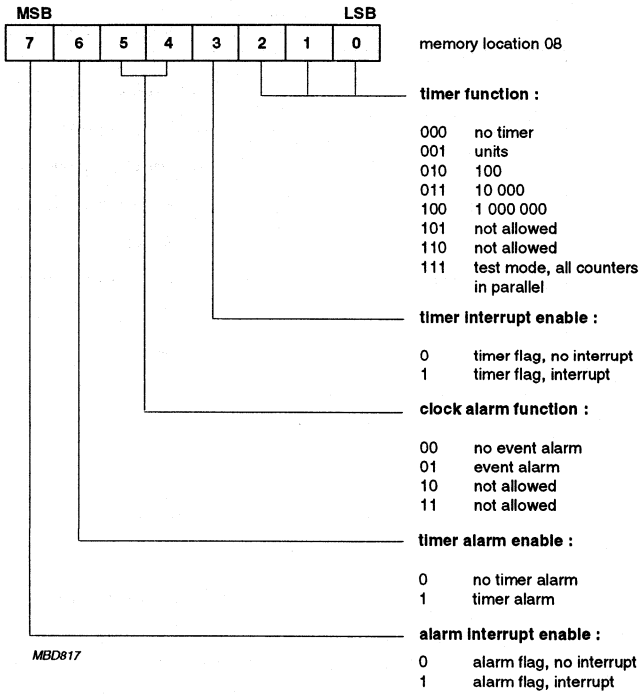
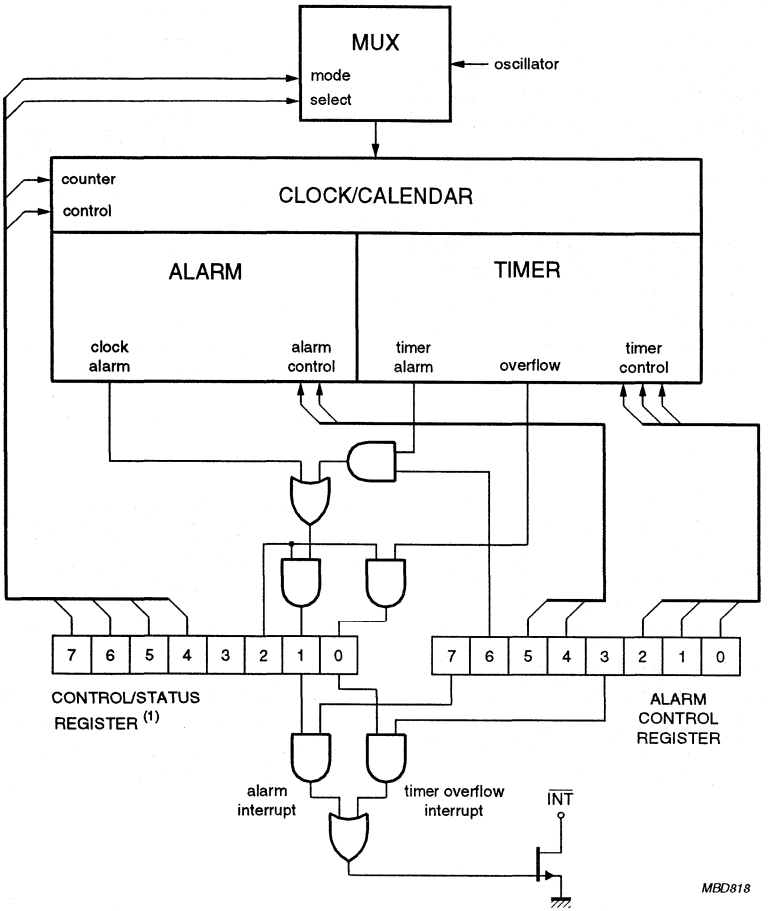


Fig.10 Alarm control register; event-counter mode.

Interrupt output

The conditions for activating the open-drain n-channel interrupt output $\overline{INT}$ (active LOW) are determined by appropriate programming of the alarm control register. These conditions are clock alarm, timer alarm, timer overflow, and event counter alarm. An interrupt occurs when the alarm flag or the timer flag is set, and the corresponding interrupt is enabled. In all events, the interrupt is cleared only by software resetting of the flag which initiated the interrupt.

In the clock mode, if the alarm enable is not activated (alarm enable bit of control/status register is logic 0), the interrupt output toggles at 1 Hz with a 50% duty cycle (may be used for calibration). The OFF voltage of the interrupt output may exceed the supply voltage, up to a maximum of 6.0 V. A logic diagram of the interrupt output is shown in Fig.11.



(1) If the alarm enable bit of the control/status register is reset (logic 0), a 1 Hz signal can be observed on the interrupt pin $\overline{INT}$.

Fig.11 Alarm and timer interrupt logic diagram.

Oscillator and divider

A 32.768 kHz quartz crystal has to be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator (see Chapter "Application information" ; Section "Quartz frequency adjustment"). A 100 Hz clock signal is derived from the quartz oscillator for the clock counters.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high-impedance state. This allows the user to feed the 50 Hz reference frequency or an external high-speed event signal into the input OSCI.

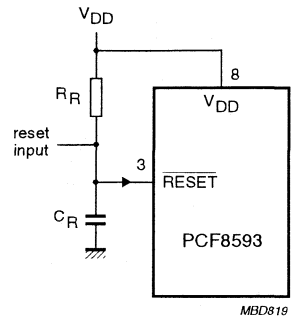
DESIGNING

When designing the printed-circuit board layout, keep the oscillator components as close to the IC package as possible, and keep all other signal lines as far away as possible. In applications involving tight packing of components, shielding of the oscillator may be necessary. AC coupling of extraneous signals can introduce oscillator inaccuracy.

Initialization (see Fig.12)

Note that immediately following power-on, all internal registers are undefined and, following a $\overline{\text{RESET}}$ pulse on pin 3, must be defined via software. Attention should be paid to the possibility that the device may be initially in event-counter mode, in which event the oscillator will not operate. Over-ride can be achieved via software.

Reset is accomplished by applying an external $\overline{\text{RESET}}$ pulse (active LOW) at pin 3. When reset occurs the I^2C-bus interface is reset. The control/status register and all clock counters are not affected by $\overline{\text{RESET}}$. $\overline{\text{RESET}}$ must return HIGH during device operation.



To avoid overload of the internal diode by falling V_{DD}, an external diode should be added in parallel to R_R if $C_R \geq 0.2\ \mu F$. Note that RC must be evaluated with the actual V_{DD} of the application, as their value will be V_{DD} rise-time dependent.

Fig.12 RC reset.

An RC combination can also be utilized to provide a power-on $\overline{\text{RESET}}$ signal at pin 3. In this event, the values of the RC must fulfil the following relationship to guarantee power-on reset (see Fig.12).

$\overline{\text{RESET}}$ input must be $\leq 0.3V_{DD}$ when V_{DD} reaches V_{DDmin} (or higher).

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states may lead to a temporary clock malfunction.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

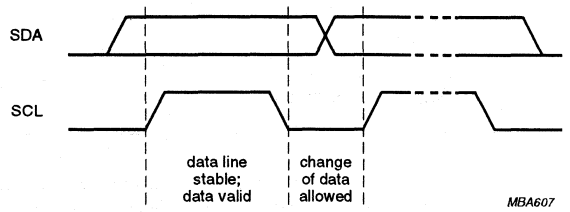


Fig.13 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

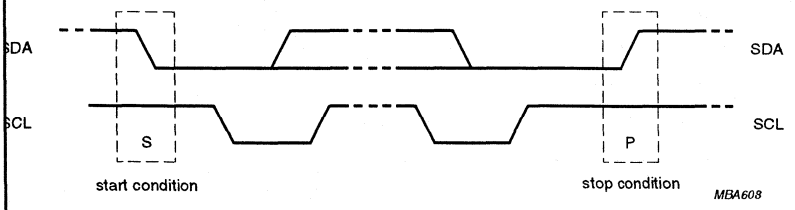


Fig.14 Definition of start and stop conditions.

System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

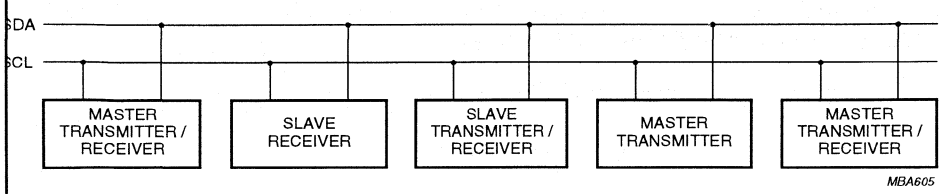


Fig.15 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

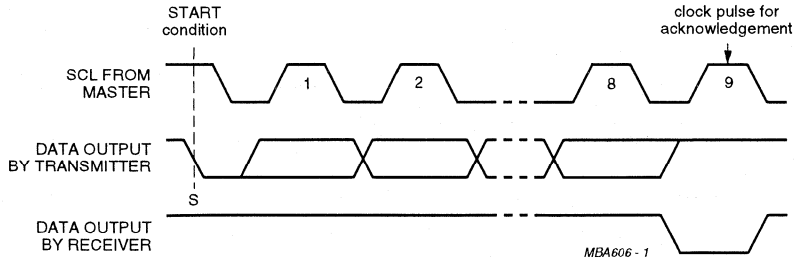


Fig.16 Acknowledgement on the I^2C-bus.

I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF8593 READ and WRITE cycles is shown in Figs 17, 18 and 19.

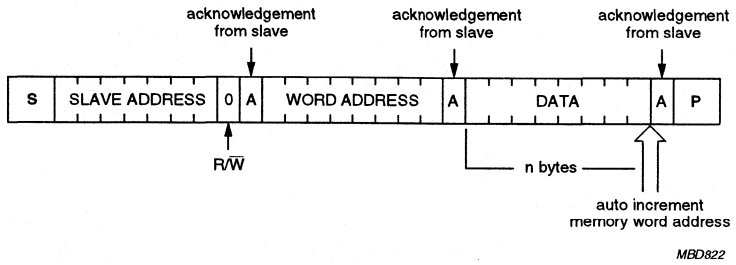


Fig.17 Master transmits to slave receiver (WRITE) mode.

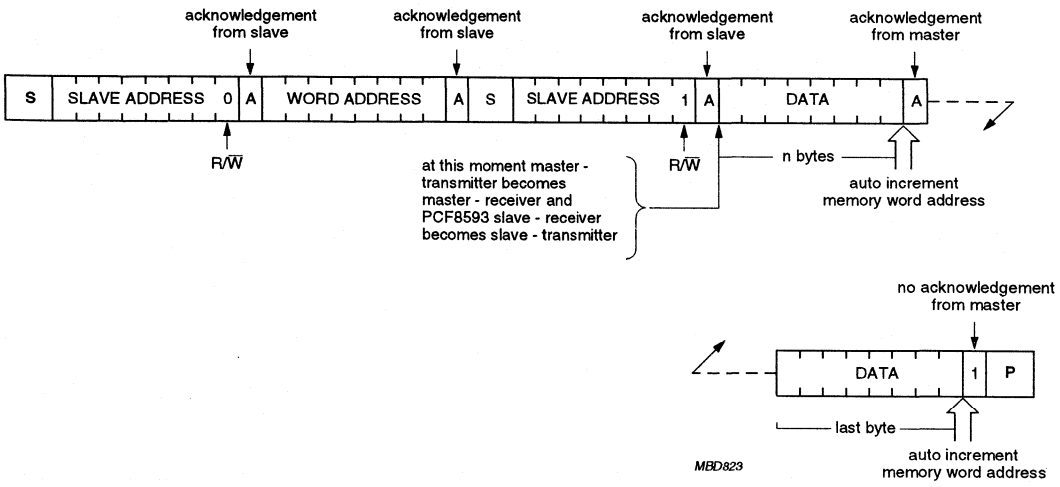


Fig.18 Master reads after setting word address (write word address; READ data).

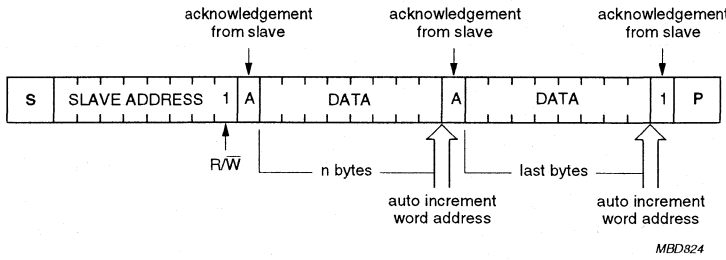


Fig.19 Master reads slave immediately after first byte (READ mode).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pin 8)	−0.8	+7.0	V
I_{DD}	supply current (pin 8)	–	50	mA
I_{SS}	supply current (pin 4)	–	50	mA
V_I	input voltage	−0.8	V_{DD} + 0.8	V
I_I	DC input current	–	10	mA
I_O	DC output current	–	10	mA
P_{tot}	total power dissipation per package	–	300	mW
P_O	power dissipation per output	–	50	mW
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

DC CHARACTERISTICS

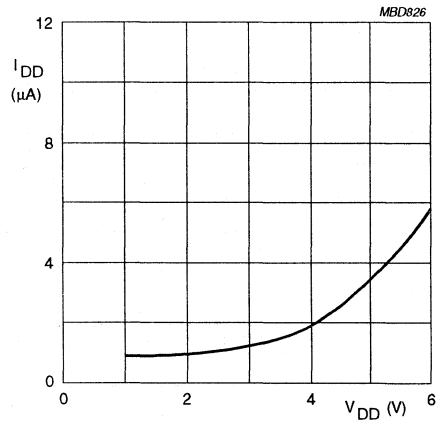
V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; f_{osc} = 32 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
Supply						
V_{DD}	supply voltage operating mode	I²C-bus active	2.5	–	6.0	V
		I²C-bus inactive	1.0	–	6.0	V
V_{DDosc}	quartz oscillator supply voltage	T_{amb} = 0 to 70 °C; note 2	1.0	–	6.0	V
		T_{amb} = −40 to 85 °C; note 2	1.2	–	6.0	V
I_{DD}	supply current operating mode	f_{scl} = 100 kHz; clock mode; note 3	–	–	200	µA
I_{DD}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 2 V; inputs at V_{DD} or V_{SS}	–	1.0	8.0	µA
		f_{scl} = 0 Hz; V_{DD} = 5 V; inputs at V_{DD} or V_{SS}	–	4.0	15	µA
SDA, SCL, $\overline{INT}$ and RESET						
V_{IL}	LOW level input voltage		0	–	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD}	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	–	–	mA
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}	−1	–	+1	µA
C_I	input capacitance	note 4	–	–	7	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
OSCI and $\overline{\text{RESET}}$						
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−250	–	+250	nA
$\overline{\text{INT}}$						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	1	–	–	mA
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA
SCL						
C_I	input capacitance	note 4	–	–	7	pF
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA

Notes

1. Typical values measured at 25 °C.
2. When powering up the device, V_{DD} must exceed the specified minimum value by 300 mV to guarantee correct start-up of the oscillator.
3. Event counter mode; supply current dependent upon input frequency.
4. Tested on sample basis.



f_{SCL} = 32 kHz; T_{amb} = 25 °C.

Fig.20 Typical supply current in clock mode as a function of supply voltage.

AC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
C_{osc}	integrated oscillator capacitance		20	25	30	pF
Δf_{osc}	oscillator stability	for ΔV_{DD} = 100 mV; T_{amb} = 25 °C; V_{DD} = 1.5 V	–	2×10^{-7}	–	
f_i	input frequency	note 1	–	–	1	MHz
Quartz crystal parameters (f = 32.768 kHz)						
R_s	series resistance		–	–	40	kΩ
C_L	parallel load capacitance		–	10	–	pF
C_T	trimmer capacitance		5	–	25	pF
I²C-bus timing (see Fig.21; notes 2 and 3)						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SP}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	start condition set-up time		4.7	–	–	µs
$t_{HD;STA}$	start condition hold time		4.0	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1.0	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid		–	–	3.4	µs
$t_{SU;STO}$	stop condition set-up time		4.0	–	–	µs

Notes

1. Event counter mode only.
2. All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
3. A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

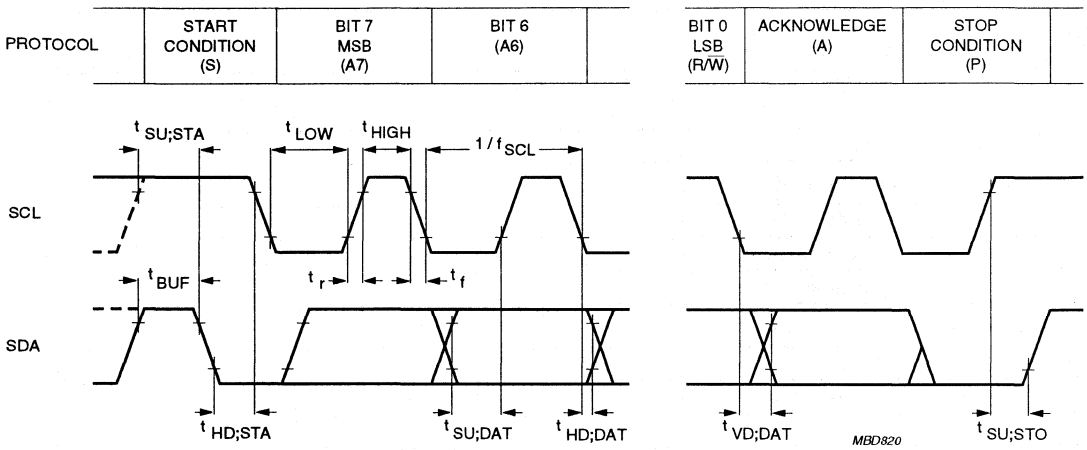


Fig.21 I^2C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

APPLICATION INFORMATION

Quartz frequency adjustment

METHOD 1: FIXED OSCI CAPACITOR

By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 1 Hz signal which can be programmed to occur at the interrupt output (pin 7). The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average $\pm 5 \times 10^{-6}$). Average deviations of ±5 minutes per year can be achieved.

METHOD 2: OSCI TRIMMER

Using the alarm function (via the I²C-bus) a signal faster than 1 Hz can be generated at the interrupt output for fast setting of a trimmer.

Procedure:

- Power-on
- Apply $\overline{\text{RESET}}$
- Initialization (alarm functions).

Routine:

- Set clock to time T and set alarm to time T + ΔT
- At time T + ΔT (interrupt) repeat routine.

METHOD 3: DIRECT OUTPUT

Direct measurement of oscillator output (accounting for test probe capacitance).

Slave address

The PCF8593 has an internally fixed I²C-bus slave address.

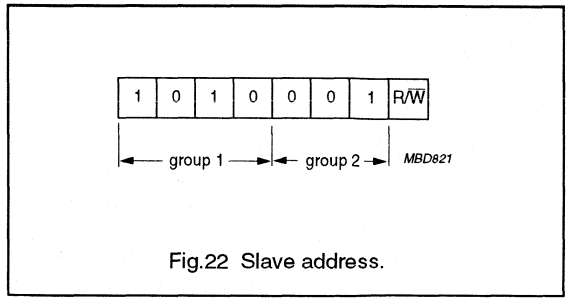
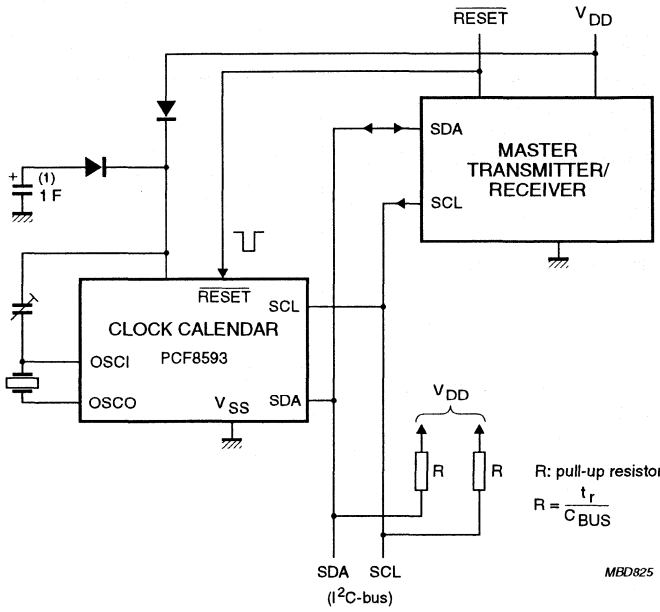


Fig.22 Slave address.



(1) Example Philips DLC 196 Double-Layer Capacitor family.

Fig.23 Application diagram.

256 x 8-bit CMOS EEPROMS with I²C-bus interface

PCX8582X-2 Family

FEATURES

- Low power CMOS
  - maximum active current 2.0 mA
  - maximum standby current 10 μA (at 6.0 V), typical 4 μA
- Non-volatile storage of 2-Kbits organized as 256 × 8-bits
- Single supply with full operation down to 2.5 V
- On-chip voltage multiplier
- Serial input/output I²C-bus
- Write operations
  - byte write mode
  - 8-byte page write mode (minimizes total write time per byte)
- Read operations
  - sequential read
  - random read
- Internal timer for writing (no external components)
- Power-on reset
- High reliability by using a redundant storage code
- Endurance
  - >500 k E/W-cycles at T_{amb} = 22 °C
- 40 years non-volatile data retention time (typ.)
- Pin and address compatible to
  - PCX8570, PCF8571, PCF8572 and PCF8581
  - PCX8494X-2, PCX8598X-2 -Family.

DESCRIPTION

The PCX8582X-2 is a 2-Kbit (256 × 8-bit) floating gate electrically erasable programmable read only memory (EEPROM). By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip, using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to eight PCX8582X-2 devices may be connected to the I²C-bus. Chip select is accomplished by three address inputs (A0, A1, A2).

Timing of the ERASE/WRITE cycle is carried out internally, thus no external components are required. Pin 7 (PTC) must be connected to either V_{DD} or left open-circuit.

There is an option of using an external clock for timing the length of an ERASE/WRITE cycle.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.5	6.0	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	–	60	μA
		V_{DD} = 6 V	–	200	μA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	–	0.6	mA
		V_{DD} = 6 V	–	2.0	mA
I_{DDSB}	supply current STANDBY	V_{DD} = 3 V	–	3.5	μA
		V_{DD} = 6 V	–	10	μA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE (°C)		SUPPLY (V)	
	NAME	DESCRIPTION	VERSION	MIN.	MAX.	MIN.	MAX.
PCF8582C-2P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1	−40	+85	2.5	6.0
PCD8582D-2P				−25	+70	3.0	6.0
PCF8582E-2P				−40	+85	4.5	5.5
PCA8582F-2P				−40	+125	4.5	5.5
PCF8582C-2T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1	−40	+85	2.5	6.0
PCD8582D-2T				−25	+70	3.0	6.0
PCF8582E-2T				−40	+85	4.5	5.5
PCA8582F-2T				−40	+125	4.5	5.5

DEVICE SELECTION

Table 1 Device selection code

SELECTION	DEVICE CODE				CHIP ENABLE			R/$\overline{W}$
Bit	b71	b6	b5	b4	b3	b2	b1	b0
Device	1	0	1	0	A2	A1	A0	R/$\overline{W}$

Note

1. The MSB b7 is sent first.

Table 2 Endurance and data retention guarantees

DEVICE	ENDURANCE E/W CYCLES	DATA RETENTION YEARS
PCF8582C-2; PCA8582F-2	500000[1]	40

Note

1. At the time of publication of this data sheet the statistical history was not yet sufficient to guarantee 1000000000 E/W cycle performance for these types.

BLOCK DIAGRAM

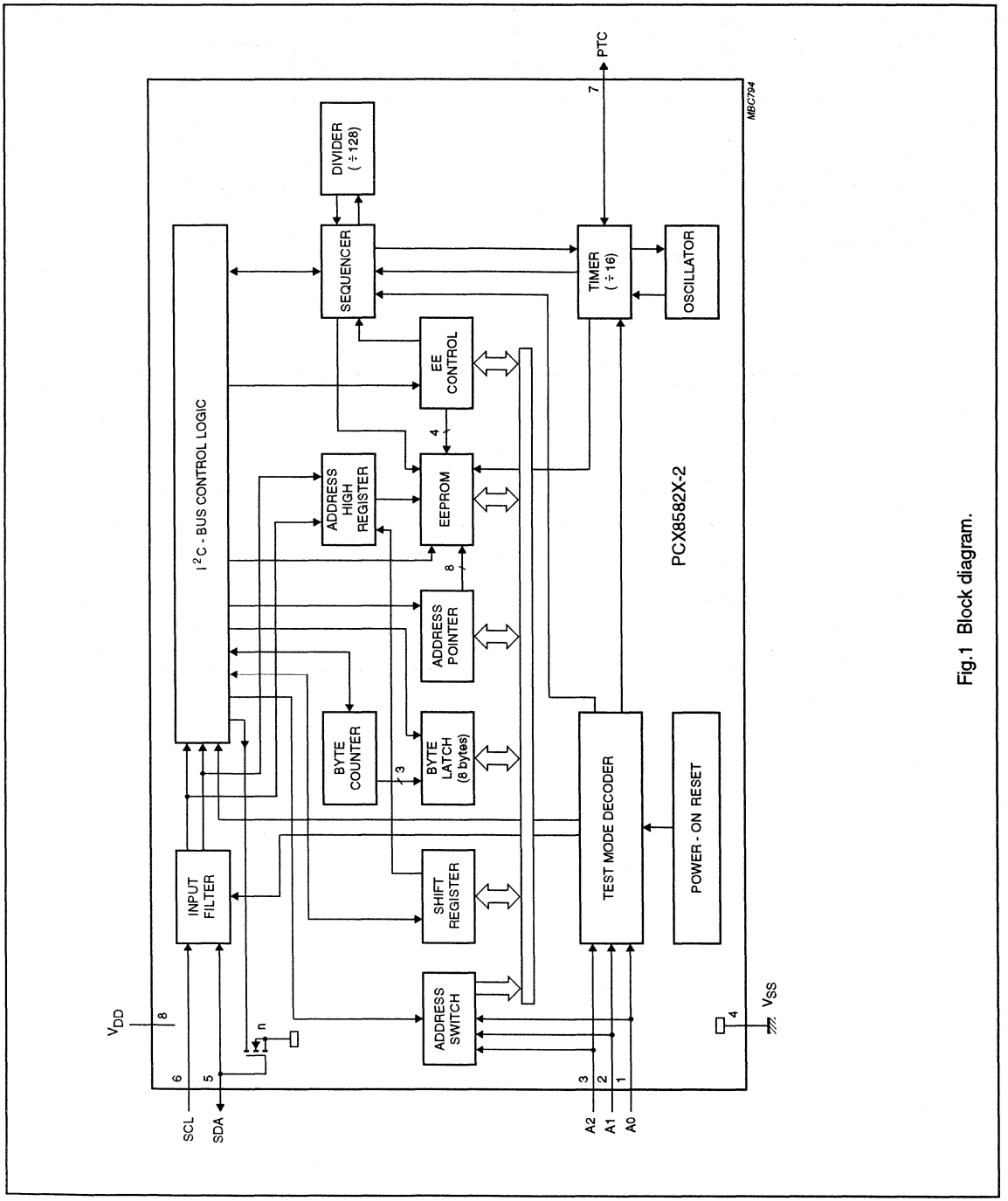


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	address input 0
A1	2	address input 1
A2	3	address input 2
V_{SS}	4	negative supply voltage
SDA	5	serial data input/output (I²C-bus)
SCL	6	serial clock input (I²C-bus)
PTC	7	programming time control output
V_{DD}	8	positive supply voltage

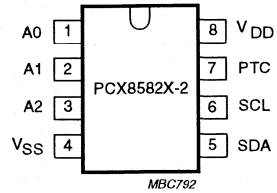


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.3	+7.0	V
V_I	voltage on any input pin	$\|Z_I\| > 500\ \Omega$	$V_{SS} - 0.8$	$V_{DD} + 0.8$	V
I_I	current on any input pin		−	1	mA
I_O	output current		−	10	mA
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature				
	PCF8582C-2; PCF8582E-2		−40	+85	°C
	PCD8582D-2		−25	+70	°C
	PCA8582F-2		−40	+125	°C

CHARACTERISTICS

PCF8582C-2: V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.
PCD8582D-2: V_{DD} = 3.0 to 6.0 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; unless otherwise specified.
PCF8582E-2: V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.
PCA8582F-2: V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +125 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supplies					
V_{DD}	supply voltage				
	PCF8582C-2		2.5	6.0	V
	PCD8582D-2		3.0	6.0	V
	PCF8582E-2; PCA8582F-2		4.5	5.5	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz			
	PCF8582C-2; PCD8582D-2	V_{DD} = 3.0 V	–	60	µA
		V_{DD} = 6.0 V	–	200	µA
	PCF8582E-2; PCA8582F-2	V_{DD} = 5.5 V	–	200	µA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz			
	PCF8582C-2; PCD8582D-2	V_{DD} = 3.0 V	–	0.6	mA
		V_{DD} = 6.0 V	–	2.0	mA
	PCF8582E-2; PCA8582F-2	V_{DD} = 5.5 V	–	2.0	mA
I_{DDSB}	supply current STANDBY	f_{SCL} = 100 kHz			
	PCF8582C-2; PCD8582D-2	V_{DD} = 3.0 V	–	3.5	µA
		V_{DD} = 6.0 V	–	10	µA
	PCF8582E-2; PCA8582F-2	V_{DD} = 5.5 V	–	10	µA
PTC input (pin 7)					
V_{IL}	LOW level input voltage		−0.8	$0.1V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.9V_{DD}$	V_{DD} + 0.8	V
SCL input (pin 6)					
V_{IL}	LOW level input voltage		−0.8	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	V_{DD} + 0.8	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	–	±1	µA
f_{SCL}	clock input frequency		0	100	kHz
C_I	input capacitance	$V_I = V_{SS}$	–	7	pF
SDA input/output (pin 5)					
V_{IL}	LOW level input voltage		−0.8	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	V_{DD} + 0.8	V
V_{OL}	LOW level output voltage	I_{OL} = 3 mA; $V_{DD(min)}$	–	0.4	V
I_{LO}	output leakage current	$V_{OH} = V_{DD}$	–	1	µA
C_I	input capacitance	$V_I = V_{SS}$	–	7	pF
Data retention time					
t_S	data retention time	T_{amb} = 55 °C	10	–	years

WRITE CYCLE LIMITS

Selection of the chip address is achieved by connecting the A0, A1 and A2 inputs to either V_{SS} or V_{DD}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ERASE/WRITE cycle timing						
$t_{E/W}$	ERASE/WRITE cycle time					
	internal oscillator		–	7	–	ms
	external clock		4	–	10	ms
Endurance						
$N_{E/W}$	ERASE/WRITE cycle per byte					
	PCF8582C-2	T_{amb} = 85 °C; $t_{E/W}$ = 4 to 10 ms	100000	–	–	cycles
		T_{amb} = 22 °C; $t_{E/W}$ = 5 ms	500000	–	–	cycles
	PCD8582D-2	T_{amb} = –25 to +70 °C; $t_{E/W}$ = 4 to 10 ms	10000	–	–	cycles
		T_{amb} = –25 to +40 °C; $t_{E/W}$ = 5 ms	100000	–	–	cycles
	PCF8582E-2	T_{amb} = –40 to +85 °C; $t_{E/W}$ = 4 to 10 ms	10000	–	–	cycles
		T_{amb} = 22 °C; $t_{E/W}$ = 5 ms	100000	–	–	cycles
	PCA8582F-2	T_{amb} = 125 °C; $t_{E/W}$ = 4 to 10 ms	50000	–	–	cycles
		T_{amb} = 85 °C; $t_{E/W}$ = 4 to 10 ms	100000	–	–	cycles
		T_{amb} = 22 °C; $t_{E/W}$ = 5 ms	500000	–	–	cycles

I²C-BUS PROTOCOL

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The serial bus consists of two bidirectional lines: one for data signals (SDA), and one for clock signals (SCL).

Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

- **Bus not busy:** both data and clock lines remain HIGH.
- **Start data transfer:** a change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH, defines the start condition.
- **Stop data transfer:** a change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH, defines the stop condition.
- **Data valid:** the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to seven bytes in the ERASE/WRITE mode and eight bytes in the PAGE ERASE/WRITE mode. Data transfer is unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low-speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined.

The PCX8582X-2 operates in both modes.

By definition a device that sends a signal is called a 'transmitter', and the device which receives the signal is called a 'receive'. The device which controls the signal is called the 'master'. The devices that are controlled by the master are called 'slaves'.

Each byte is followed by one acknowledge bit. This acknowledge bit is a HIGH level, put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse. The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.

The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.

Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

DEVICE ADDRESSING

Following a start condition the bus master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Fig.3). For the PCX8582X-2 this is fixed as 1010.

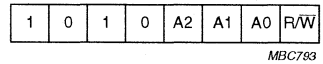


Fig.3 Slave address.

The next three significant bits address a particular device. A system could have up to eight PCX8582X-2 devices on the bus. The eight addresses are defined by the state of the A0, A1 and A2 inputs.

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read operation is selected.

Address bits must be connected to either V_{DD} or V_{SS}.

WRITE OPERATIONS

Byte/word write

For a write operation the PCX8582X-2 requires a second address field. This address field is a word address providing access to the 256 words of memory. Upon receipt of the word address the PCX8582X-2 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. Word address is automatically incremented. The master can now terminate the transfer by generating a stop condition or transmit up to six more bytes of data and then terminate by generating a stop condition.

After this stop condition the ERASE/WRITE cycle starts and the bus is free for another transmission. Its duration is 7 ms (typ.) per byte.

During the ERASE/WRITE cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

PAGE WRITE

The PCX8582X-2 is capable of an eight-byte page write operation. It is initiated in the same manner as the byte write operation. The master can transmit eight data bytes within one transmission. After receipt of each byte the PCX8582X-2 will respond with an acknowledge. The typical ERASE/WRITE time in this mode is 9×7 ms = 63 ms.

After the receipt of each data byte the three low order bits of the word address are internally incremented. The high order five bits of the address remain unchanged. If the master transmits more than eight bytes prior to generating the stop condition, no acknowledge will be given on the ninth (and following) data bytes and the whole transmission will be ignored. As in the byte write operation, all inputs are disabled until completion of the internal write cycles.

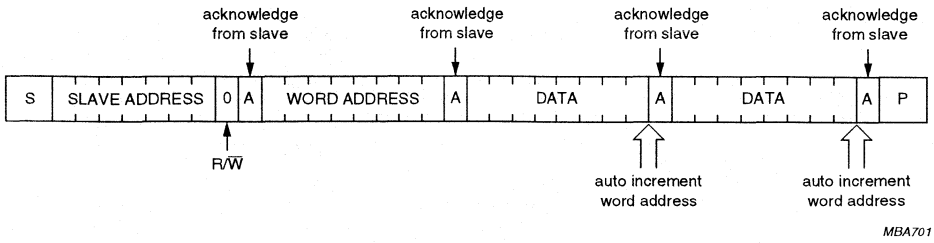


Fig.4 Auto increment memory word address; two byte write.

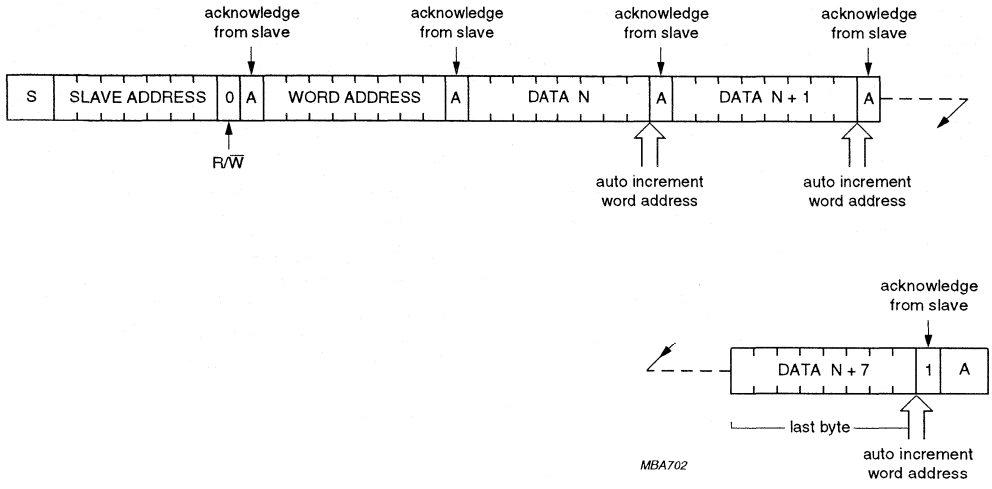


Fig.5 Page write operation; eight byte.

READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the LSB of the slave address is set to logic 1. There are three basic read operations; current address read, random read and sequential read.

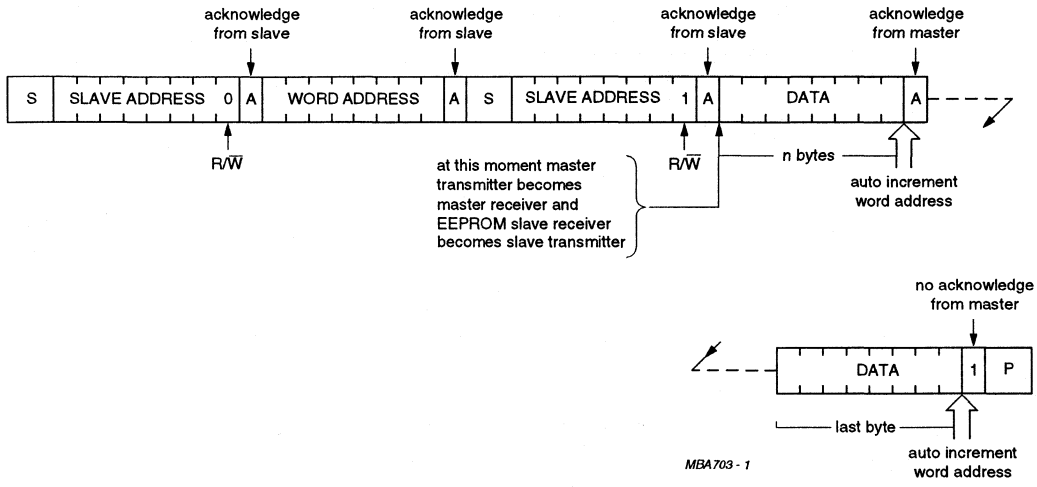


Fig.6 Master reads PCX8582X-2 slave after setting word address (WRITE word address; READ data).

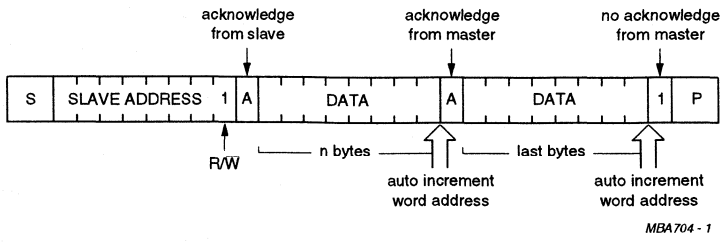


Fig.7 Master reads PCX8582X-2 immediately after first byte (READ mode).

I²C-BUS TIMING

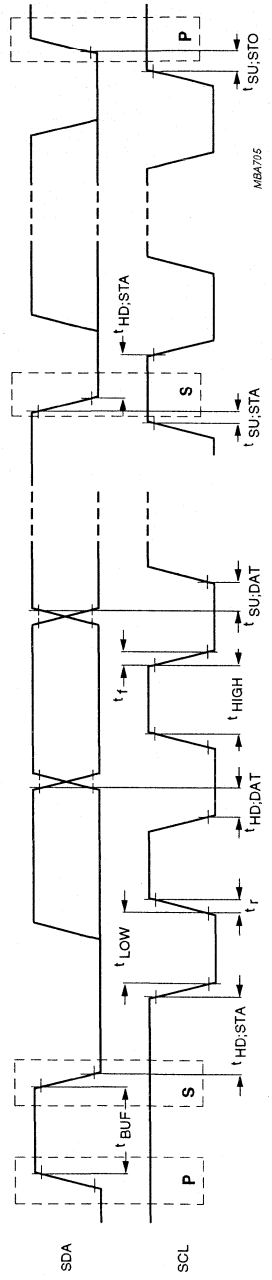


Fig.8 Timing requirements for the I²C-bus.

I²C-BUS CHARACTERISTICS

All of the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing from V_{SS} to V_{DD}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{SCL}	clock frequency		0	100	kHz
t_{BUF}	time the bus must be free before new transmission can start		4.7	–	µs
$t_{HD;STA}$	start condition hold time after which first clock pulse is generated		4.0	–	µs
t_{LOW}	LOW level clock period		4.7	–	µs
t_{HIGH}	HIGH level clock period		4.0	–	µs
$t_{SU;STA}$	set-up time for start condition	repeated start	4.7	–	µs
$t_{HD;DAT}$	data hold time for bus compatible masters		5	–	µs
$t_{HD;DAT}$	data hold time for bus devices	note 1	0	–	ns
$t_{SU;DAT}$	data set-up time		250	–	ns
t_r	SDA and SCL rise time		–	1	µs
t_f	SDA and SCL fall time		–	300	ns
$t_{SU;STO}$	set-up time for stop condition		4.7	–	µs

Note

1. The hold time required (not greater than 300 ns) to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter.

EXTERNAL CLOCK TIMING

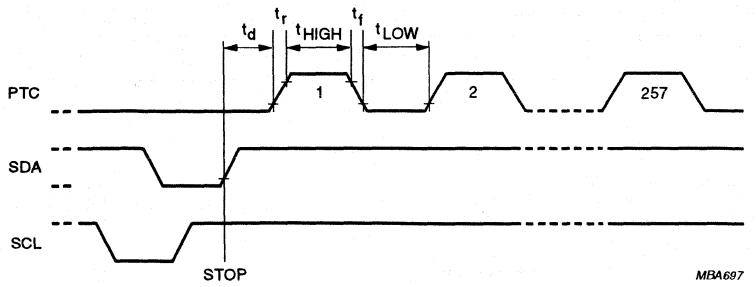


Fig.9 One byte ERASE/WRITE cycle.

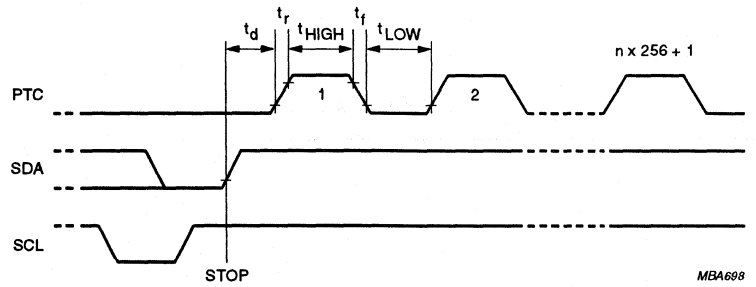


Fig.10 n byte ERASE/WRITE cycle (n = 2 to 7).

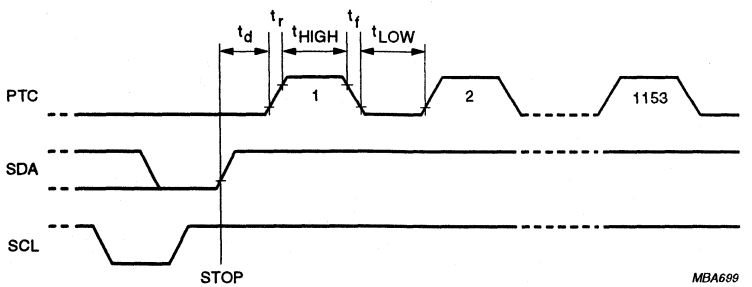
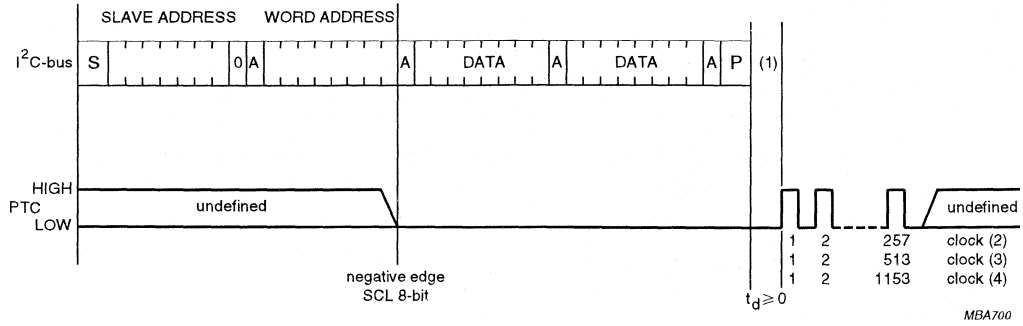


Fig.11 Page mode.



(1) If an external clock is chosen, this information is latched internally by setting pin 7 (PTC) LOW after transmission of the eighth bit of the word address (negative edge of SCL). Thus the state of pin 7 may be previously undefined. Leaving pin 7 LOW causes a higher standby current.

(2) 1-byte programming.

(3) 2-byte programming.

(4) One page (8 byte) programming.

Fig.12 External clock.

512 x 8-bit CMOS EEPROMS with I²C-bus interface

PCX8594X-2 Family

FEATURES

- Low power CMOS
  - maximum active current 2.5 mA
  - maximum standby current 10 µA (at 6.0 V), typical 4 µA
- Non-volatile storage of 4-Kbits organized as two pages of 256 × 8-bits each
- Single supply with full operation down to 2.5 V
- On-chip voltage multiplier
- Serial input/output I²C-bus
- Write operations
  - byte write mode
  - 8-byte page write mode (minimizes total write time per byte)
- Write-protection input
- Read operations
  - sequential read
  - random read
- Internal timer for writing (no external components)
- Power-on reset
- High reliability by using a redundant storage code (single bit error correction)
- Endurance
  - >500 k E/W-cycles at T_{amb} = 22 °C
- 40 years non-volatile data retention time (typ.)
- Pin and address compatible to
  - PCX8582X-2 Family and PCX8598X-2 Family.

DESCRIPTION

The PCX8594X-2 is a 4-Kbit (512 × 8-bit) floating gate electrically erasable programmable read only memory (EEPROM). By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip, using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to four PCX8594X-2 devices may be connected to the I²C-bus. Chip select is accomplished by two address inputs (A1 and A2).

Timing of the ERASE/WRITE cycle is carried out internally, thus no external components are required. Pin 7 (PTC) must be connected to either V_{DD} or left open-circuit.

There is an option of using an external clock for timing the length of an ERASE/WRITE cycle.

A write-protection input at pin 1 (WP) allows disable of write-commands from the master by a hardware signal. When pin 1 is HIGH and one of the upper 256 EEPROM cells is addressed, then the data bytes will not be acknowledged by the PCX8594X-2 and the EEPROM contents are not changed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.5	6.0	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	–	60	µA
		V_{DD} = 6 V	–	200	µA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	–	0.8	mA
		V_{DD} = 6 V	–	2.5	mA
I_{DDSB}	supply current STANDBY	V_{DD} = 3 V	–	3.5	µA
		V_{DD} = 6 V	–	10	µA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE (°C)		SUPPLY (V)	
	NAME	DESCRIPTION	VERSION	MIN.	MAX.	MIN.	MAX.
PCF8594C-2P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1	−40	+85	2.5	6.0
PCD8594D-2P				−25	+70	3.0	6.0
PCF8594E-2P				−40	+85	4.5	5.5
PCA8594F-2P				−40	+125	4.5	5.5
PCF8594C-2T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1	−40	+85	2.5	6.0
PCD8594D-2T				−25	+70	3.0	6.0
PCF8594E-2T				−40	+85	4.5	5.5
PCA8594F-2T				−40	+125	4.5	5.5

DEVICE SELECTION

Table 1 Device selection code

SELECTION	DEVICE CODE				CHIP ENABLE			R/$\overline{W}$
Bit	b7[1]	b6	b5	b4	b3	b2	b1	b0
Device	1	0	1	0	A2	A1	MEM SEL	R/$\overline{W}$

Note

1. The MSB b7 is sent first.

Table 2 Endurance and data retention guarantees

DEVICE	ENDURANCE E/W CYCLES	DATA RETENTION YEARS
PCF8594C-2; PCA8594F-2	500000[1]	40

Note

1. At the time of publication of this data sheet the statistical history was not yet sufficient to guarantee 1000000000 E/W cycle performance for these types.

BLOCK DIAGRAM

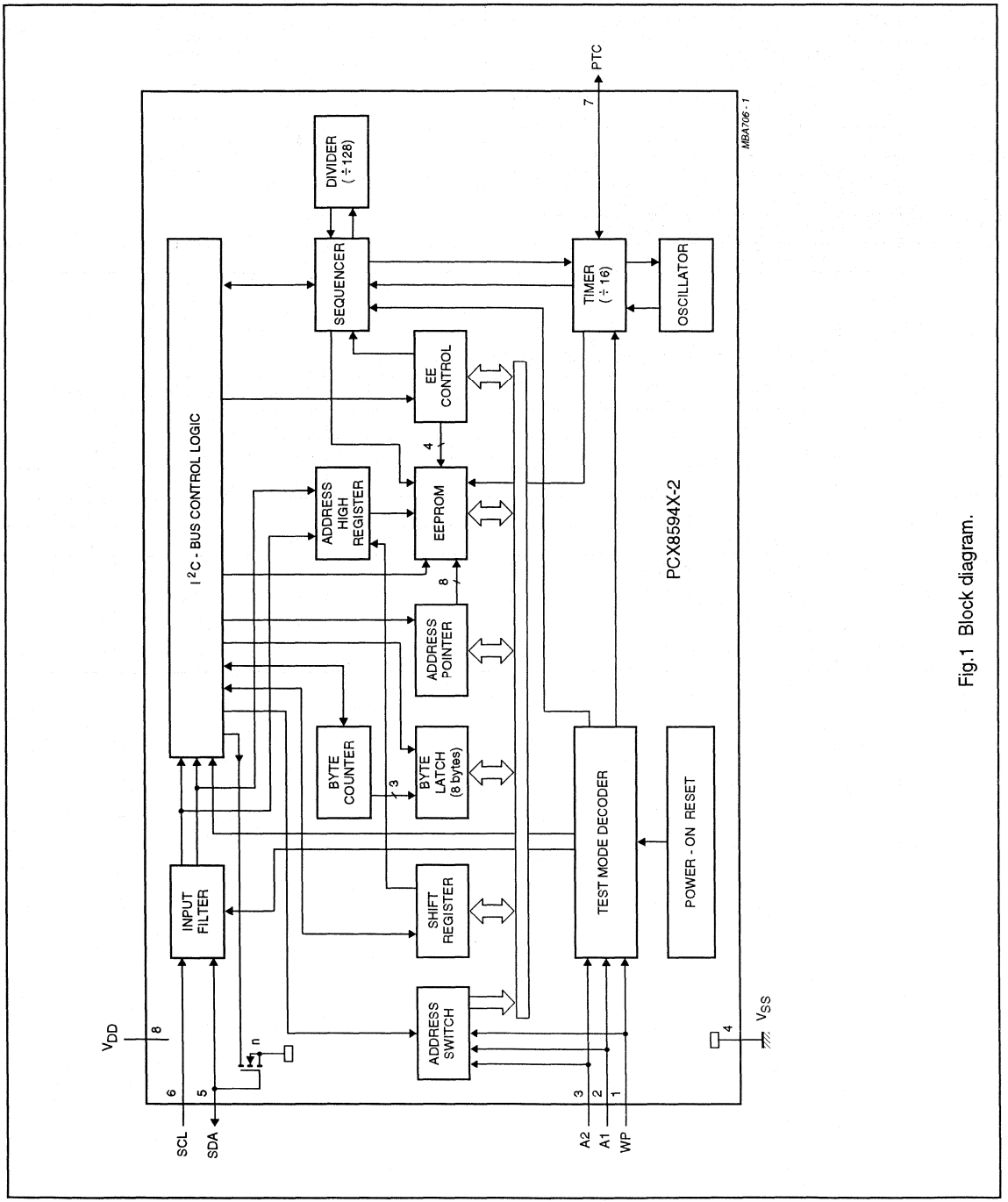


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
WP	1	write-protection input
A1	2	address input 1
A2	3	address input 2
V_{SS}	4	negative supply voltage
SDA	5	serial data input/output (I²C-bus)
SCL	6	serial clock input (I²C-bus)
PTC	7	programming time control output
V_{DD}	8	positive supply voltage

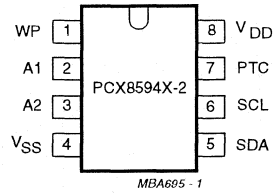


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.3	+7.0	V
V_I	voltage on any input pin	$\|Z_I\| > 500\ \Omega$	$V_{SS} - 0.8$	$V_{DD} + 0.8$	V
I_I	current on any input pin		–	1	mA
I_O	output current		–	10	mA
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature				
	PCF8594C-2; PCF8594E-2		−40	+85	°C
	PCD8594D-2		−25	+70	°C
	PCA8594F-2		−40	+125	°C

CHARACTERISTICS

PCF8594C-2: V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.
PCD8594D-2: V_{DD} = 3.0 to 6.0 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; unless otherwise specified.
PCF8594E-2: V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.
PCA8594F-2: V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +125 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supplies					
V_{DD}	supply voltage				
	PCF8594C-2		2.5	6.0	V
	PCD8594D-2		3.0	6.0	V
	PCF8594E-2; PCA8594F-2		4.5	5.5	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz			
	PCF8594C-2; PCD8594D-2	V_{DD} = 3.0 V	–	60	µA
		V_{DD} = 6.0 V	–	200	µA
	PCF8594E-2; PCA8594F-2	V_{DD} = 5.5 V	–	200	µA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz			
	PCF8594C-2; PCD8594D-2	V_{DD} = 3.0 V	–	0.8	mA
		V_{DD} = 6.0 V	–	2.5	mA
	PCF8594E-2; PCA8594F-2	V_{DD} = 5.5 V	–	2.5	mA
I_{DDSB}	supply current STANDBY	f_{SCL} = 100 kHz			
	PCF8594C-2; PCD8594D-2	V_{DD} = 3.0 V	–	3.5	µA
		V_{DD} = 6.0 V	–	10	µA
	PCF8594E-2; PCA8594F-2	V_{DD} = 5.5 V	–	10	µA
PTC input (pin 7)					
V_{IL}	LOW level input voltage		−0.8	$0.1V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.9V_{DD}$	V_{DD} + 0.8	V
SCL input (pin 6)					
V_{IL}	LOW level input voltage		−0.8	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	V_{DD} + 0.8	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	–	±1	µA
f_{SCL}	clock input frequency		0	100	kHz
C_I	input capacitance	$V_I = V_{SS}$	–	7	pF
SDA input/output (pin 5)					
V_{IL}	LOW level input voltage		−0.8	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	V_{DD} + 0.8	V
V_{OL}	LOW level output voltage	I_{OL} = 3 mA; $V_{DD(min)}$	–	0.4	V
I_{LO}	output leakage current	$V_{OH} = V_{DD}$	–	1	µA
C_I	input capacitance	$V_I = V_{SS}$	–	7	pF
Data retention time					
t_S	data retention time	T_{amb} = 55 °C	10	–	years

WRITE CYCLE LIMITS

The power-on reset circuit resets the I²C-bus logic with a set-up time of ≤10 µs.
Selection of the chip address is achieved by connecting the A1 and A2 inputs to either V_{SS} or V_{DD}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ERASE/WRITE cycle timing						
$t_{E/W}$	ERASE/WRITE cycle time					
	internal oscillator		–	7	–	ms
	external clock		4	–	10	ms
Endurance						
$N_{E/W}$	ERASE/WRITE cycle per byte					
	PCF8594C-2	T_{amb} = 85 °C; $t_{E/W}$ = 4 to 10 ms	100000	–	–	cycles
		T_{amb} = 22 °C; $t_{E/W}$ = 5 ms	500000	–	–	cycles
	PCD8594D-2	T_{amb} = −25 to +70 °C; $t_{E/W}$ = 4 to 10 ms	10000	–	–	cycles
		T_{amb} = −25 to +40 °C; $t_{E/W}$ = 5 ms	100000	–	–	cycles
	PCF8594E-2	T_{amb} = −40 to +85 °C; $t_{E/W}$ = 4 to 10 ms	10000	–	–	cycles
		T_{amb} = 22 °C; $t_{E/W}$ = 5 ms	100000	–	–	cycles
	PCA8594F-2	T_{amb} = 125 °C; $t_{E/W}$ = 4 to 10 ms	50000	–	–	cycles
		T_{amb} = 85 °C; $t_{E/W}$ = 4 to 10 ms	100000	–	–	cycles
		T_{amb} = 22 °C; $t_{E/W}$ = 5 ms	500000	–	–	cycles
Programming						
f_p	programming frequency		25	–	60	kHz
t_{LOW}	LOW time		5	–	–	µs
t_{HIGH}	HIGH time		5	–	–	µs
t_r	rise time		–	–	300	ns
t_f	fall time		–	–	300	ns
t_d	delay time		0	–	t_{LOW}	µs

I²C-BUS PROTOCOL

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The serial bus consists of two bidirectional lines: one for data signals (SDA), and one for clock signals (SCL).

Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

Bus not busy: both data and clock lines remain HIGH.

Start data transfer: a change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH, defines the start condition.

Stop data transfer: a change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH, defines the stop condition.

Data valid: the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to seven bytes in the ERASE/WRITE mode and eight bytes in the PAGE ERASE/WRITE mode. Data transfer is unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low-speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined.

The PCX8594X-2 operates in both modes.

By definition a device that sends a signal is called a 'transmitter', and the device which receives the signal is called a 'receive'. The device which controls the signal is called the 'master'. The devices that are controlled by the master are called 'slaves'.

Each byte is followed by one acknowledge bit. This acknowledge bit is a HIGH level, put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse. The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.

The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.

Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

DEVICE ADDRESSING

Following a start condition the bus master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Fig.3). For the PCX8594X-2 this is fixed as 1010.

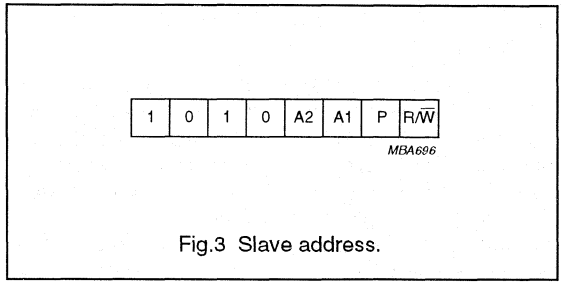


Fig.3 Slave address.

The next two significant bits address a particular device. A system could have up to four PCX8594X-2 devices on the bus. The four addresses are defined by the state of the A1 and A2 inputs.

The next bit (bit 1) of the slave address field is the page selection bit. It is used by the host to select the upper/lower 256 bytes of memory. This is, in effect, the most significant bit for the word address.

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read operation is selected.

Address bits must be connected to either V_{DD} or V_{SS}.

WRITE OPERATIONS

Byte/word write

For a write operation the PCX8594X-2 requires a second address field. This address field is a word address providing access to any one of the two 256 words of memory. Upon receipt of the word address the PCX8594X-2 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. Word address is automatically incremented. The master can now terminate the transfer by generating a stop condition or transmit up to six more bytes of data and then terminate by generating a stop condition.

After this stop condition the ERASE/WRITE cycle starts and the bus is free for another transmission. Its duration is 7 ms (typ.) per byte.

During the ERASE/WRITE cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

PAGE WRITE

The PCX8594X-2 is capable of an eight-byte page write operation. It is initiated in the same manner as the byte write operation. The master can transmit eight data bytes within one transmission. After receipt of each byte the PCX8594X-2 will respond with an acknowledge. The typical ERASE/WRITE time in this mode is 9×7 ms = 63 ms.

After the receipt of each data byte the three low order bits of the word address are internally incremented. The high order five bits of the address remain unchanged. If the master transmits more than eight bytes prior to generating the stop condition, no acknowledge will be given on the ninth (and following) data bytes and the whole transmission will be ignored. As in the byte write operation, all inputs are disabled until completion of the internal write cycles.

Remark

A write to the EEPROM is always performed if the pin WP is LOW. If WP is HIGH, then the upper half of the EEPROM is write-protected and no acknowledge will be given by the PCX8594X-2 when one of the upper 256 EEPROM bytes is addressed. However, an acknowledge will be given after the slave address and the word address.

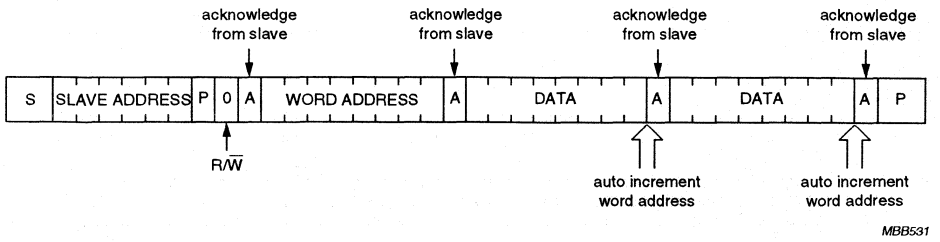


Fig.4 Auto increment memory word address; two byte write.

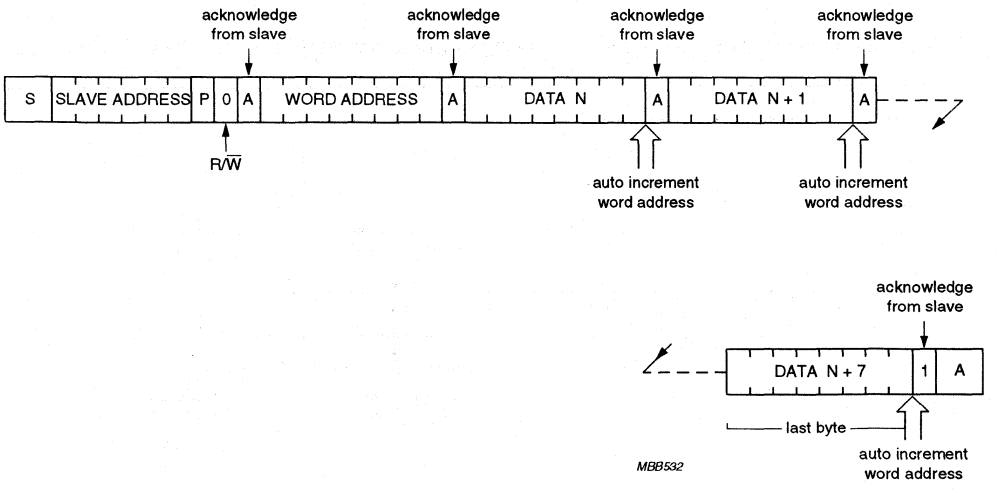


Fig.5 Page write operation; eight byte.

READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the LSB of the slave address is set to logic 1. There are three basic read operations; current address read, random read and sequential read.

Remark

The lower 8-bits of the word address are incremented after each transmission of a data byte (read or write). The MSB of the word address, which is defined in the slave address, is not changed when the word address count overflows. Thus, the word address overflows from 255 to 0 and from 511 to 256.

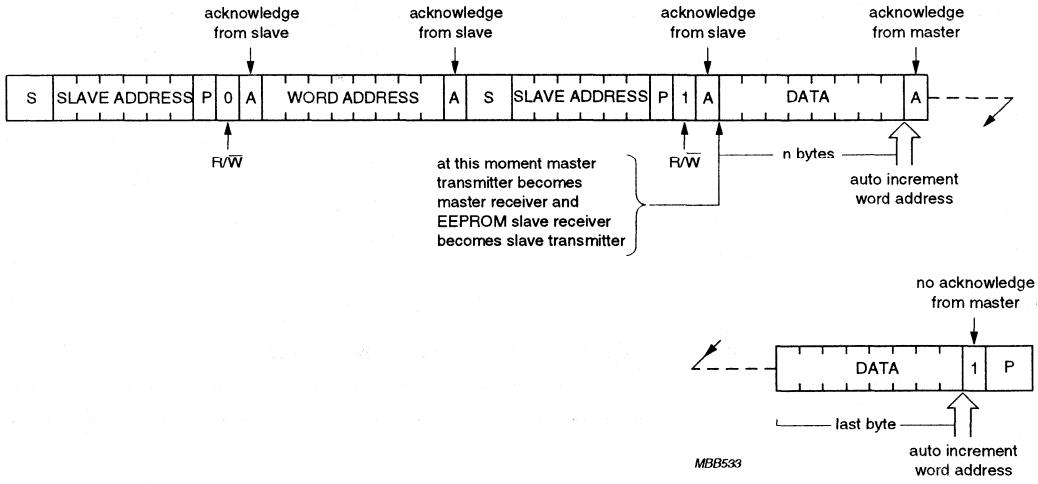


Fig.6 Master reads PCX8594X-2 slave after setting word address (WRITE word address; READ data).

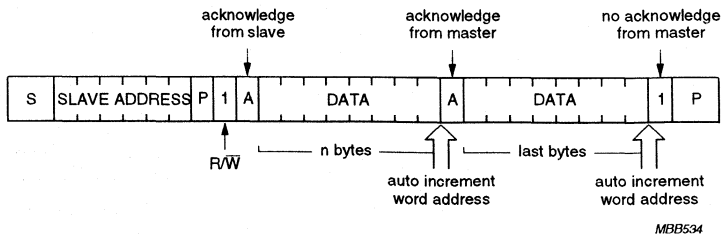


Fig.7 Master reads PCX8594X-2 immediately after first byte (READ mode).

I²C-BUS TIMING

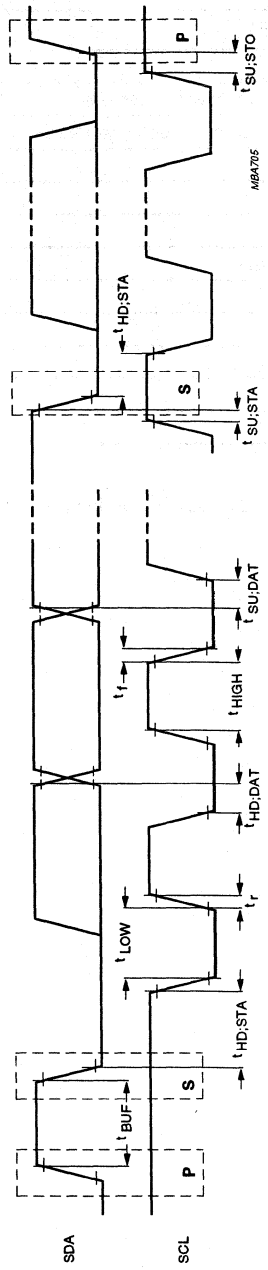


Fig.8 Timing requirements for the I²C-bus.

I²C-BUS CHARACTERISTICS

All of the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing from V_{SS} to V_{DD}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{SCL}	clock frequency		0	100	kHz
t_{BUF}	time the bus must be free before new transmission can start		4.7	–	µs
$t_{HD;STA}$	start condition hold time after which first clock pulse is generated		4.0	–	µs
t_{LOW}	LOW level clock period		4.7	–	µs
t_{HIGH}	HIGH level clock period		4.0	–	µs
$t_{SU;STA}$	set-up time for start condition	repeated start	4.7	–	µs
$t_{HD;DAT}$	data hold time for bus compatible masters		5	–	µs
$t_{HD;DAT}$	data hold time for bus devices	note 1	0	–	ns
$t_{SU;DAT}$	data set-up time		250	–	ns
t_r	SDA and SCL rise time		–	1	µs
t_f	SDA and SCL fall time		–	300	ns
$t_{SU;STO}$	set-up time for stop condition		4.7	–	µs

Note

1. The hold time required (not greater than 300 ns) to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter.

EXTERNAL CLOCK TIMING

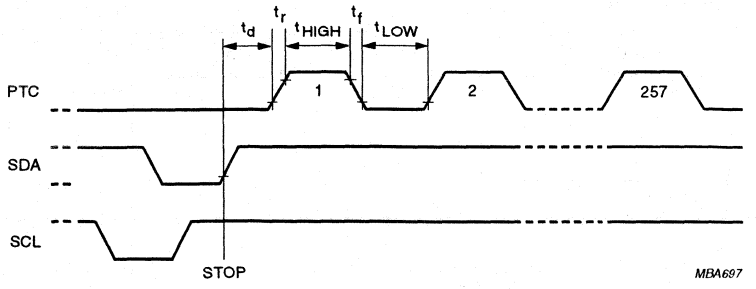


Fig.9 One byte ERASE/WRITE cycle.

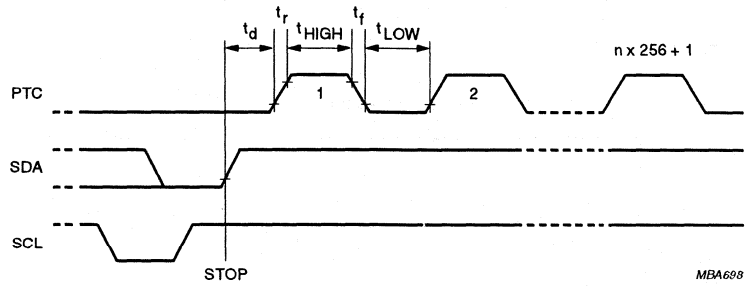


Fig.10 n byte ERASE/WRITE cycle (n = 2 to 7).

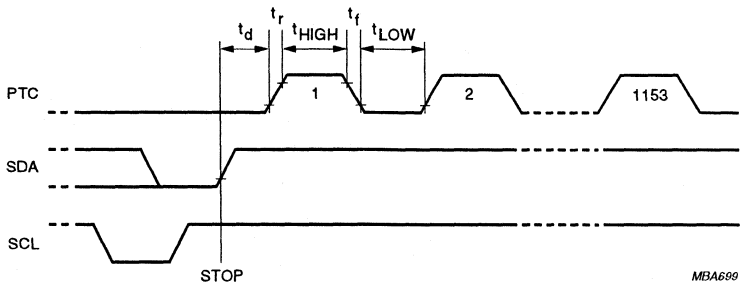
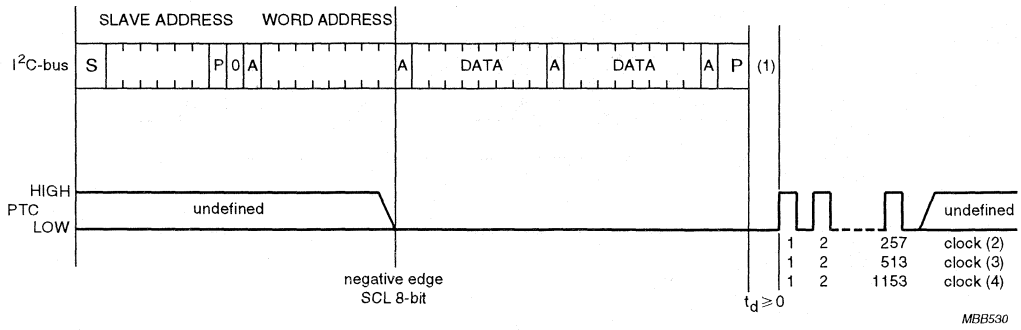


Fig.11 Page mode.



(1) If an external clock is chosen, this information is latched internally by setting pin 7 (PTC) LOW after transmission of the eighth bit of the word address (negative edge of SCL).
Thus the state of pin 7 may be previously undefined. Leaving pin 7 LOW causes a higher standby current.

(2) 1-byte programming.

(3) 2-byte programming.

(4) One page (8 byte) programming.

Fig.12 External clock.

1024 × 8-bit CMOS EEPROMS with I²C-bus interface

PCX8598X-2 Family

FEATURES

- Low power CMOS
  - maximum active current 4.0 mA
  - maximum standby current 10 μA (at 6.0 V), typical 4 μA
- Non-volatile storage of 8-Kbits organized as four pages of 256 × 8-bits each
- Single supply with full operation down to 2.5 V
- On-chip voltage multiplier
- Serial input/output I²C-bus
- Write operations
  - byte write mode
  - 8-byte page write mode (minimizes total write time per byte)
- Write-protection input
- Read operations
  - sequential read
  - random read
- Internal timer for writing (no external components)
- Power-on reset
- High reliability by using a redundant storage code (single bit error correction)
- Endurance
  - >500 k E/W-cycles at T_{amb} = 22 °C
- 40 years non-volatile data retention time (typ.)
- Pin and address compatible to
  - PCX8582X-2 Family and PCX8594X-2 Family.

DESCRIPTION

The PCX8598X-2 is an 8-Kbit (1024 × 8-bit) floating gate electrically erasable programmable read only memory (EEPROM). By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip, using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to two PCX8598X-2 devices may be connected to the I²C-bus. Chip select is accomplished by one address input (A2).

Timing of the ERASE/WRITE cycle is carried out internally, thus no external components are required. Pin 7 (PTC) must be connected to either V_{DD} or left open-circuit.

There is an option of using an external clock for timing the length of an ERASE/WRITE cycle.

A write-protection input at pin 1 (WP) allows disable of write-commands from the master by a hardware signal. When pin 1 is HIGH and one of the upper 512 EEPROM cells is addressed, then the data bytes will not be acknowledged by the PCX8598X-2 and the EEPROM contents are not changed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.5	6.0	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	–	60	μA
		V_{DD} = 6 V	–	200	μA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	–	1.0	mA
		V_{DD} = 6 V	–	4.0	mA
I_{DDSB}	supply current STANDBY	V_{DD} = 3 V	–	3.5	μA
		V_{DD} = 6 V	–	10	μA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE (°C)		SUPPLY (V)	
	NAME	DESCRIPTION	VERSION	MIN.	MAX.	MIN.	MAX.
PCF8598C-2P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1	−40	+85	2.5	6.0
PCD8598D-2P				−25	+70	3.0	6.0
PCF8598E-2P				−40	+85	4.5	5.5
PCA8598F-2P				−40	+125	4.5	5.5
PCF8598C-2T	SO8	plastic small outline package; 8 leads; body width 7.5 mm	SOT176-1	−40	+85	2.5	6.0
PCD8598D-2T				−25	+70	3.0	6.0
PCF8598E-2T				−40	+85	4.5	5.5
PCA8598F-2T				−40	+125	4.5	5.5

DEVICE SELECTION

Table 1 Device selection code

SELECTION	DEVICE CODE				CHIP ENABLE			R/$\overline{W}$
Bit	b7[1]	b6	b5	b4	b3	b2	b1	b0
Device	1	0	1	0	A2	MEM SEL	MEM SEL	R/$\overline{W}$

Note

1. The MSB b7 is sent first.

Table 2 Endurance and data retention guarantees

DEVICE	ENDURANCE E/W CYCLES	DATA RETENTION YEARS
PCF8598C-2; PCA8598F-2	500000[1]	40

Note

1. At the time of publication of this data sheet the statistical history was not yet sufficient to guarantee 1000000000 E/W cycle performance for these types.

BLOCK DIAGRAM

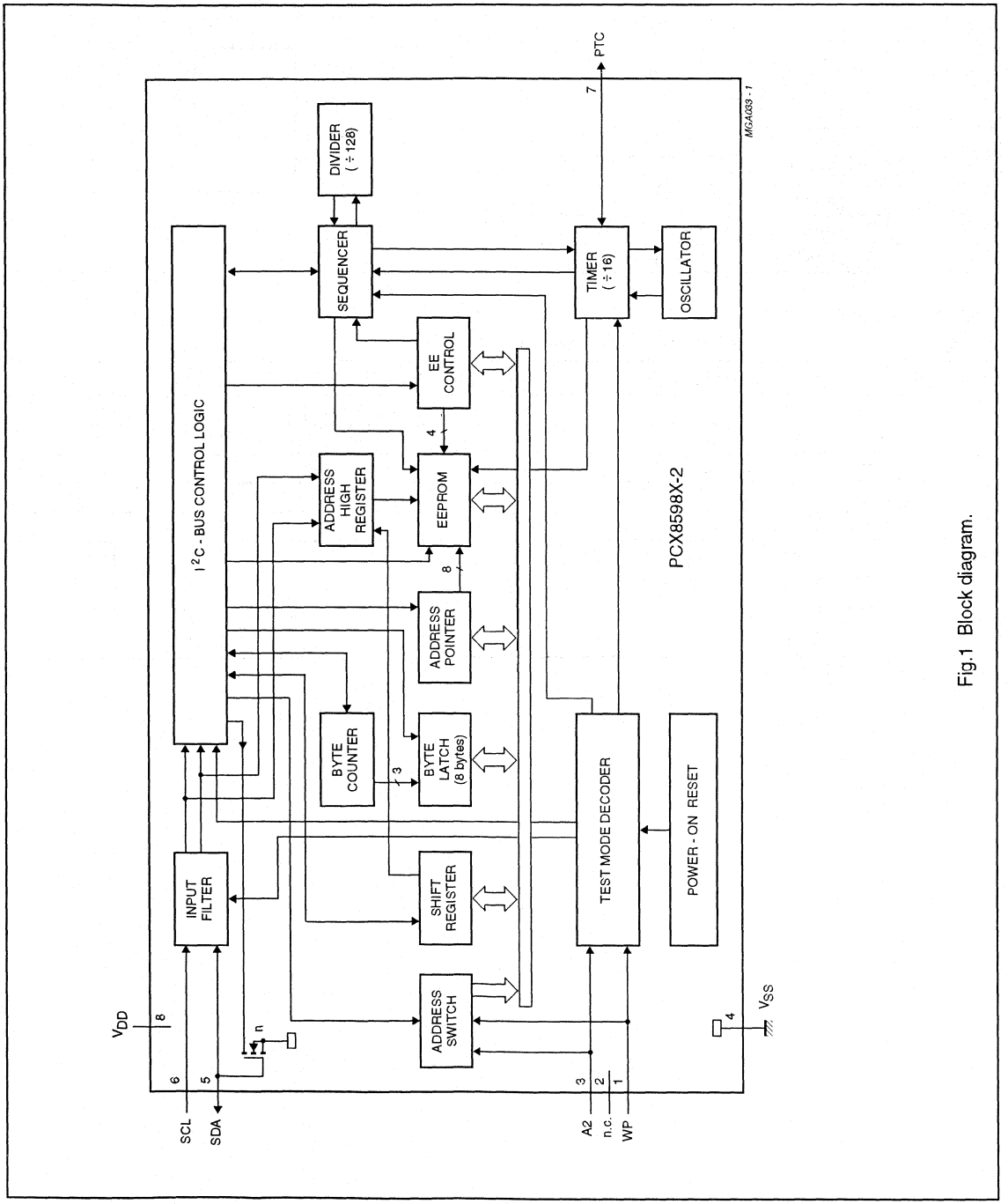


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
WP	1	write-protection input
n.c.	2	not connected
A2	3	address input 2
V_{SS}	4	negative supply voltage
SDA	5	serial data input/output (I²C-bus)
SCL	6	serial clock input (I²C-bus)
PTC	7	programming time control output
V_{DD}	8	positive supply voltage

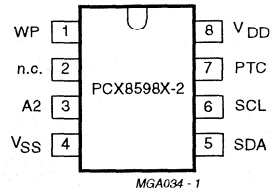


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.3	+7.0	V
V_I	voltage on any input pin	$\|Z_I\| > 500\ \Omega$	$V_{SS} - 0.8$	$V_{DD} + 0.8$	V
I_I	current on any input pin		−	1	mA
I_O	output current		−	10	mA
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature				
	PCF8598C-2; PCF8598E-2		−40	+85	°C
	PCD8598D-2		−25	+70	°C
	PCA8598F-2		−40	+125	°C

CHARACTERISTICS

PCF8598C-2: V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.
PCD8598D-2: V_{DD} = 3.0 to 6.0 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; unless otherwise specified.
PCF8598E-2: V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.
PCA8598F-2: V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +125 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supplies					
V_{DD}	supply voltage				
	PCF8598C-2		2.5	6.0	V
	PCD8598D-2		3.0	6.0	V
	PCF8598E-2; PCA8598F-2		4.5	5.5	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz			
	PCF8598C-2; PCD8598D-2	V_{DD} = 3.0 V	–	60	μA
		V_{DD} = 6.0 V	–	200	μA
	PCF8598E-2; PCA8598F-2	V_{DD} = 5.5 V	–	200	μA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz			
	PCF8598C-2; PCD8598D-2	V_{DD} = 3.0 V	–	1.0	mA
		V_{DD} = 6.0 V	–	4.0	mA
	PCF8598E-2; PCA8598F-2	V_{DD} = 5.5 V	–	4.0	mA
I_{DDSB}	supply current STANDBY	f_{SCL} = 100 kHz			
	PCF8598C-2; PCD8598D-2	V_{DD} = 3.0 V	–	3.5	μA
		V_{DD} = 6.0 V	–	10	μA
	PCF8598E-2; PCA8598F-2	V_{DD} = 5.5 V	–	10	μA
PTC input (pin 7)					
V_{IL}	LOW level input voltage		−0.8	$0.1V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.9V_{DD}$	V_{DD} + 0.8	V
SCL input (pin 6)					
V_{IL}	LOW level input voltage		−0.8	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	V_{DD} + 0.8	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	–	±1	μA
f_{SCL}	clock input frequency		0	100	kHz
C_I	input capacitance	$V_I = V_{SS}$	–	7	pF
SDA input/output (pin 5)					
V_{IL}	LOW level input voltage		−0.8	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	V_{DD} + 0.8	V
V_{OL}	LOW level output voltage	I_{OL} = 3 mA; $V_{DD(min)}$	–	0.4	V
I_{LO}	output leakage current	$V_{OH} = V_{DD}$	–	1	μA
C_I	input capacitance	$V_I = V_{SS}$	–	7	pF
Data retention time					
t_S	data retention time	T_{amb} = 55 °C	10	–	years

WRITE CYCLE LIMITS

The power-on reset circuit resets the I²C-bus logic with a set-up time of ≤10 µs.
Selection of the chip address is achieved by connecting the A2 input to either V_{SS} or V_{DD}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ERASE/WRITE cycle timing						
$t_{E/W}$	ERASE/WRITE cycle time					
	internal oscillator		–	7	–	ms
	external clock		4	–	10	ms
Endurance						
$N_{E/W}$	ERASE/WRITE cycle per byte					
	PCF8598C-2	T_{amb} = 85 °C; $t_{E/W}$ = 4 to 10 ms	100000	–	–	cycles
		T_{amb} = 22 °C; $t_{E/W}$ = 5 ms	500000	–	–	cycles
	PCD8598D-2	T_{amb} = −25 to +70 °C; $t_{E/W}$ = 4 to 10 ms	10000	–	–	cycles
		T_{amb} = −25 to +40 °C; $t_{E/W}$ = 5 ms	100000	–	–	cycles
	PCF8598E-2	T_{amb} = −40 to +85 °C; $t_{E/W}$ = 4 to 10 ms	10000	–	–	cycles
		T_{amb} = 22 °C; $t_{E/W}$ = 5 ms	100000	–	–	cycles
	PCA8598F-2	T_{amb} = 125 °C; $t_{E/W}$ = 4 to 10 ms	50000	–	–	cycles
		T_{amb} = 85 °C; $t_{E/W}$ = 4 to 10 ms	100000	–	–	cycles
		T_{amb} = 22 °C; $t_{E/W}$ = 5 ms	500000	–	–	cycles
Programming						
f_p	programming frequency		25	–	60	kHz
t_{LOW}	LOW time		5	–	–	µs
t_{HIGH}	HIGH time		5	–	–	µs
t_r	rise time		–	–	300	ns
t_f	fall time		–	–	300	ns
t_d	delay time		0	–	t_{LOW}	µs

I²C-BUS PROTOCOL

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The serial bus consists of two bidirectional lines: one for data signals (SDA), and one for clock signals (SCL).

Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

- **Bus not busy:** both data and clock lines remain HIGH.

  Start data transfer: a change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH, defines the start condition.
- **Stop data transfer:** a change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH, defines the stop condition.
- **Data valid:** the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to seven bytes in the ERASE/WRITE mode and eight bytes in the PAGE ERASE/WRITE mode. Data transfer is unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low-speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined.

The PCX8598X-2 operates in both modes.

By definition a device that sends a signal is called a 'transmitter', and the device which receives the signal is called a 'receive'. The device which controls the signal is called the 'master'. The devices that are controlled by the master are called 'slaves'.

Each byte is followed by one acknowledge bit. This acknowledge bit is a HIGH level, put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse. The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.

The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.

Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

DEVICE ADDRESSING

Following a start condition the bus master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Fig.3). For the PCX8598X-2 this is fixed as 1010.

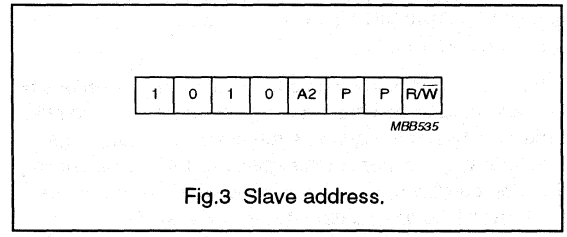


Fig.3 Slave address.

The next significant bit (A2) addresses a particular device. A system could have up to two PCX8598X-2 devices on the bus. The two addresses are defined by the state of the A2 input.

The next two significant bits of the slave address field are the page selection bits. It is used by the host to select one out of four pages (page = 256 bytes of memory). These are, in effect, the two most significant bits of the word address.

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read operation is selected.

Address bit A2 must be connected to either V_{DD} or V_{SS}.

WRITE OPERATIONS

Byte/word write

For a write operation the PCX8598X-2 requires a second address field. This address field is a word address providing access to any one of the four 256 words of memory. Upon receipt of the word address the PCX8598X-2 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. Word address is automatically incremented. The master can now terminate the transfer by generating a stop condition or transmit up to six more bytes of data and then terminate by generating a stop condition.

After this stop condition the ERASE/WRITE cycle starts and the bus is free for another transmission. Its duration is 7 ms (typ.) per byte.

During the ERASE/WRITE cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

PAGE WRITE

The PCX8598X-2 is capable of an eight-byte page write operation. It is initiated in the same manner as the byte write operation. The master can transmit eight data bytes within one transmission. After receipt of each byte the PCX8598X-2 will respond with an acknowledge. The typical ERASE/WRITE time in this mode is 9×7 ms = 63 ms.

After the receipt of each data byte the three low order bits of the word address are internally incremented. The high order five bits of the address remain unchanged. If the master transmits more than eight bytes prior to generating the stop condition, no acknowledge will be given on the ninth (and following) data bytes and the whole transmission will be ignored. As in the byte write operation, all inputs are disabled until completion of the internal write cycles.

Remark

A write to the EEPROM is always performed if the pin WP is LOW. If WP is HIGH, then the upper half of the EEPROM is write-protected and no acknowledge will be given by the PCX8598X-2 when one of the upper 512 EEPROM bytes is addressed. However, an acknowledge will be given after the slave address and the word address.

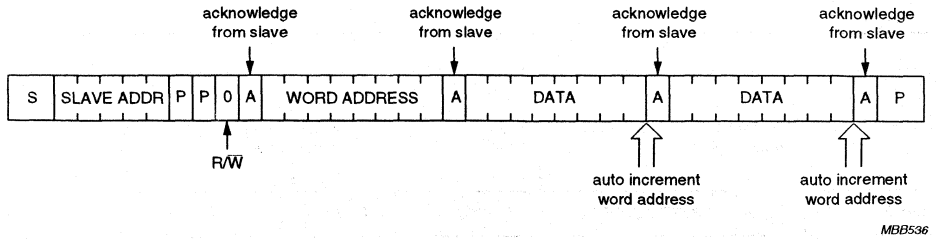


Fig.4 Auto increment memory word address; two byte write.

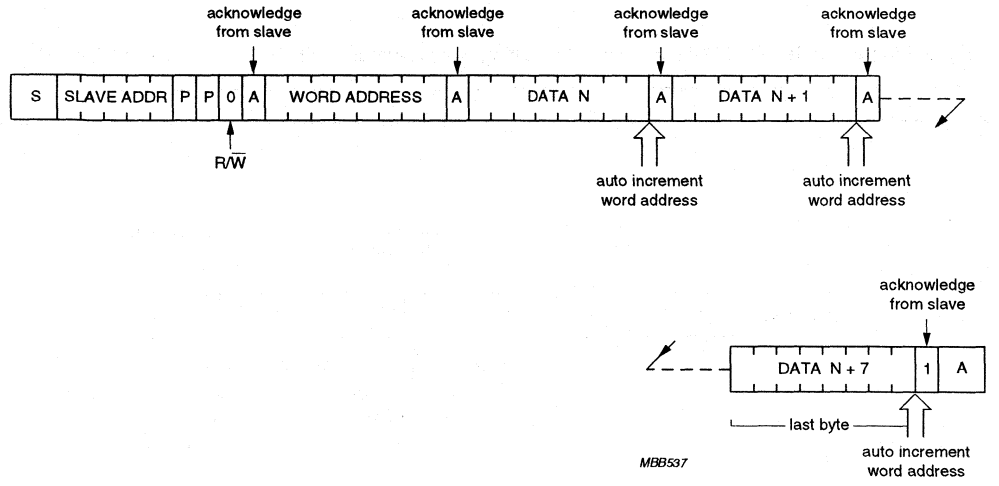


Fig.5 Page write operation; eight byte.

READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the LSB of the slave address is set to logic 1. There are three basic read operations; current address read, random read and sequential read.

Remark

The lower 8-bits of the word address are incremented after each transmission of a data byte (read or write). The MSB of the word address, which is defined in the slave address, is not changed when the word address count overflows. Thus, the word address overflows from 255 to 0, from 511 to 256, from 767 to 512 and from 1023 to 768.

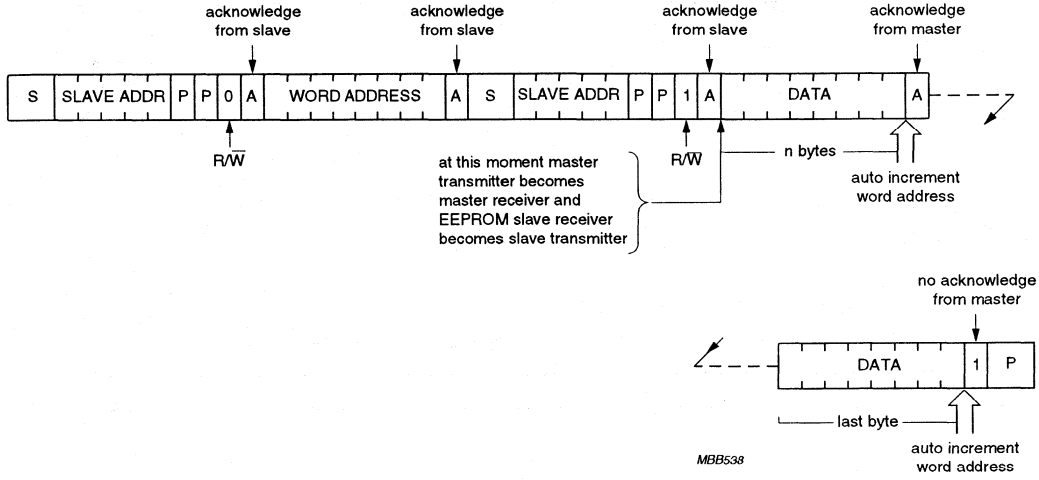


Fig.6 Master reads PCX8598X-2 slave after setting word address (WRITE word address; READ data).

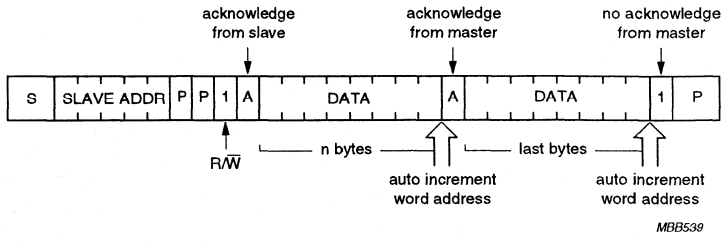


Fig.7 Master reads PCX8598X-2 immediately after first byte (READ mode).

I²C-BUS TIMING

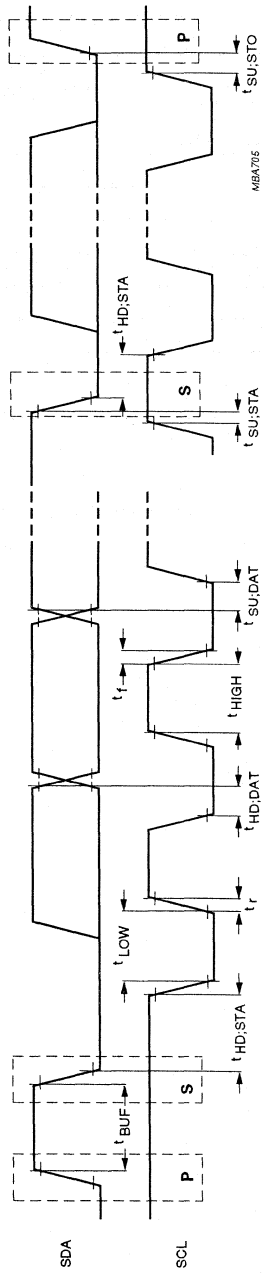


Fig.8 Timing requirements for the I²C-bus.

I²C-BUS CHARACTERISTICS

All of the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing from V_{SS} to V_{DD}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{SCL}	clock frequency		0	100	kHz
t_{BUF}	time the bus must be free before new transmission can start		4.7	–	µs
$t_{HD;STA}$	start condition hold time after which first clock pulse is generated		4.0	–	µs
t_{LOW}	LOW level clock period		4.7	–	µs
t_{HIGH}	HIGH level clock period		4.0	–	µs
$t_{SU;STA}$	set-up time for start condition	repeated start	4.7	–	µs
$t_{HD;DAT}$	data hold time for bus compatible masters		5	–	µs
$t_{HD;DAT}$	data hold time for bus devices	note 1	0	–	ns
$t_{SU;DAT}$	data set-up time		250	–	ns
t_r	SDA and SCL rise time		–	1	µs
t_f	SDA and SCL fall time		–	300	ns
$t_{SU;STO}$	set-up time for stop condition		4.7	–	µs

Note

1. The hold time required (not greater than 300 ns) to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter.1

EXTERNAL CLOCK TIMING

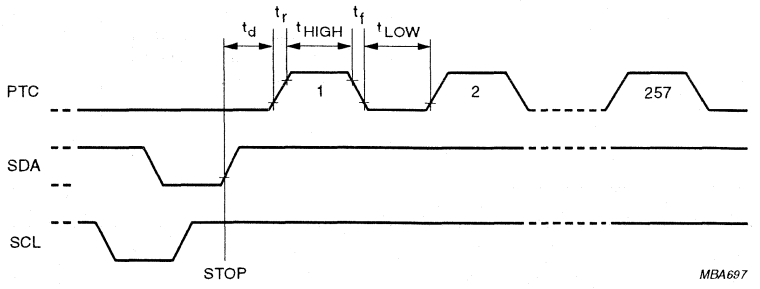


Fig.9 One byte ERASE/WRITE cycle.

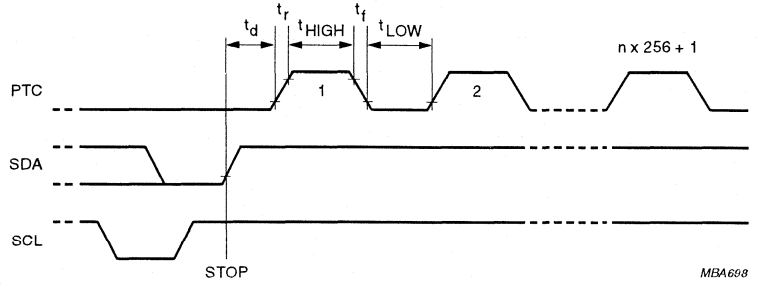


Fig.10 n byte ERASE/WRITE cycle (n = 2 to 7).

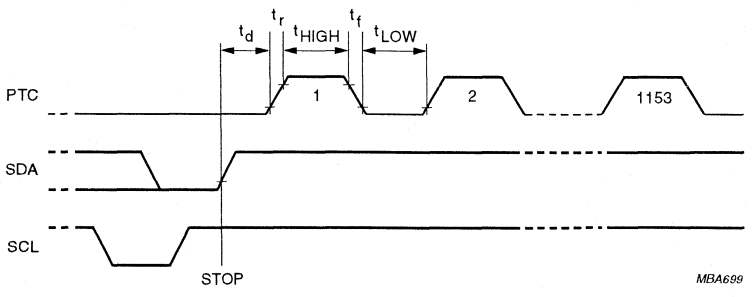
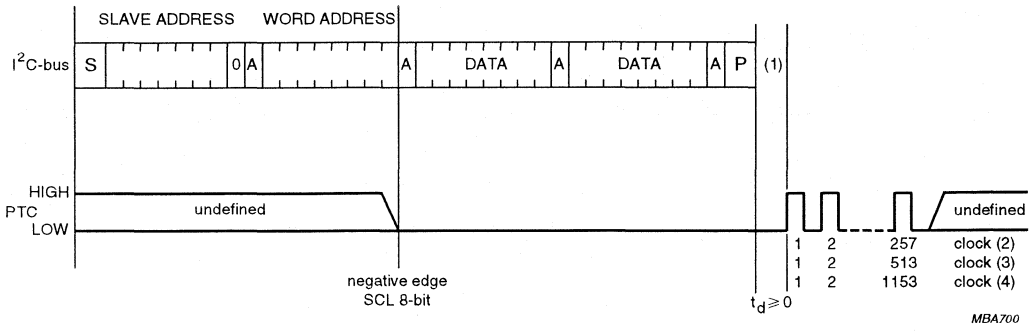


Fig.11 Page mode.



(1) If an external clock is chosen, this information is latched internally by setting pin 7 (PTC) LOW after transmission of the eighth bit of the word address (negative edge of SCL). Thus the state of pin 7 may be previously undefined. Leaving pin 7 LOW causes a higher standby current.

(2) 1-byte programming.

(3) 2-byte programming.

(4) One page (8 byte) programming.

Fig.12 External clock.

4-DIGIT LED-DRIVER WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The LED-driver is a bipolar integrated circuit made in an I²L compatible 18 volts process. The circuit is especially designed to drive four 7-segment LED displays with decimal point by means of multiplexing between two pairs of digits. It features an I²C-Bus slave transceiver interface with the possibility to program four different SLAVE ADDRESSES, a POWER RESET flag, 16 current sink OUTPUTS, controllable by software up to 21 mA, two multiplex drive outputs for common anode segments, an on-chip multiplex oscillator, control bits to select static, dynamic and blank mode, and one bit for segment test.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	$V_{EE} = 0$ V	V_{CC}	4.5	5	15	V
Supply current all outputs OFF	$V_{CC} = 5$ V	I_{CC}*	7	9.5	14	mA
Total power dissipation 24-lead DIL (SOT101B)		P_{tot}	–	–	1000	mW
24-lead DIL SO (SOT137A)		P_{tot}	–	–	500	mW
Operating ambient temperature range		T_{amb}	–40	–	+85	°C

* The positive current is defined as the conventional current flow into a device (sink current).

PACKAGE OUTLINE

SAA1064: 24-lead DIL; plastic with internal heat spreader (SOT101B).
SAA1064T: 24-lead mini-pack; plastic (SO-24; SOT137A).

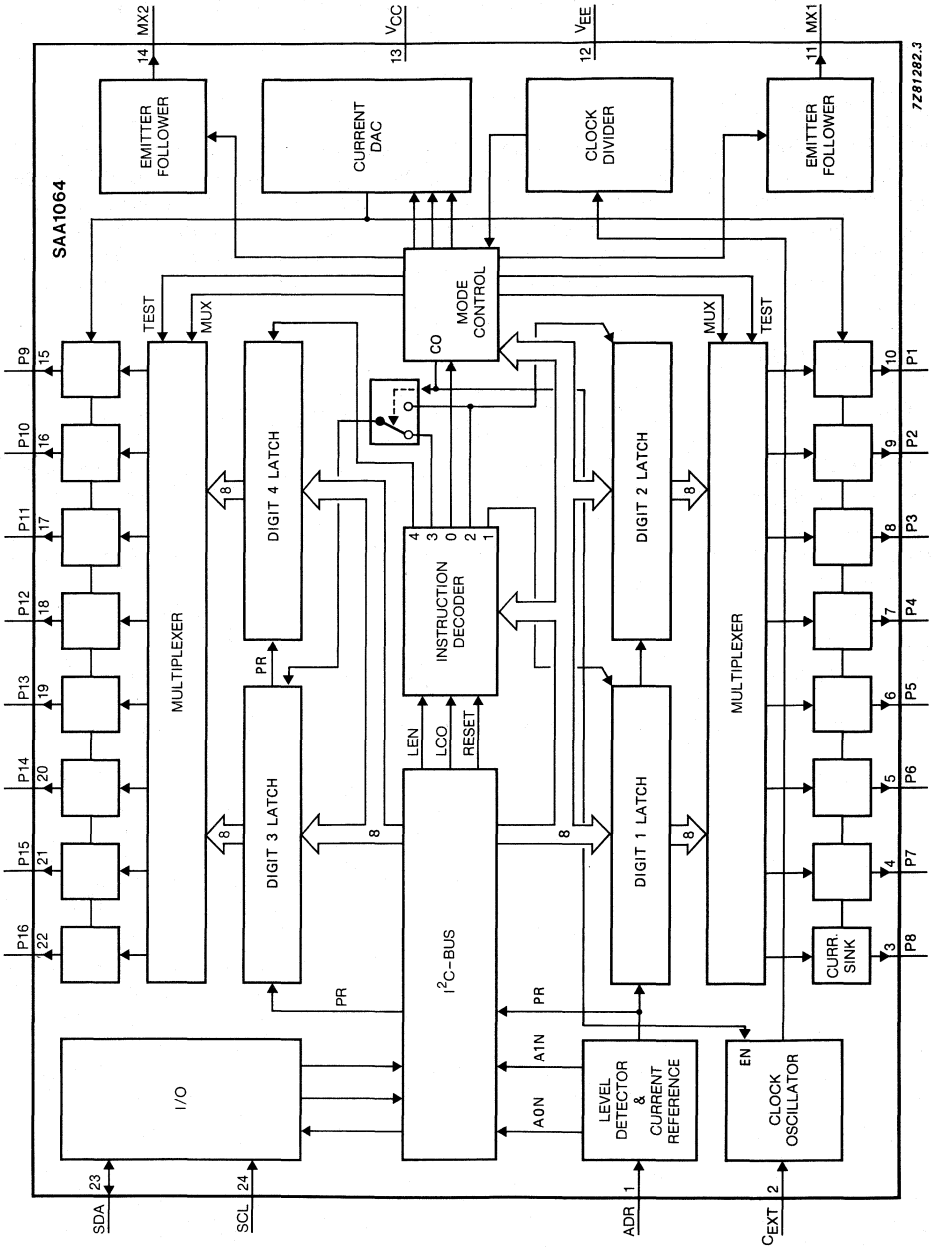


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
ADR	1	I²C-Bus slave address input
C_{EXT}	2	external control
P8 to P1	3-10	segment output
MX1	11	multiplex output
V_{EE}	12	ground
V_{CC}	13	positive supply
MX2	14	multiplex output
P9 to P16	15-22	segment output
SDA	23	I²C-Bus serial data line
SCL	24	I²C-Bus serial clock line

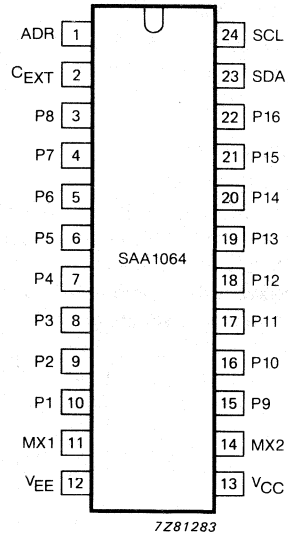


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

slave address status byte

Fig. 3a I²C-Bus format; READ mode.

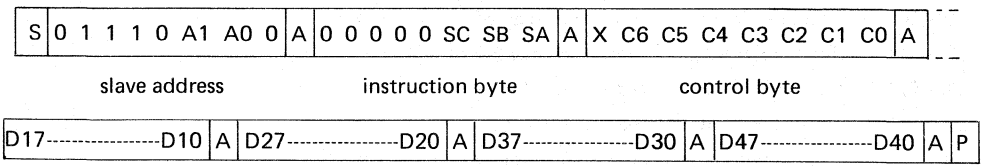


Fig. 3b I²C-Bus format; WRITE mode.

S = start condition
P = stop condition
A = acknowledge
X = don't care

A1, A0 = programmable address bits
SC SB SA = subaddress bits
C6 to C0 = control bits
PR = POWER RESET flag

Address pin ADR

Four different slave addresses can be chosen by connecting ADR either to V_{EE}, 3/8 V_{CC}, 5/8 V_{CC} or V_{CC}. This results in the corresponding valid addresses HEX 70, 72, 74 and 76 for writing and 71, 73, 75 and 77 for reading. All other addresses cannot be acknowledged by the circuit.

Status byte

Only one bit is present in the status byte, the POWER RESET flag. A logic 1 indicates the occurence of a power failure since the last time it was read out. After completion of the READ action this flag will be set to logic 0.

Subaddressing

The bits SC, SB and SA form a pointer and determine to which register the data byte following the instruction byte will be written. All other bytes will then be stored in the registers with consecutive subaddresses. This feature is called Auto-Increment (AI) of the subaddress and enables a quick initialization by the master.
The subaddress pointer will wrap around from 7 to 0.
The subaddresses are given as follows:

SC	SB	SA	sub-address	function
0	0	0	00	control register
0	0	1	01	digit 1
0	1	0	02	digit 2
0	1	1	03	digit 3
1	0	0	04	digit 4
1	0	1	05	reserved, not used
1	1	0	06	
1	1	1	07	

Control bits (see Fig. 4)

The control bits C0 to C6 have the following meaning:

C0 = 0	static mode, i.e. continuous display of digits 1 and 2
C0 = 1	dynamic mode, i.e. alternating display of digit 1 + 3 and 2 + 4
C1 = 0/1	digits 1 + 3 are blanked/not blanked
C2 = 0/1	digits 2 + 4 are blanked/not blanked
C3 = 1	all segment outputs are switched-on for segment test*
C4 = 1	adds 3 mA to segment output current
C5 = 1	adds 6 mA to segment output current
C6 = 1	adds 12 mA to segment output current

Data

A segment is switched ON if the corresponding data bit is logic 1. Data bits D17 to D10 correspond with digit 1, D27 to D20 with digit 2, D37 to D30 with digit 3 and D47 to D40 with digit 4.
The MSBs correspond with outputs P8 and P16, the LSBs with P1 and P9. Digit numbers 1 to 4 are equal to their subaddresses (hex) 1 to 4.

* At a current determined by C4, C5 and C6.

SDA, SCL

The SDA and SCL I/O meet the I²C-Bus specification. For protection against positive voltage pulses on these inputs voltage regulator diodes are connected to V_{EE}. This means that normal line voltage should not exceed 5,5 volt. Data will be latched on the positive-going edge of the acknowledge related clock pulse.

Power-on reset

The power-on reset signal is generated internally and sets all bits to zero, resulting in a completely blanked display. Only the POWER RESET flag is set.

External Control (C_{EXT})

With a capacitor connected to pin 2 the multiplex frequency can be set (see Fig. 5). When static this pin can be connected to V_{EE} or V_{CC} or left floating since the oscillator will be switched off.

Segment outputs

The segment outputs P1 to P16 are controllable current-sink sources. They are switched on by the corresponding data bits and their current is adjusted by control bits C4, C5 and C6.

Multiplex outputs

The multiplex outputs MX1 and MX2 are switched alternately in dynamic mode with a frequency derived from the clock-oscillator. In static mode MX1 is switched on. The outputs consist of an emitter-follower, which can be used to drive the common anodes of two displays directly provided that the total power dissipation of the circuit is not exceeded. If this occurs external transistors should be connected to pins 11 and 14 as shown in Fig. 5.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 13)	$V_{EE} = 0$ V	V_{CC}	−0.5	18	V
Supply current (pin 13)		I_{CC}	−50	200	mA
Total power dissipation					
24-lead DIL (SOT101B)		P_{tot}		1000	mW
24-lead SO (SO137A)		P_{tot}		500	mW
SDA, SCL voltages	$V_{EE} = 0$ V	$V_{23,24}$	−0.5	5.9	V
Voltages ADR-MX1 and MX2-P16	$V_{EE} = 0$ V	$V_{1\text{-}11}$, $V_{14\text{-}22}$	−0.5	$V_{CC}+0.5$	V
Input/output current all pins	outputs OFF	$\pm I_{I/O}$	−	10	mA
Operating ambient temperature range		T_{amb}	−40	+85	°C
Storage temperature range		T_{stg}	−55	+150	°C

THERMAL RESISTANCE

From crystal to ambient

24-lead DIL	$R_{th\,j\text{-}a}$	35 K/W
24-lead SO (on ceramic substrate)	$R_{th\,j\text{-}a}$	75 K/W
24-lead SO (on printed circuit board)	$R_{th\,j\text{-}a}$	105 K/W

CHARACTERISTICS

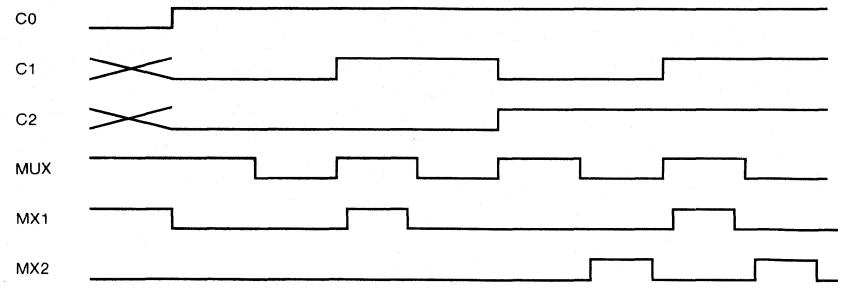
V_{CC} = 5 V; T_{amb} = 25 °C; voltages are referenced to ground (V_{EE} = 0 V); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 13)		V_{CC}	4,5	5,0	15	V
Supply current	all outputs OFF V_{CC} = 5 V	I_{CC}	7,0	9,5	14,0	mA
Power dissipation	all outputs OFF	P_d	–	50	–	mW
SDA; SCL (pins 23 and 24)						
Input voltages		$V_{23,24}$	0	–	5,5	V
Logic input voltage LOW		$V_{IL(L)}$	–	–	1,5	V
Logic input voltage HIGH		$V_{IH(L)}$	3,0	–	–	V
Input current LOW	$V_{23,24} = V_{EE}$	$-I_{IL}$	–	–	10	μA
Input current HIGH	$V_{23,24} = V_{CC}$	I_{IH}	–	–	10	μA
SDA						
Logic output voltage LOW	I_O = 3 mA	$V_{OL(L)}$	–	–	0,4	V
Output sink current		I_{SDA}	3	–	–	mA
Address input (pin 1)						
Input voltage programmable address bits:						
A0 = 0; A1 = 0		V_1	V_{EE}	–	$3/16V_{CC}$	V
A0 = 1; A1 = 0		V_1	$5/16V_{CC}$	$3/8V_{CC}$	$7/16V_{CC}$	V
A0 = 0; A1 = 1		V_1	$9/16V_{CC}$	$5/8V_{CC}$	$11/16V_{CC}$	V
A0 = 1; A1 = 1		V_1	$13/16V_{CC}$	–	V_{CC}	V
Input current LOW	$V_1 = V_{EE}$	$-I_1$	–	–	10	μA
Input current HIGH	$V_1 = V_{CC}$	I_1	–	–	10	μA
External control (C_{EXT}) pin 2						
Switching level input						
Input voltage LOW		V_{IL}	–	–	$V_{CC}-3,3$	V
Input voltage HIGH		V_{IH}	$V_{CC}-1,5$	–	–	V
Input current	V_2 = 2 V	I_2	−140	−160	−180	μA
	V_2 = 4 V	I_2	140	160	180	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Segment outputs (P8 to P1; pins 3 to 10) P9 to P16; pins 15 to 22)						
Output voltages	I_O = 15 mA	V_O	–	–	0.5	V
Output leakage current HIGH	$V_O = V_{CC}$ = 15 V	I_{LO}	–	–	± 10	μA
Output current LOW						
All control bits (C4, C5 and C6) are HIGH	V_{OL} = 5 V	I_{OL}	17.85	21	25.2	mA
Contribution of:						
control bit C4		I_O	2.55	3.0	3.6	mA
control bit C5		I_O	5.1	6.0	7.2	mA
control bit C6		I_O	10.2	12.0	14.4	mA
Relative segment output current accuracy						
with respect to highest value		ΔI_O	–	–	7.5	%
Multiplex 1 and 2 (pins 11 and 14)						
Maximum output voltage (when ON)	$-I_{MPX}$ = 50 mA	V_{MPX}	V_{CC}–1.5	–	–	V
Maximum output current HIGH (when ON)	V_{MPX} = 2 V	$-I_{MPX}$	50	–	110	mA
Maximum output current LOW (when OFF)	V_O = 2 V	$+ I_{MPX}$	50	70	110	μA
Multiplex output period	C_{EXT} = 2.7 nF	T_{MPX}	5	–	10	ms
Multiplexed duty factor			–	48.4	–	%

* Value to be fixed.



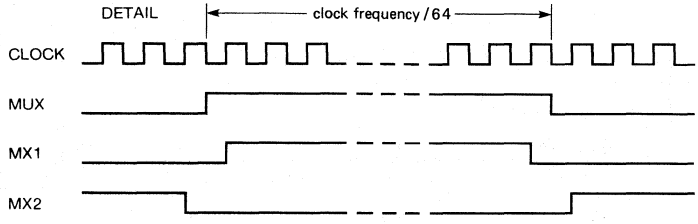


Fig. 4 Timing diagram.

APPLICATION INFORMATION

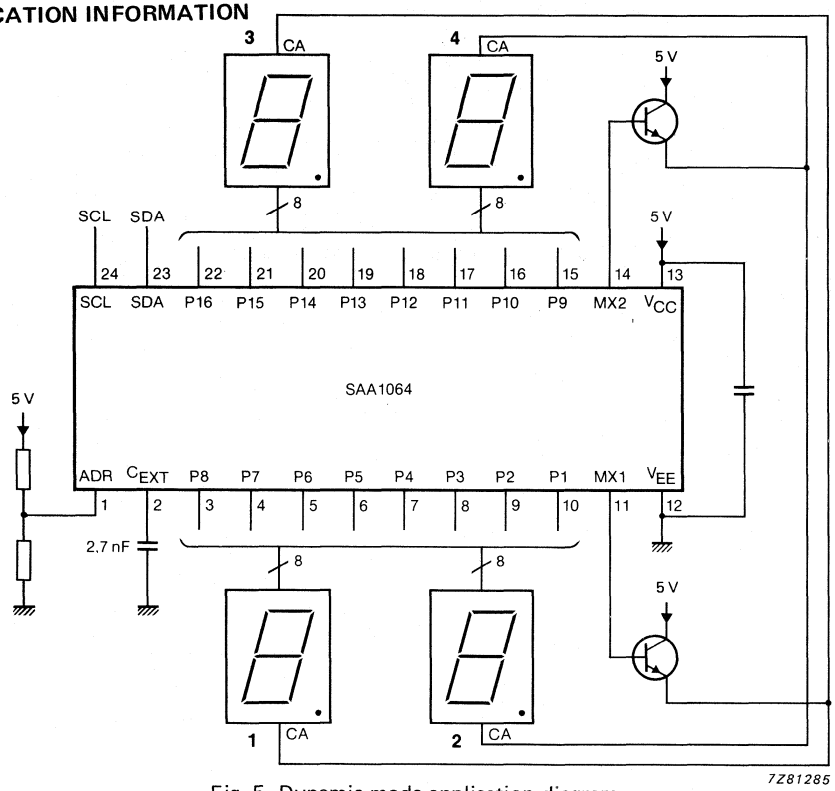


Fig. 5 Dynamic mode application diagram.

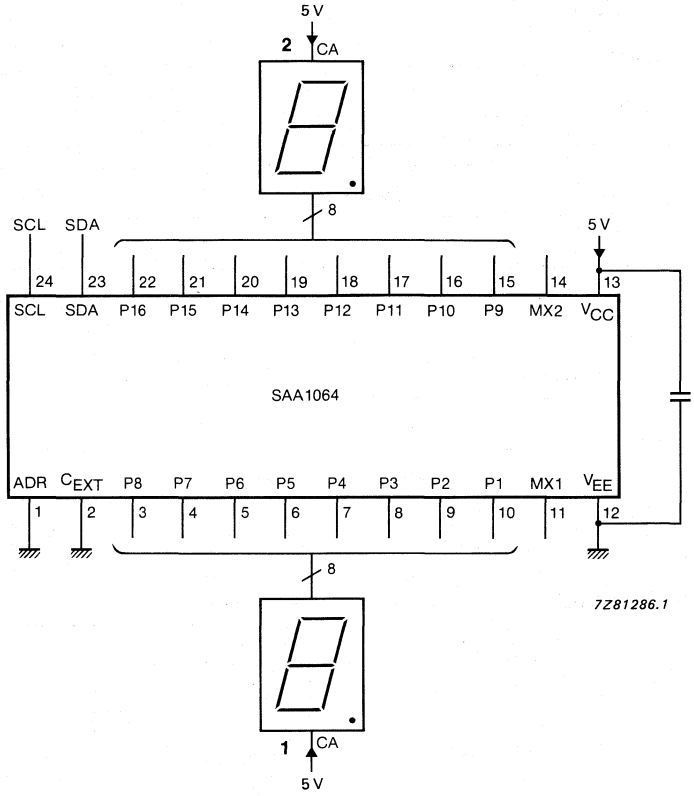


Fig. 6 Static mode application diagram.

POWER DISSIPATION

The total maximum power dissipation of the SAA1064 is made up by the following parts:

1. Maximum dissipation when none of the outputs are programmed (continuous line in Fig.7).
2. Maximum dissipation of each programmed output. The dashed line in Fig.7 visualises the dissipation when **all** the segments are programmed (max. 16 in the static, and max. 32 in the dynamic mode). When less segments are programmed one should take a proportional part of the maximum value.
3. Maximum dissipation of the programmed segment drivers which can be expressed as: $P_{add} = V_o \times I_o \times N$.

Where:
- P_{add} = The additional power dissipation of the segment drivers
- V_o = The low state segment driver output voltage
- I_o = The programmed segment output current
- N = The number of programmed segments in the static mode, or half the number of programmed segment drivers in the dynamic mode.

Under no conditions the total maximum dissipation (500 mW for the SO and 1000 mW for the DIL package) should be exceeded.

Example: V_{cc} = 5 V

V_o = 0.25 V

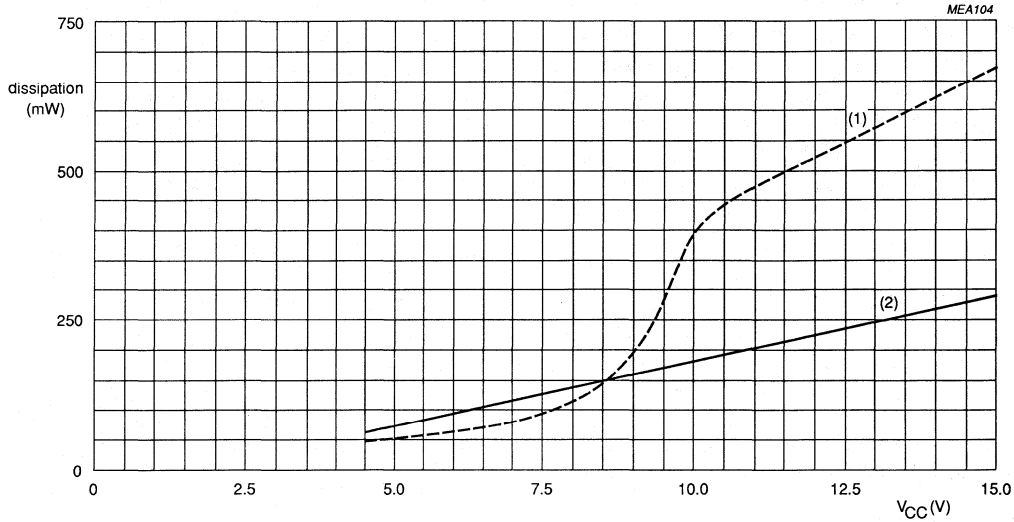
I_o = 12 mA

24 programmed segments in dynamic mode

$P_{tot} = P_1 + P_2 + P_3$

$= 75\ mW + (50 * 24/32)\ mW + (0.25 * 12.10^{-3} * 12)\ mW$

$= 148.5\ mW$



(1) All outputs programmed (no segment current sink).

(2) Outputs not programmed.

Fig.7 SAA1064 power dissipation as a function of supply voltage.

TUNER SWITCHING CIRCUIT

The SAA1300 is for switching on and off the supply lines of various circuit parts via an I²C bus signal. Furthermore, it can be used to supply current for switching diodes in radio and television tuners. It contains 5 output stages, which are capable of supplying up to 85 mA in the ON state or sinking up to −100 μA in the OFF state.

Current limiting and short-circuit protection are included. The output stages are driven by a shift register/latch combination which is loaded via data from the I²C bus. A power-on reset of the latches ensures the OFF state of the output stages (OUT 2 to OUT 5) without data reception from the I²C bus. A subaddressing system allows the connection of up to three circuits on the same I²C bus lines; one of the outputs (OUT 1, pin 7) can also be used as an input to select the device via a simple internal A/D converter.

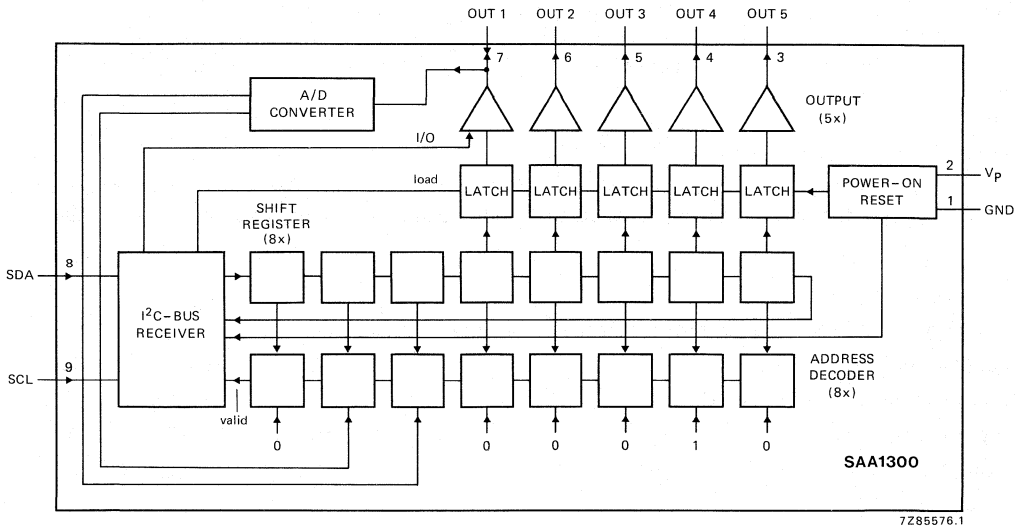


Fig. 1 Block diagram.

PACKAGE OUTLINE

9-lead SIL; plastic (SOT142).

PINNING

pin no.	symbol	function
1	GND	ground
2	V_P	positive supply
3	OUT 5	outputs
4	OUT 4	
5	OUT 3	
6	OUT 2	
7	OUT 1	output and subaddressing input
8	SDA	serial data line (I^2C bus)
9	SCL	serial clock line (I^2C bus)

I^2C BUS INFORMATION

Address, first byte

0 1 0 0 0 A B 0 where,

A	B	function	condition
0	0	general address	OUT 1 = output
0	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,L}$ (LOW)
1	0	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,H}$ (HIGH)
1	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,M}$ (MEDIUM)

Data, second byte

OUT 5, OUT 4, OUT 3, OUT 2, OUT 1, X, X, X

The I/O output stage (OUT 1) is switched as an input stage after a power-on reset. It depends on the contents of the first data transmission whether the output stage is switched as an output or remains as an input.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max. 13,2	V
Input voltage range at SDA, SCL	V_I	−0,5 to + 6,0	V
Input voltage range at OUT 1	V_I	−0,5 to + 12,5	V
Output voltage range at OUT 1 to OUT 5	V_O	−0,5 to + 12,5	V
Input current at SDA, SCL	I_I	max. 20	mA
Input current at OUT 1	I_I	max. 20	mA
Total power dissipation	P_{tot}	max. 825	mW
Storage temperature range	T_{stg}	−40 to + 125	°C
Operating ambient temperature range	T_{amb}	−20 to + 80	°C

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 2)					
Supply voltage range	V_P	4	8	12	V
Supply current					
5 outputs LOW	I_{PL}	5	10	15	mA
5 outputs HIGH	I_{PH}	30	50	70	mA
Power-on reset level output stage in "OFF' condition	V_{PR}	–	3,5	3,8	V
Maximum power dissipation*	P_{max}	–	650	–	mW
Inputs SDA, SCL (pins 8 and 9)					
Input voltage HIGH	V_{IH}	3,0	–	5,5	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input current HIGH	$-I_{IH}$	–	–	10	μA
Input current LOW	I_{IH}	–	–	0,4	μA
Acknowledge sink current	I_{ACK}	2,5	–	–	mA
Maximum input frequency	$f_{i\,max}$	100	–	–	kHz
Outputs OUT 1 to OUT 5 (pins 3 to 7)					
Maximum output current; source: "ON"	I_{Oso}	+ 85	–	+ 150	mA
Maximum output current; source: "ON" T_{amb} = 80 °C	I_{Oso}	60	–	–	mA
Output voltage HIGH at I_{Oso} = 85 mA	V_{OH}	V_P–2	–	–	V
Output current; sink "OFF"	I_{Osi}	–100	–300	–	μA
Output voltage LOW at I_{Osi} = –100 μA	V_{OL}	–	–	100	mV
Output voltage MEDIUM at I_O = 10 mA	V_{OM}	V_P–0,5	–	–	V
OUT 1 used as subaddressing input					
Input voltage HIGH (code 1 0)	$V_{OUT\,1H}$	0,72 V_P	–	V_P	V
Input voltage MEDIUM (code 1 1)	$V_{OUT\,1M}$	0,39 V_P	–	0,61 V_P	V
Input voltage LOW (code 0 1)	$V_{OUT\,1L}$	0	–	0,28 V_P	V

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

* Outputs must not be driven simultaneously at maximum source current.

I²C-BUS INTERFACE FOR COLOUR DECODERS

GENERAL DESCRIPTION

The TDA8442 provides control of four analogue functions and has one high-current and two switching outputs. Control of the IC is performed via the two-line, bidirectional I²C-bus.

Features

- Four analogue control outputs
- One high-current output port (npn open emitter)
- Two switching output ports (npn collector with internal pull-up resistor)
- I²C-bus slave receiver
- Power-down reset

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 9)		V_P	10.8	12.0	13.2	V
Supply current	no outputs loaded	I_P	8	13	18	mA
Total power dissipation	no outputs loaded	P_{tot}	–	–	1	W
Operating ambient temperature range		T_{amb}	−20	–	+70	°C

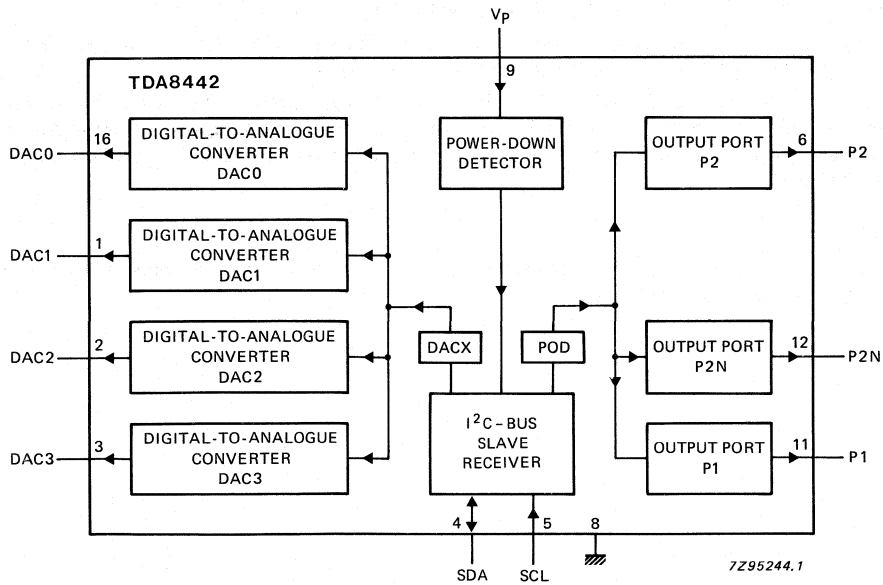


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

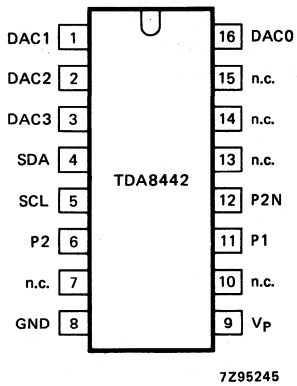


Fig. 2 Pinning diagram

PINNING

1	DAC1	analogue output 1
2	DAC2	analogue output 2
3	DAC3	analogue 3
4	SDA	serial data line } I^2C-bus
5	SCL	serial clock line } I^2C-bus
6	P2	Port 2 npn collector output with internal pull-up resistor
7	n.c.	not connected
8	GND	supply return (ground)
9	V_P	positive supply voltage
10	n.c.	not connected
11	P1	Port 1 open npn emitter output
12	P2N	inverted P2 output
13	n.c.	not connected
14	n.c.	not connected
15	n.c.	not connected
16	DAC0	analogue output 0

FUNCTIONAL DESCRIPTION

Control

Analogue control is facilitated by four 6-bit digital-to-analogue converters (DAC0 to DAC3). The values of the output voltages from the DACs are set via the I^2C-bus.

The high-current output port (P1) is suitable for switching between internal and external RGB signals. It is an open npn emitter output capable of sourcing 14 mA (min.).

The two output ports (P2 and P2N) can be used for NTSC/PAL switching. These are npn collector outputs with internal pull-up resistors of 10 kΩ (typ.). Both outputs are capable of sinking up to 2 mA with a voltage drop of less than 400 mV. If one output is switched on (LOW), the other output is switched off, and vice versa.

Reset

The power-down-reset mode occurs whenever the positive supply voltage falls below 8.5 V (typ.) and resets all registers to a defined state.

OPERATION

Write

The TDA8442 is controlled via the I²C-bus (specifications for the I²C-bus will be supplied on request). Programming of the TDA8442 is performed using the format shown in Fig. 3.

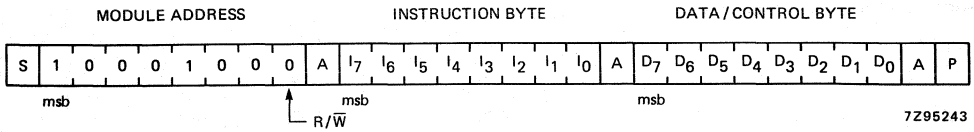


Fig. 3 TDA8442 programming format.

Acknowledge (A) is generated by the TDA8442 only when a valid address is received and the device is not in the power-down-reset mode ($V_P > 8.5$ V (typ.)).

Control

Control is implemented by the instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) together with the corresponding data/control bytes (see Fig. 4).

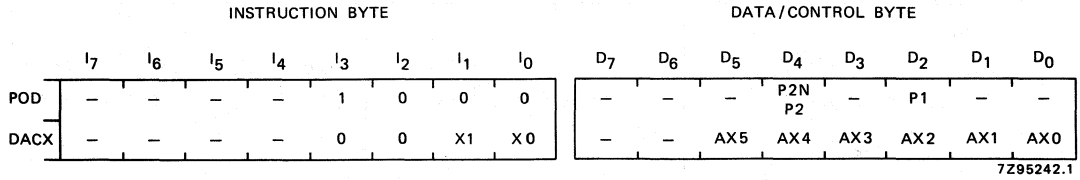


Fig. 4 Control programming.

POD bit P1: If a logic 1 is programmed, the P1 output is switched on. If a logic 0 is programmed or after a power-down-reset, the P1 output is switched off (high-impedance state).

POD bit P2/P2N: If a logic 1 is programmed, the P2 output is switched off and the P2N output is switched on (LOW). If a logic 0 is programmed or after a power-down-reset, the P2 output is switched on (LOW) and the P2N output is switched off.

DAX bits AX5 to AX0: The digital-to-analogue converter selected corresponds to the decimal equivalent of the two bits X1 and X0. The output voltage of the selected DAC is programmed using bits AX5 to AX0, the lowest value being with all data AX5 to AX0 at logic 0 or when power-down-reset has been activated.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 9)	V_P	−0.3	+ 13.2	V
Input/output voltage ranges				
pin 4	V_{SDA}	−0.3	+ 13.2	V
pin 5	V_{SCL}	−0.3	+ 13.2	V
pin 6	V_{P2}	−0.3	V_P*	V
pin 11	V_{P1}	−0.3	V_P*	V
pin 12	V_{P2N}	−0.3	V_P*	V
pins 1 to 3 and pin 16	V_{DAX}	−0.3	V_P*	V
Total power dissipation	P_{tot}	−	1	W
Operating ambient temperature range	T_{amb}	−20	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = + 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 9)		V_P	10.8	12.0	13.2	V
Supply current (pin 9)	no outputs loaded	I_P	8	13	18	mA
I²C-bus inputs						
SDA (pin 4); SCL (pin 5)						
Input voltage HIGH	note 1	V_{IH}	3.0	−	V_P−1	V
Input voltage LOW		V_{IL}	−0.3	−	1.5	V
Input current HIGH	note 1	I_{IH}	−	−	10	μA
Input current LOW	note 1	I_{IL}	−	−	10	μA
I²C-bus output						
SDA (pin 4)	open collector					
Output voltage LOW	I_{OL} = 3.0 mA	V_{OL}	−	−	0.4	V
Maximum output sink current		I_{OL}	3	5	−	mA

* Pin voltage may exceed V_P if the current in that pin is limited to 10 mA.

parameter	conditions	symbol	min.	typ.	max.	unit
Ports P2 and P2N (pins 6 and 12)	npn collector output with pull-up resistor to V_P					
Internal pull-up resistor to V_P		R_O	5	10	15	kΩ
Output voltage switched on (LOW)	I_{OL} = 2 mA	V_{OL}	–	–	0.4	V
Maximum output sink current		I_{OL}	2	5	–	mA
Leakage current output switched off		$-I_{leak}$	–	–	25	μA
Port P1 (pin 11)	open npn emitter output					
Output current switched on	V_O = 0 to 5 V	I_O	14	–	–	mA
Leakage current switched off	V_O = 0 to V_P	$\pm I_{leak}$	–	–	100	μA
Digital-to-analogue outputs	note 2					
DAC0 (pin 16)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	3.0	–	4.25	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	0.15	–	1.0	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	16	–	72	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	45	mV
Output impedance	I_O = –2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
DAC1 (pin 1)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	4.0	–	5.0	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	1.0	–	1.7	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	18	–	86	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	50	mV
Output impedance	I_O = –2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Digital-to-analogue outputs (continued)						
DAC2 (pin 2)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	4.0	–	5.0	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	1.0	–	1.7	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	18	–	86	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	50	mV
Output impedance	I_O = –2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
DAC3 (pin 3)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	10.0	–	11.2	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	0.1	–	1.0	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	70	–	250	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	150	mV
Output impedance	I_O = –2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
Power-down reset						
Maximum value of V_P at which power-down reset is active		V_{PD}	6	–	10	V
Rise time of V_P during power-on	V_P rising from 0 V to V_{PD}	t_r	5	–	–	μs

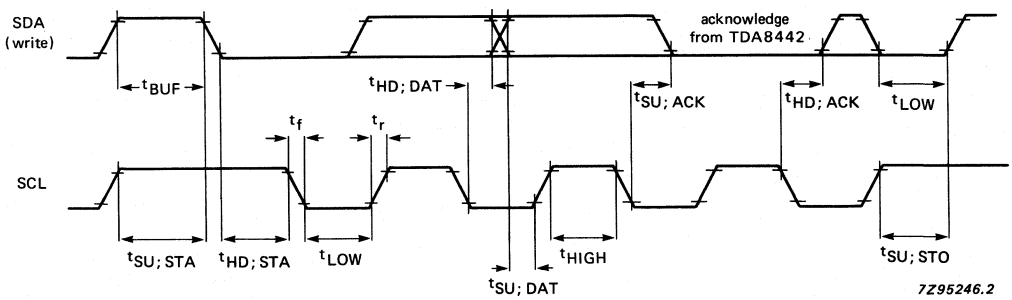
Notes to the characteristics

1. If $V_p < 1$ V, the input current is limited to 10 μA at input voltages up to 13.2 V.
2. Pure capacitive load should be avoided because of possible oscillations.
3. Values are proportional to V_P.

I²C-BUS TIMING

Bus loading conditions: 4 kΩ pull-up resistor to + 5 V; 200 pF capacitor to GND. All values are referred to V_{IH} = 3 V and V_{IL} = 1.5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4.0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
LOW period SCL, SDA	t_{LOW}	4.0	–	–	μs
HIGH period SCL	t_{HIGH}	4.0	–	–	μs
Rise time SCL, SDA	t_r	–	–	1.0	μs
Fall time SCL, SDA	t_f	–	–	0.30	μs
Data set-up time (write)	$t_{SU;DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD;DAT}$	1	–	–	μs
Acknowledge (from TDA8442) set-up time	$t_{SU;ACK}$	–	–	3.5	μs
Acknowledge (from TDA8442) hold time	$t_{HD;ACK}$	0	–	–	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs



Reference levels are 10 and 90%.

Fig. 5 I²C-bus timing; TDA8442.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

OCTUPLE 6-BIT DAC WITH I²C-BUS

GENERAL DESCRIPTION

The TDA8444 comprises eight digital-to-analogue converters (DACs) each controlled via the two-wire I²C-bus. The DACs are individually programmed using a 6-bit word to select an output from one of 64 voltage steps. The maximum output voltage of all DACs is set by the input V_{max} and the resolution is approximately $V_{max}/64$. At power-on all DAC outputs are set to their lowest value. The I²C-bus slave receiver has a 7-bit address of which 3 bits are programmable via pins A0, A1 and A2.

Features

- Eight discrete DACs
- I²C-bus slave receiver
- 16-pin DIL package

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	I_{CC}	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input	V_P = 12 V	V_{max}	1	–	10.5	V
DAC output voltage range		V_O	0.1	–	V_P–0.5	V
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

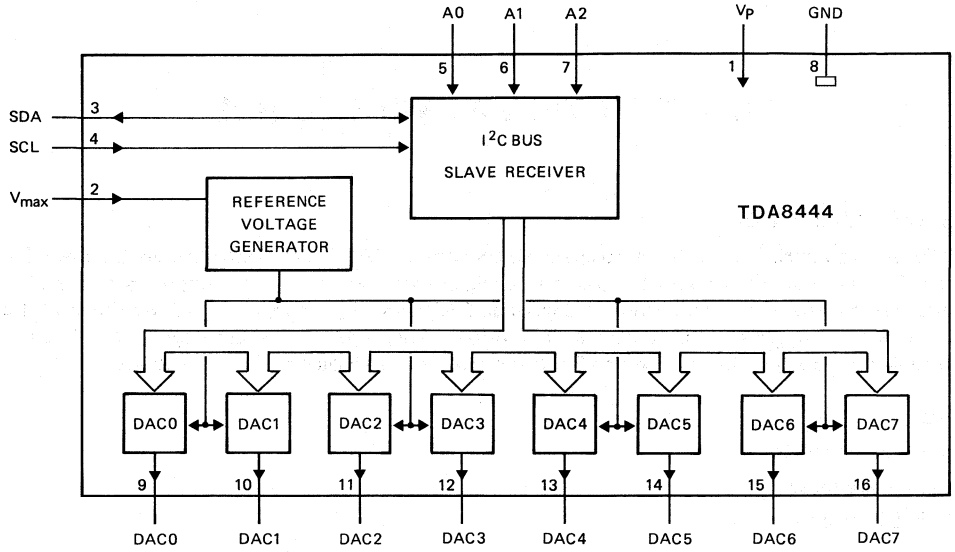


Fig. 1 Block diagram.

PINNING

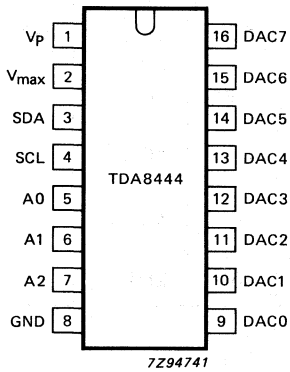


Fig. 2 Pinning diagram.

1	V_P	positive supply voltage
2	V_{max}	control input for DAC maximum output voltage
3	SDA	I^2C-bus serial data input/output
4	SCL	I^2C-bus serial data clock
5	A0	programmable address bits for I^2C-bus slave receiver
6	A1	
7	A2	
8	GND	ground
9-16	DAC0-7	analogue voltage outputs

FUNCTIONAL DESCRIPTION (continued)

Input V_{max}

Input V_{max} (pin 2) provides a means of compressing the output voltage swing of the DACs. The maximum DAC output voltage is restricted to approximately V_{max} while the 6-bit resolution is maintained, so giving a finer voltage resolution of smaller output swings.

Digital-to-analogue converters

Each DAC comprises a 6-bit data latch, current switches and an output driver. Current sources with values weighted by 2^0 up to 2^5 are switched according to the data input so that the sum of the selected currents gives the required analogue voltage from the output driver. The range of the output voltage is approximately 0.5 to 10.5 V when $V_{max} = V_P$.

The DAC outputs are protected against short-circuits to V_P and GND.

To avoid the possibility of oscillations, capacitive loading at the DAC outputs should not exceed 2 nF.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		$V_P = V_1$	−0.5	18	V
Supply current (source)		$I_p = I_1$	−	−10	mA
		$I_P = I_I$	−	40	mA
I^2C-bus line voltage		$V_{3,4}$	−0.5	5.9	V
Input voltage		V_I	−0.5	V_P + 0.5	V
Output voltage		V_O	−0.5	V_P + 0.5	V
Maximum current on any pin (except pins 1 and 8)		$\pm I_{max}$	−	10	mA
Total power dissipation		P_{tot}	−	500	mW
Operating ambient temperature range		T_{amb}	−20	+ 70	°C
Storage temperature range		T_{stg}	−55	+ 150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 75 K/W

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

FUNCTIONAL DESCRIPTION

I²C-bus

The TDA8444 I²C-bus interface is a receive-only slave. Data is accepted from the I²C-bus in the following format:

S	0 1 0 0 A2 A1 A0 0	A	I3 I2 I1 I0 SD SC SB SA	A	X X D5 D4 D3 D2 D1 D0	A	P
	← address byte →		← instruction byte →		← first data byte →		

Where:

S	= start condition	A2, A1, A0	= programmable address bits
P	= stop condition	I3, I2, I1, I0	= instruction bits
A	= acknowledge	SD, SC, SB, SA	= subaddress bits
X	= don't care	D5, D4, D3, D2, D1, D0	= data bits

Fig. 3 Data format.

Address byte

Valid addresses are 40, 42, 44, 46, 48, 4A, 4C, 4E (hexadec), depending on the programming of bits A2, A1 and A0. With these addresses, up to eight TDA8444 ICs can be operated independently from one I²C-bus. No other addresses are acknowledged by the TDA8444.

Instruction and data bytes

Valid instructions are 00 to 0F and F0 to FF (hexadec); the TDA8444 will not respond to other instruction values.

Instructions 00 to 0F cause auto-incrementing of the subaddress (bits SD to SA) when more than one data byte is sent within one transmission. With auto-incrementing, the first data byte is written into the DAC addressed by bits SD to SA and then the subaddress is automatically incremented by one position for the next data byte in the series.

Auto-incrementation does not occur with instructions F0 to FF. Other than auto-incrementation there is no difference between instructions 00 to 0F and F0 to FF. When only one data byte per transmission is present, the DAC addressed by the subaddress will always receive the data.

Valid subaddresses (bits SD to SA) are 0 to 7 (hexadec) relating numerically to DAC0 to DAC7. When the auto-incrementing function is used, the subaddress will sequence through all possible values (0 to F, 0 to F, etc.).

I²C-bus

Input SCL (pin 3) and input/output SDA (pin 4) conform to I²C-bus specifications.* Pins 3 and 4 are protected against positive voltage pulses by internal zener diodes connected to the ground plane and therefore the normal bus line voltage should not exceed 5.5 V.

The address inputs A0, A1, A2 are programmed by a connection to GND for An = 0 or to V_P for An = 1. If the inputs are left floating, An = 1 will result.

CHARACTERISTICS

All voltages are with respect to GND; T_{amb} = 25 °C; V_P = 12 V unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Voltage level for power-on reset		V_1	1	–	4.8	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	$I_P = I_1$	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input (pin 2)	V_P = 12 V	$V_{max} = V_2$	1.0	–	10.5	V
Pin 2 current	V_2 = 1 V	I_2	–	–	−10	μA
	$V_2 = V_P$	I_2	–	–	10	μA
SDA, SCL inputs (pins 3 and 4)						
Input voltage range		V_I	0	–	5.5	V
Input voltage LOW		V_{IL}	–	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	–	V
Input current LOW	$V_{3;4}$ = 0.3 V	I_{IL}	–	–	−10	μA
Input current HIGH	$V_{3;4}$ = 6 V	I_{IH}	–	–	±10	μA
SDA output (pin 3)						
Output voltage LOW	I_3 = 3 mA	V_{OL}	–	–	0.4	V
Sink current		I_O	3	8	–	mA
Address inputs (pins 5 to 7)						
Input voltage range		V_I	0	–	5	V
Input voltage LOW		V_{IL}	–	–	1	V
Input voltage HIGH		V_{IH}	2.1	–	–	V
Input current LOW		I_{IL}	–	−7	−12	μA
Input current HIGH		I_{IH}	–	–	1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
DAC outputs (pins 9 to 16)						
Output voltage range		V_O	0.1	–	V_P–0.5	V
Minimum output voltage	data = 00; I_O = –2 mA	V_{Omin}	0.1	0.4	0.8	V
Maximum output voltage	data = 3F; I_O = –2 mA					
at $V_{max} = V_P$		V_{Omax}	10	10.5	11.5	V
at $1 < V_{max} < 10.5$ V		V_{Omax}		see note		V
Output sink current	V = V_P; data = 1F	I_O	2	8	15	mA
Output source current	V = 0V; data = 1F	I_O	–2	–	–6	mA
Output impedance	data = 1F; $-2 < I_O < +2$ mA	Z_O	–	4	50	Ω
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV
Deviation from linearity	I_O = –2 mA; N ≠ 32		0	–	50	mV
Deviation from linearity	I_O = –2 mA; N = 32		0	–	70	mV

Note to the characteristics

$V_O = 0.95\ V_{max} + V_{Omin}$.

APPLICATION INFORMATION

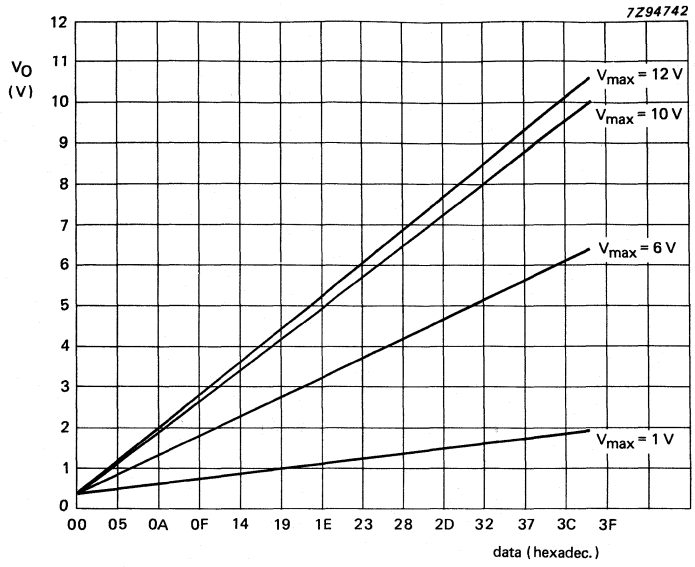


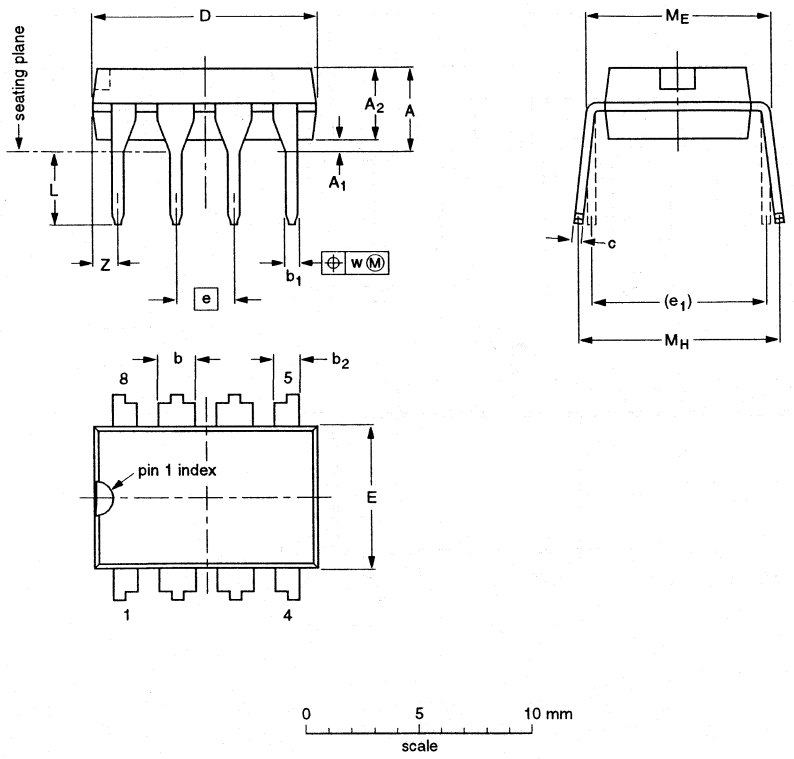
Fig. 4 Graph showing output voltage as a function of the input data value for V_{max} values of 1, 6, 10 and 12 V; V_P = 12 V.

PACKAGE INFORMATION

INDEX

DIP

DIP8: plastic dual in-line package; 8 leads (300 mil) SOT97-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

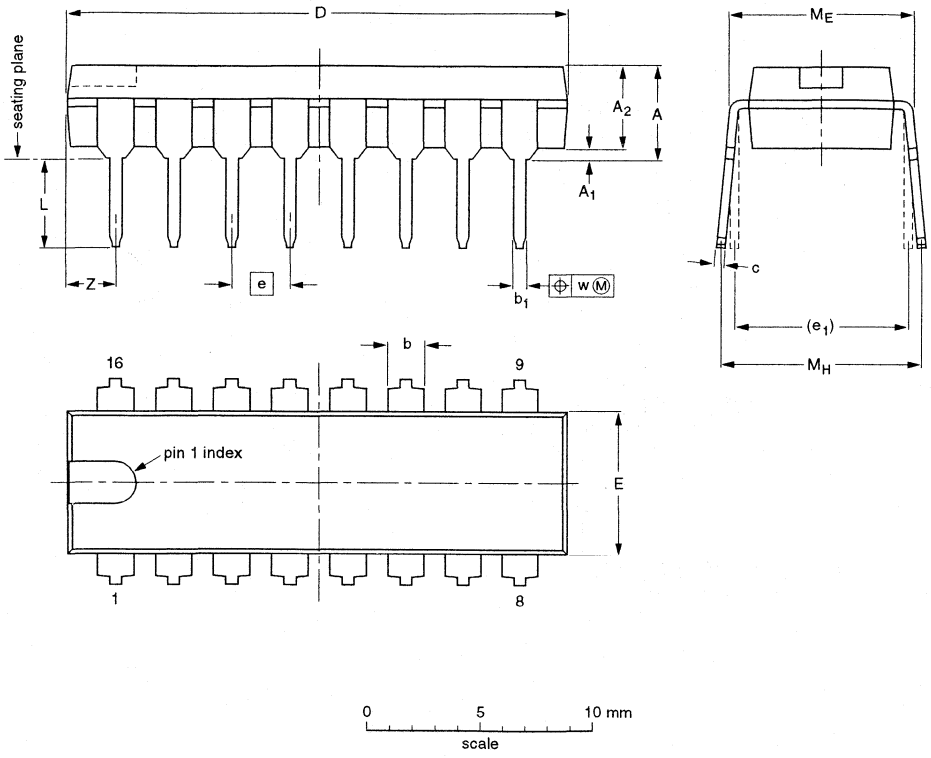
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

DIP16: plastic dual in-line package; 16 leads (300 mil); long body SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

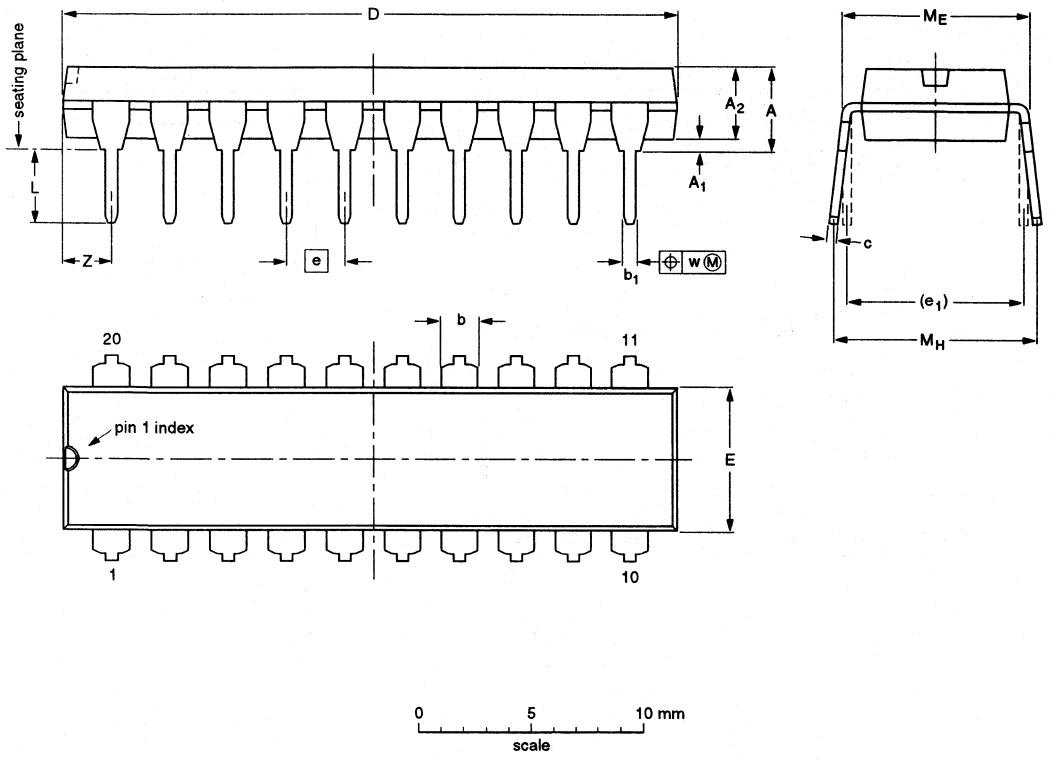
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

DIP20: plastic dual in-line package; 20 leads (300 mil) SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

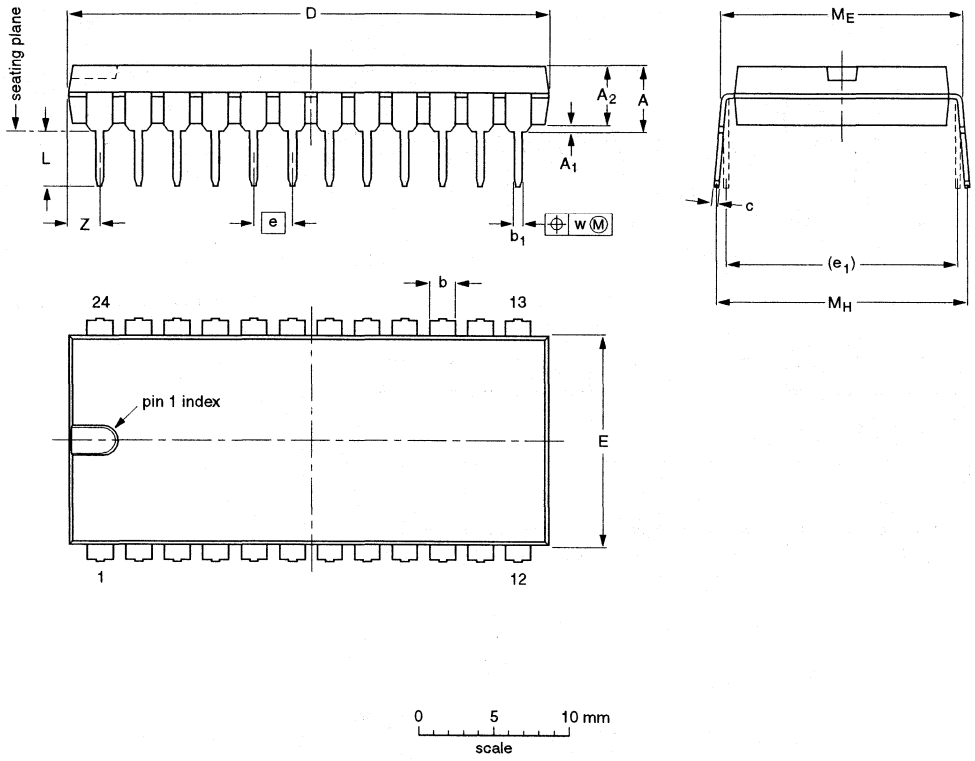
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

DIP24: plastic dual in-line package; 24 leads (600 mil) SOT101-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

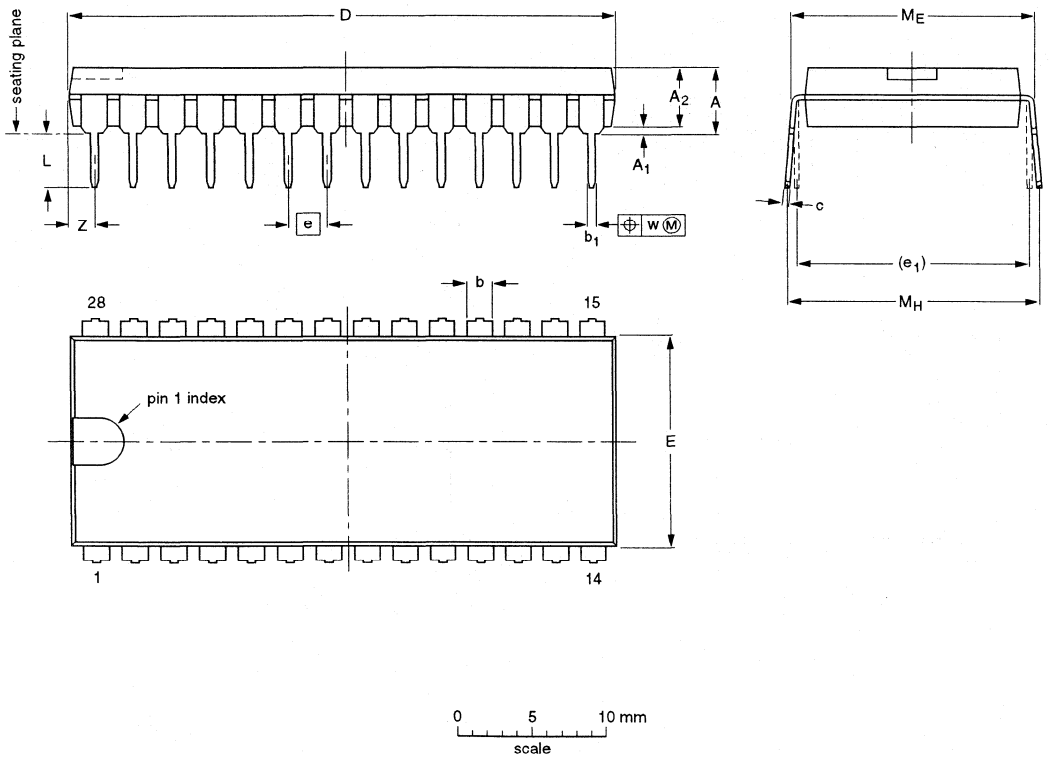
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT101-1	051G02	MO-015AD				~~92-11-17~~ 95-01-23

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

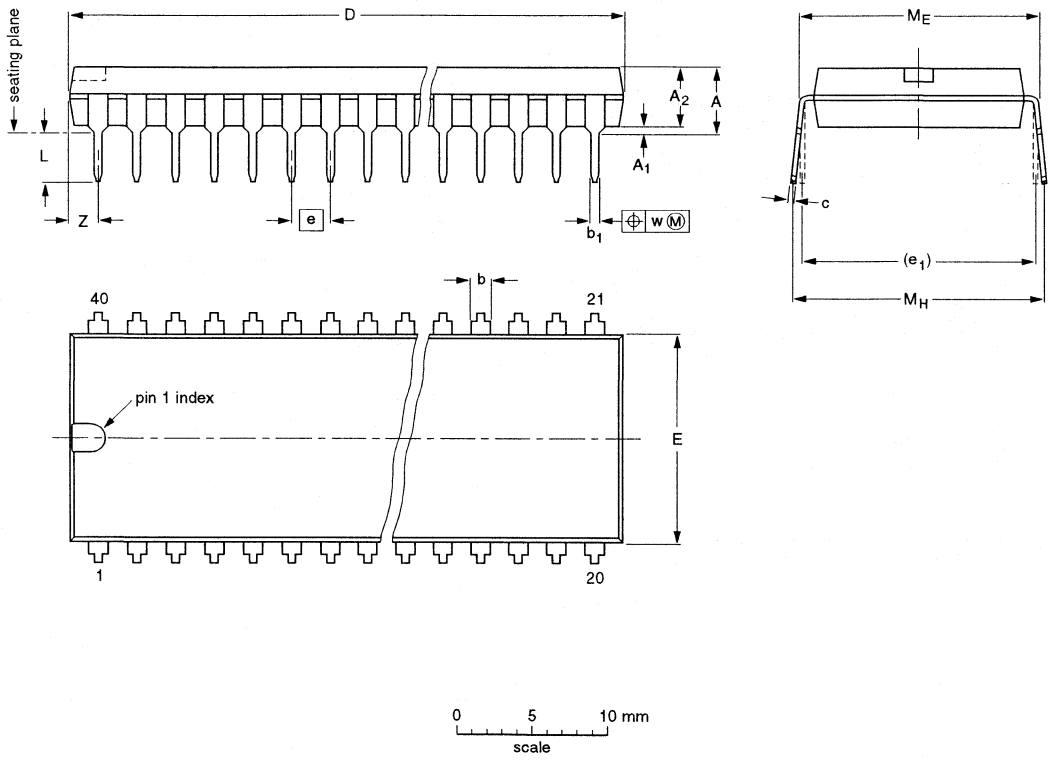
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

DIP40: plastic dual in-line package; 40 leads (600 mil) SOT129-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

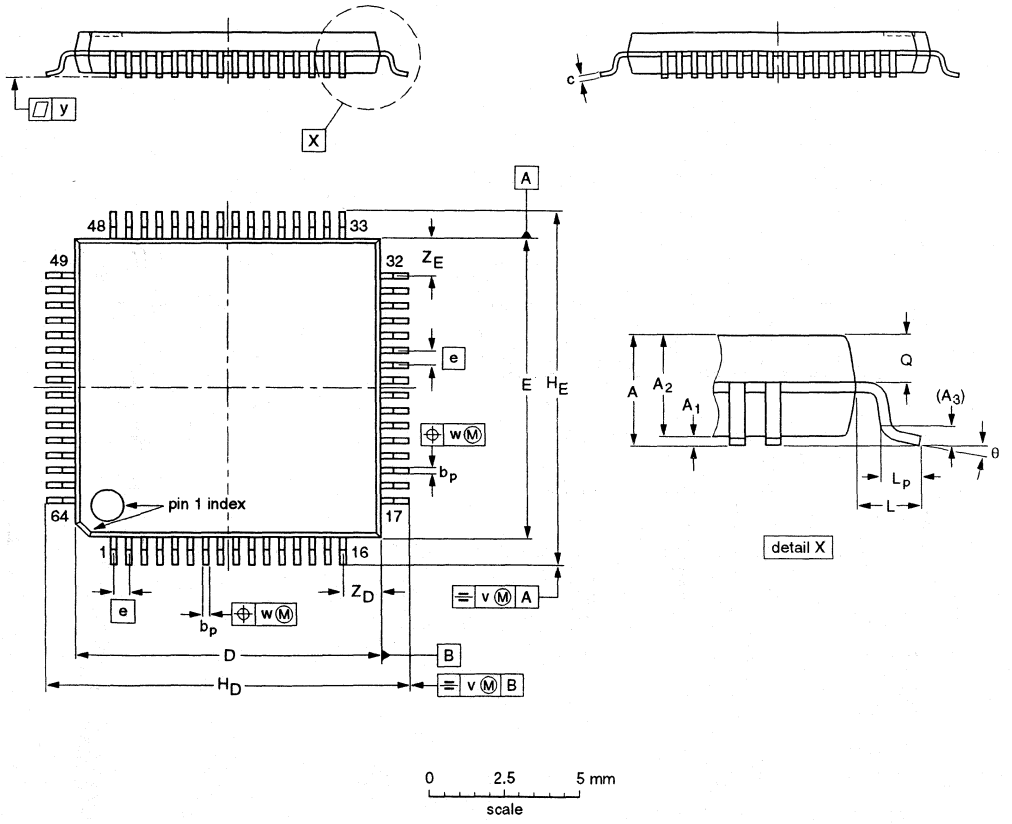
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

LQFP

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm SOT314-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7° 0°

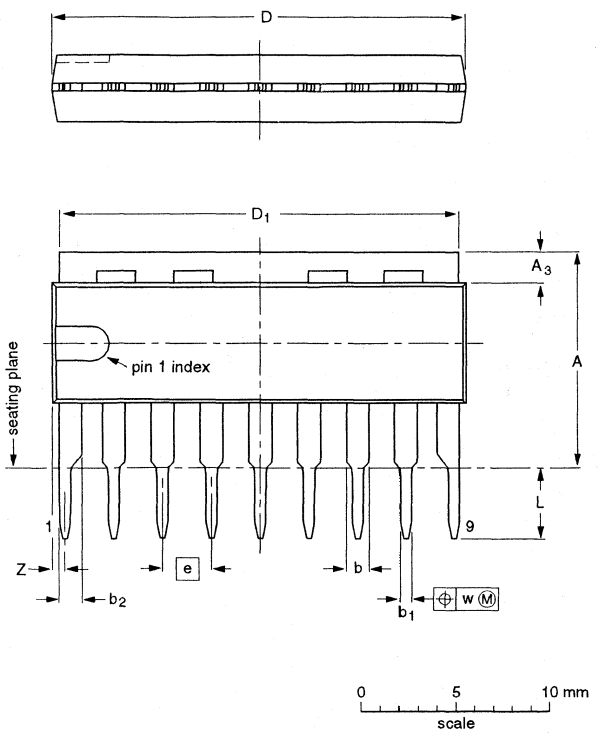
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT314-2						~~94-01-07~~ 95-02-25

SIL

SIL9MP: plastic single in-line medium power package; 9 leads SOT142-1



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2 max.	A_3	b	b_1	b_2	c	$D^{(1)}$	D_1	$E^{(1)}$	e	L	Q	w	$Z^{(1)}$ max.
mm	12 11	3.7	1.8 1.4	1.40 1.14	0.67 0.50	1.40 1.14	0.48 0.38	21.8 21.4	21.4 20.7	6.48 6.20	2.54	3.9 3.4	1.75 1.55	0.25	1.0

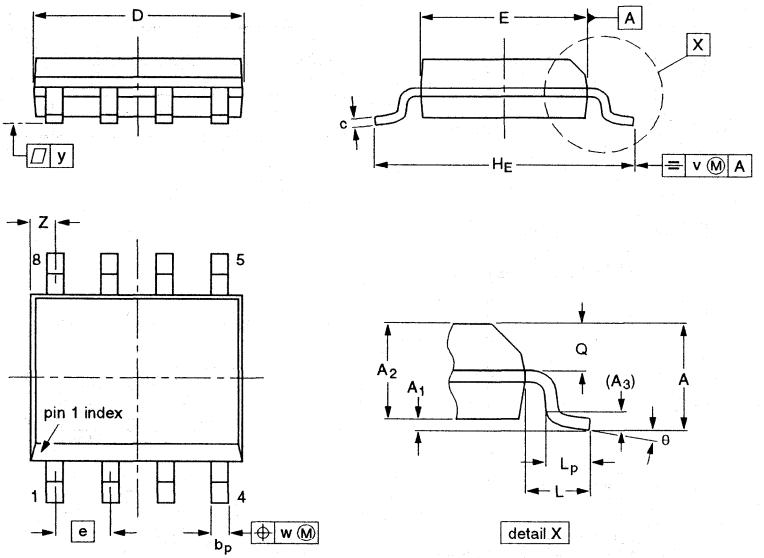
Note

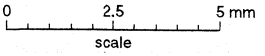
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT142-1						~~92-11-17~~ 95-02-09

SO

SO8: plastic small outline package; 8 leads; body width 3.9 mm SOT96-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

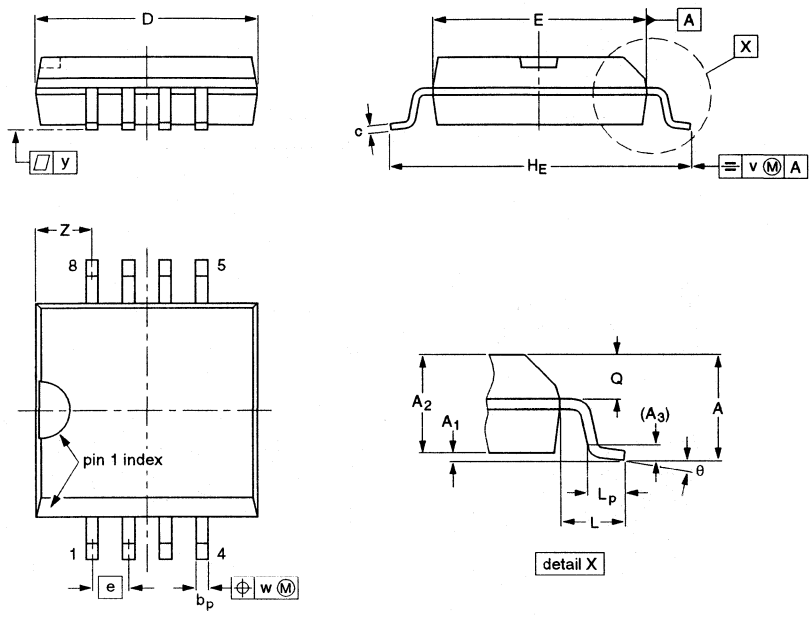
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.20 0.19	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~92-11-17~~ 95-02-04

SO8: plastic small outline package; 8 leads; body width 7.5 mm **SOT176-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

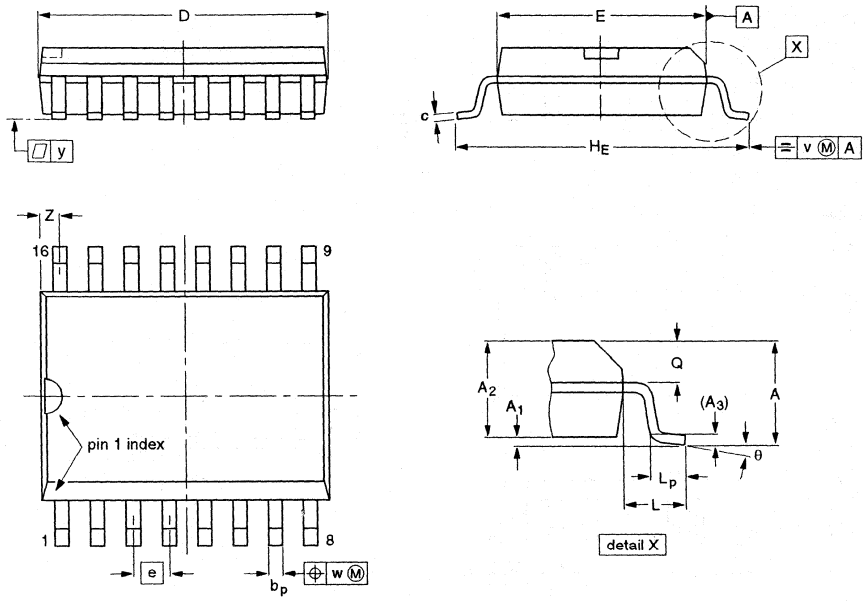
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	7.65 7.45	7.6 7.4	1.27	10.65 10.00	1.45	1.1 0.45	1.1 1.0	0.25	0.25	0.1	2.0 1.8	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.30 0.29	0.30 0.29	0.050	0.42 0.39	0.057	0.043 0.018	0.043 0.039	0.01	0.01	0.004	0.079 0.071	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT176-1						~~91-08-13~~ 95-02-25

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

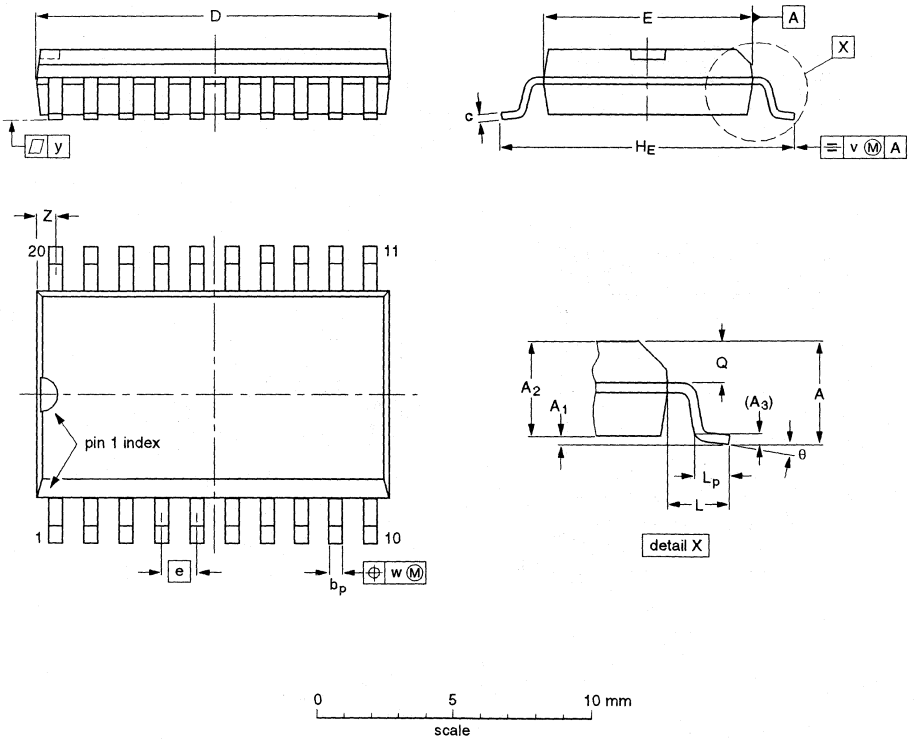
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~92-11-17~~ 95-01-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

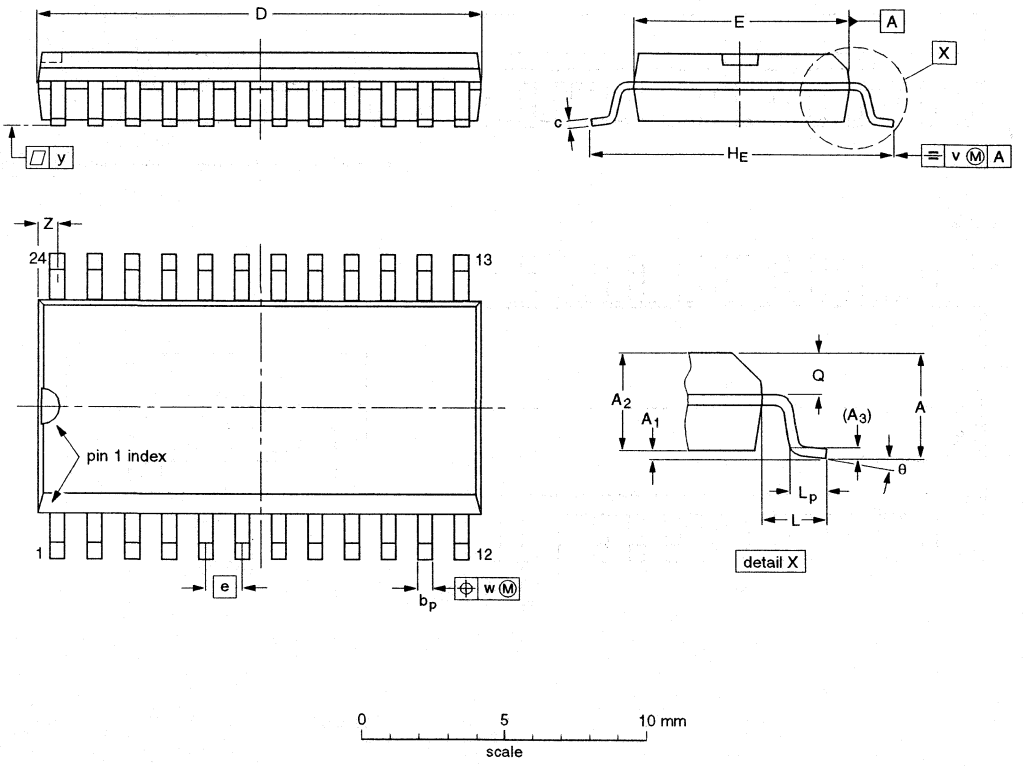
UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SO24: plastic small outline package; 24 leads; body width 7.5 mm SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

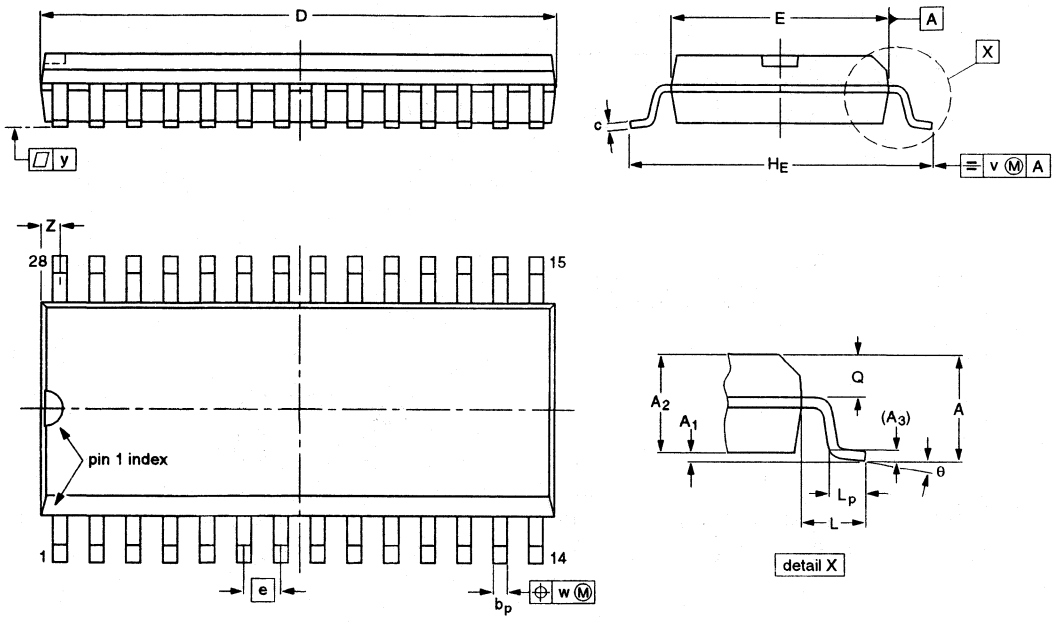
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~92-11-17~~ 95-01-24

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

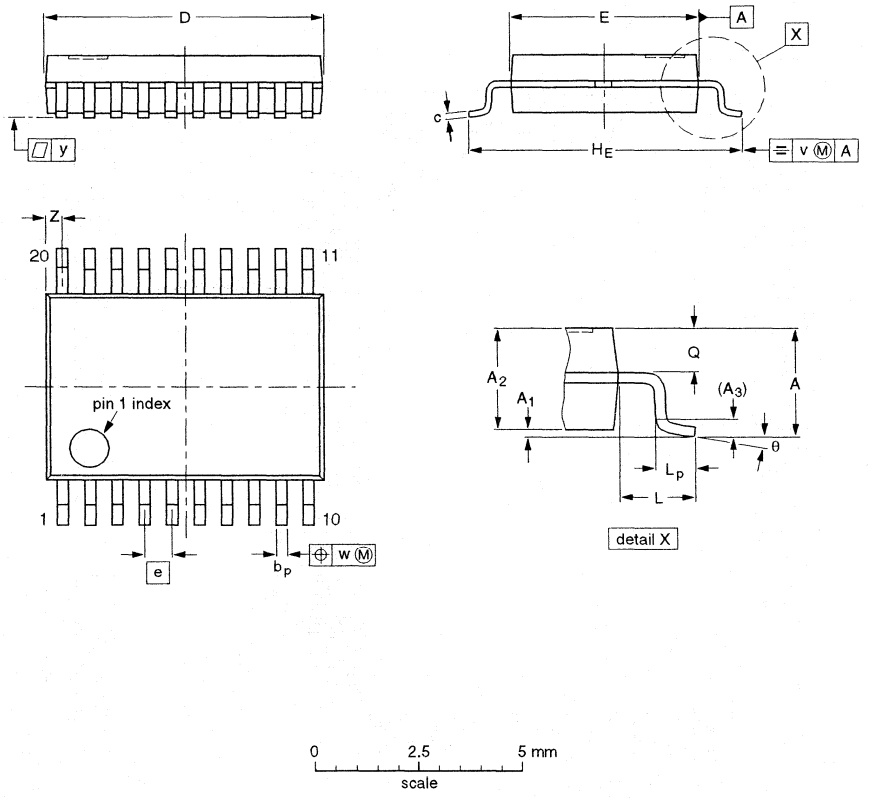
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~91-08-13~~ 95-01-24

SSOP

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm SOT266-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

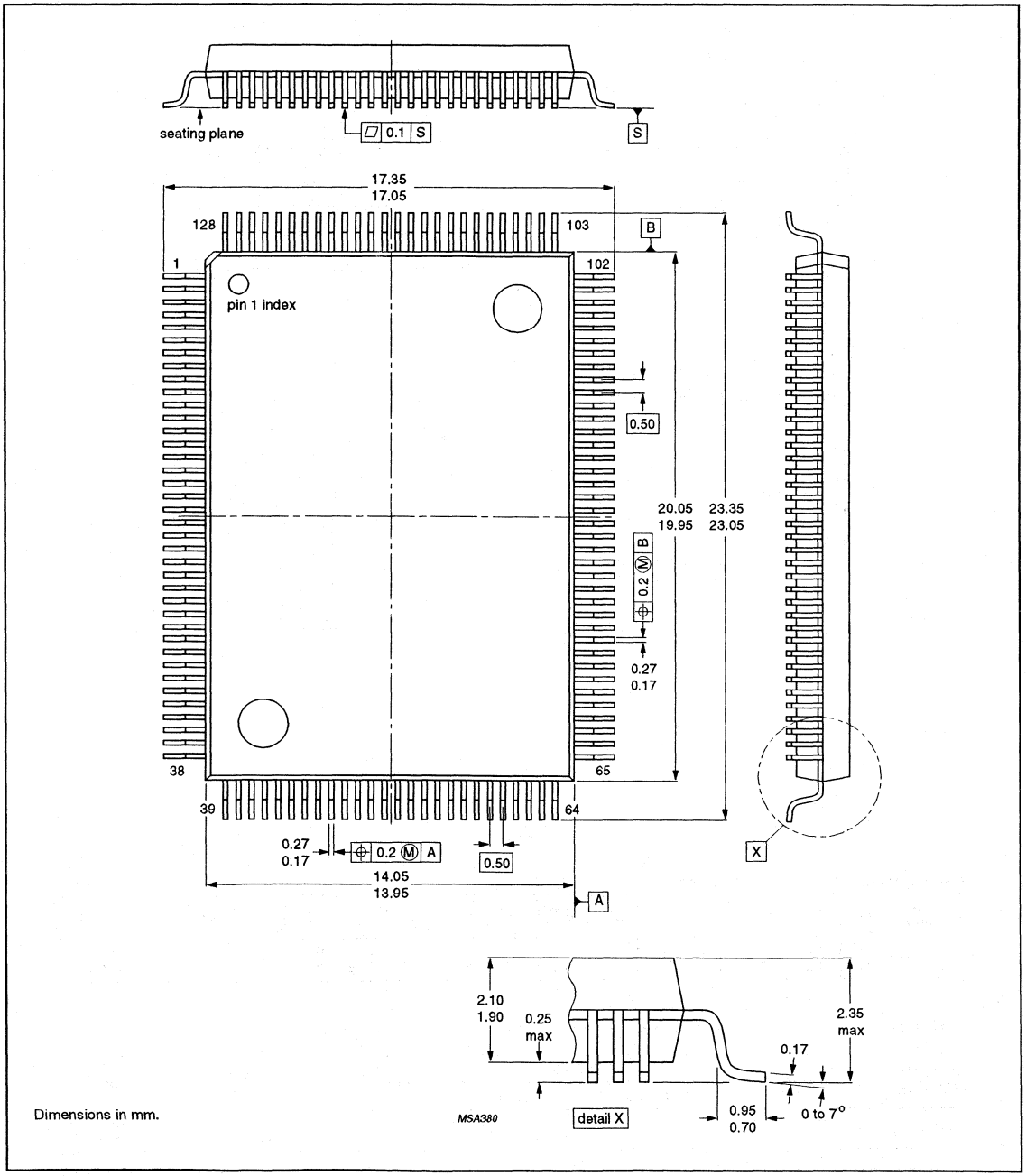
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1							~~90-04-05~~ 95-02-25

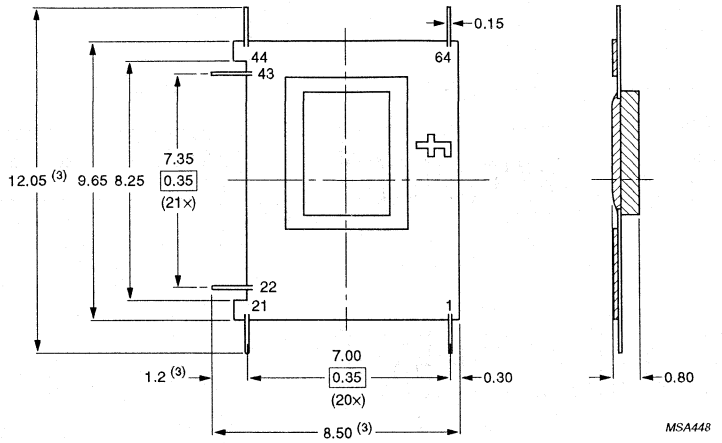
SQFP

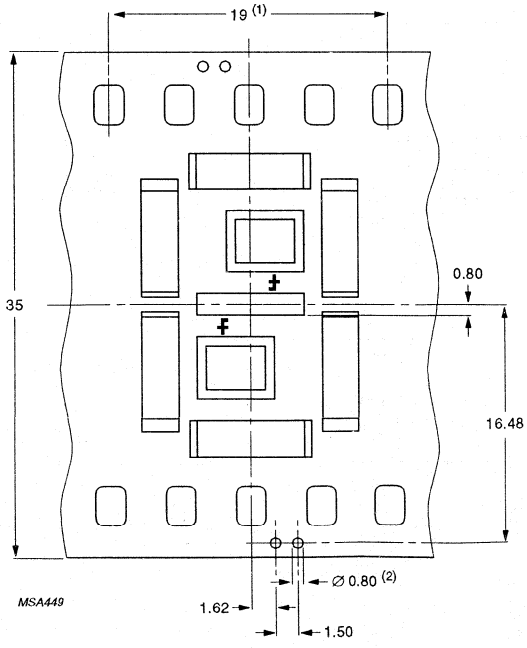
SQFP128: plastic shrink quad flat package;
128 leads (lead length 1.6 mm); body 14 x 20 x 2.0 mm **SOT387-1**

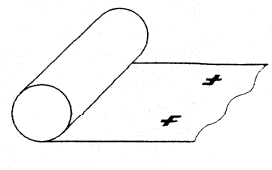


TAB

TAB64: tape automated bonding module; 64 leads SOT267







Dimensions in mm.

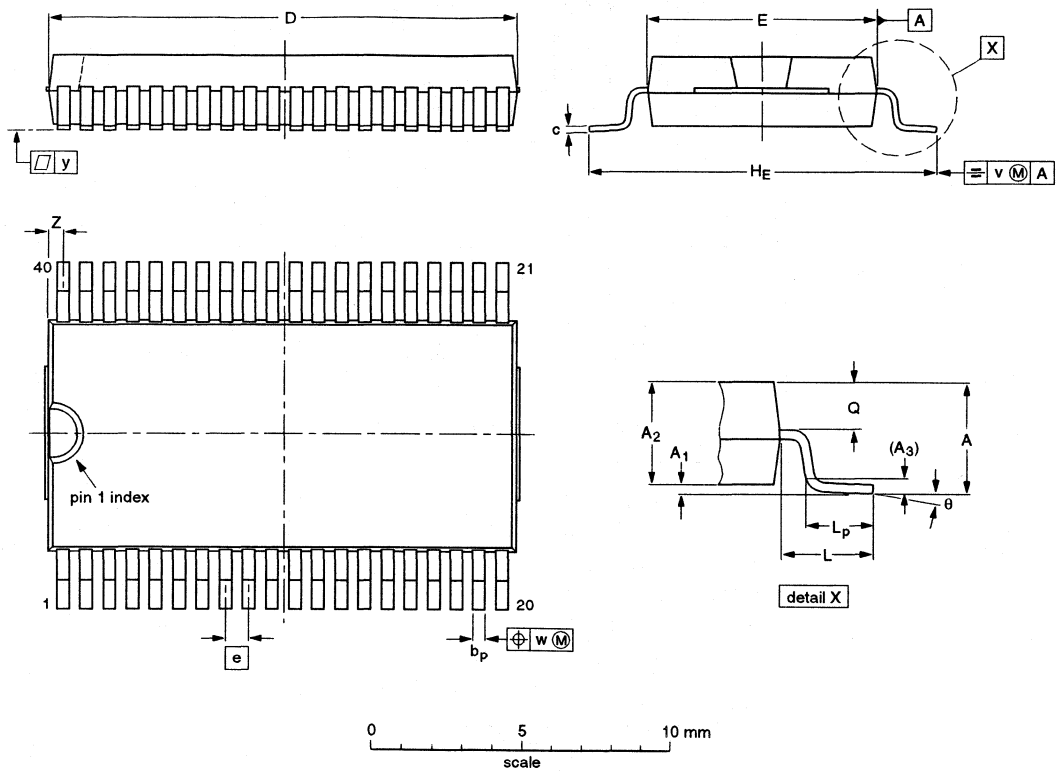
(1) 1 pattern = 4 perforation pitch intervals (contains two modules).

(2) Circuit-test holes.

(3) Fixed by the user.

VSO

VSO40: plastic very small outline package; 40 leads SOT158-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

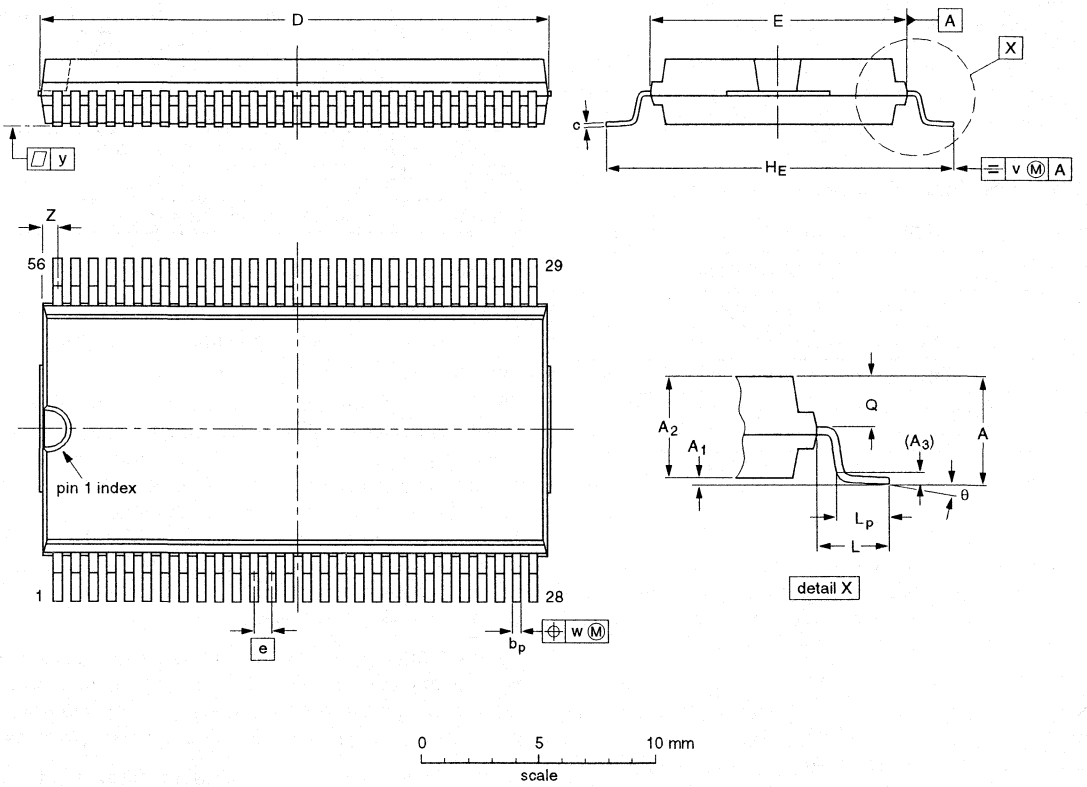
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.70	0.3 0.1	2.45 2.25	0.25	0.42 0.30	0.22 0.14	15.6 15.2	7.6 7.5	0.762	12.3 11.8	2.25	1.7 1.5	1.15 1.05	0.2	0.1	0.1	0.6 0.3	7° 0°
inches	0.11	0.012 0.004	0.096 0.089	0.010	0.017 0.012	0.0087 0.0055	0.61 0.60	0.30 0.29	0.03	0.48 0.46	0.089	0.067 0.059	0.045 0.041	0.008	0.004	0.004	0.024 0.012	

Notes

1. Plastic or metal protrusions of 0.4 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT158-1						~~92-11-17~~ 95-01-24

VSO56: plastic very small outline package; 56 leads **SOT190-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	3.3	0.3 0.1	3.0 2.8	0.25	0.42 0.30	0.22 0.14	21.9 21.5	11.1 11.0	0.75	15.8 15.2	2.25	1.6 1.4	1.45 1.30	0.2	0.1	0.1	0.90 0.55	7° 0°
inches	0.13	0.012 0.004	0.12 0.11	0.01	0.017 0.012	0.0087 0.0085	0.86 0.55	0.44 0.43	0.03	0.62 0.60	0.089	0.063 0.055	0.057 0.051	0.008	0.004	0.004	0.035 0.022	

Note

1. Plastic or metal protrusions of 0.3 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT190-1						~~92-11-17~~ 95-01-24

Package information — Soldering

INTRODUCTION

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

THROUGH-HOLE MOUNTED PACKAGES

Table 1 Types of through-hole mounted packages

TYPE	DESCRIPTION
DIP	plastic dual in-line package
SDIP	plastic shrink dual in-line package
HDIP	plastic heat-dissipating dual in-line package
DBS	plastic dual in-line bent from a single in-line package
SIL	plastic single in-line package

Soldering by dipping or wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SURFACE MOUNTED PACKAGES

Table 2 Types of surface mounted packages

TYPE	DESCRIPTION
SO	plastic small outline package
SSOP	plastic shrink small outline package
TSSOP	plastic thin shrink small outline package
VSO	plastic very small outline package
QFP	plastic quad flat package
LQFP	plastic low profile quad flat package
SQFP	plastic shrink quad flat package
TQFP	plastic thin quad flat package
PLCC	plastic leaded chip carrier

Reflow soldering

Reflow soldering techniques are suitable for all SMD packages, ease of soldering varies with the type of package as indicated in Table 3.

The choice of heating method may be influenced by larger plastic packages (QFP or PLCC with 44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information on moisture prevention, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Table 3 Suitability of surface mounted packages for various soldering methods: rating from 'a' to 'd': **'a' indicates most suitable** (soldering is not difficult); **'d' indicates least suitable** (soldering is achievable with difficulty).

PACKAGE TYPE	REFLOW METHOD					DOUBLE WAVE METHOD
	INFRARED	HOT BELT	HOT GAS	VAPOUR PHASE	RESISTANCE	
SO	a	a	a	a	d	a
SSOP	a	a	a	c	d	c
TSSOP	b	b	b	c	d	d
VSO	b	b	a	b	a	b
QFP	b	b	a	c	a	c
LQFP	b	b	a	c	d	d
SQFP	b	b	a	c	d	d
TQFP	b	b	a	c	d	d
PLCC	c	b	b	d	d	b

Wave soldering

Wave soldering is **not** recommended for SSOP, TSSOP, QFP, LQFP, SQFP or TQFP packages, this is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- For SSOP, TSSOP and VSO packages, the longitudinal axis of the package footprint must be parallel to the solder flow **and** must incorporate solder thieves at the downstream end.
- For QFP, LQFP and TQFP packages, the footprint must be at an angle of 45° to the board direction **and** must incorporate solder thieves downstream and at the side corners.

Even with these conditions, consider wave soldering only for the following package types:

- SO
- VSO
- PLCC
- SSOP **only with body width 4.4 mm**, e.g. SSOP16 (SOT369-1) or SSOP20 (SOT266-1).
- QFP **except** QFP52 (SOT379-1), QFP100 (SOT317-1, SOT317-2, SOT382-1) and QFP160 (SOT322-1); these are **not** suitable for wave soldering.
- LQFP **except** LQFP32 (SOT401-1), LQFP48 (SOT313-1, SOT313-2), LQFP64 (SOT314-2), LQFP80 (SOT315-1); these are **not** suitable for wave soldering.
- TQFP **except** TQFP64 (SOT357-1), TQFP80 (SOT375-1) and TQFP100 (SOT386-1); these are **not** suitable for wave soldering.

SQFP are **not** suitable for wave soldering.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DATA HANDBOOK SYSTEM

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SC08b	RF Power Transistors for UHF
SC09	RF Power Modules
SC10	Surface Mounted Semiconductors
SC13	PowerMOS Transistors including TOPFETs and IGBTs
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Magnetic products

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Printed in the USA

5278K/413051/45M/FP/pp624 Date of release: 10-95

Document order number: 9397 750 00306

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